METHEUS
OMEGA-MCU
MEMORY CONTROL UNIT

Features

- 16Mhz System Clock
- Graphics Operations as fast as 4 Pixels per Clock (64 MPixels)
- 10 Mpixel average vector draw, 16 Mpixel max.
- Patented "Page Mode Drawing"
- Pixel Cache for Block Moves
- Multiple MCUs Cascade up to 32 Bits/Pixel
- Logical and Arithmetic Raster Ops
- Three Operand Logical Operations, Source, Constant, and Destination
- Logical Ops on 4 Pixels Paralell
- Four Memory Address Registers
- Two port frame buffer access
- Access Memory as Word or Pixel
- Specifically Designed New Generation Video Memories

Product Description

The OMEGA-MCU provides all the video frame-buffer address and data control required in a high performance graphics system. The chip is intended as a Z-Bus Slave for the OMEGA-GPU Graphics Processor.

The OMEGA-MCU contains address registers, a pixel cache, and both arithmetic and logical raster-op logic. Many low-level pixel operations occur at the frequency of the system clock. These include vectors, character copies and block moves. Area fill operations run at four times the system clock or 64 Mpixel/sec.

The OMEGA-MCU also supports simultaneous host access to the frame buffer. The host may use this path to pass data/commands to/from the graphics system or to directly manipulate the pixel data.

The Omega-MCU is implemented in low power CMOS technology and operates at input clock rates to 16 Mhz.

The Omega-MCU is packaged in a low cost 120-pin plastic flat-pack.

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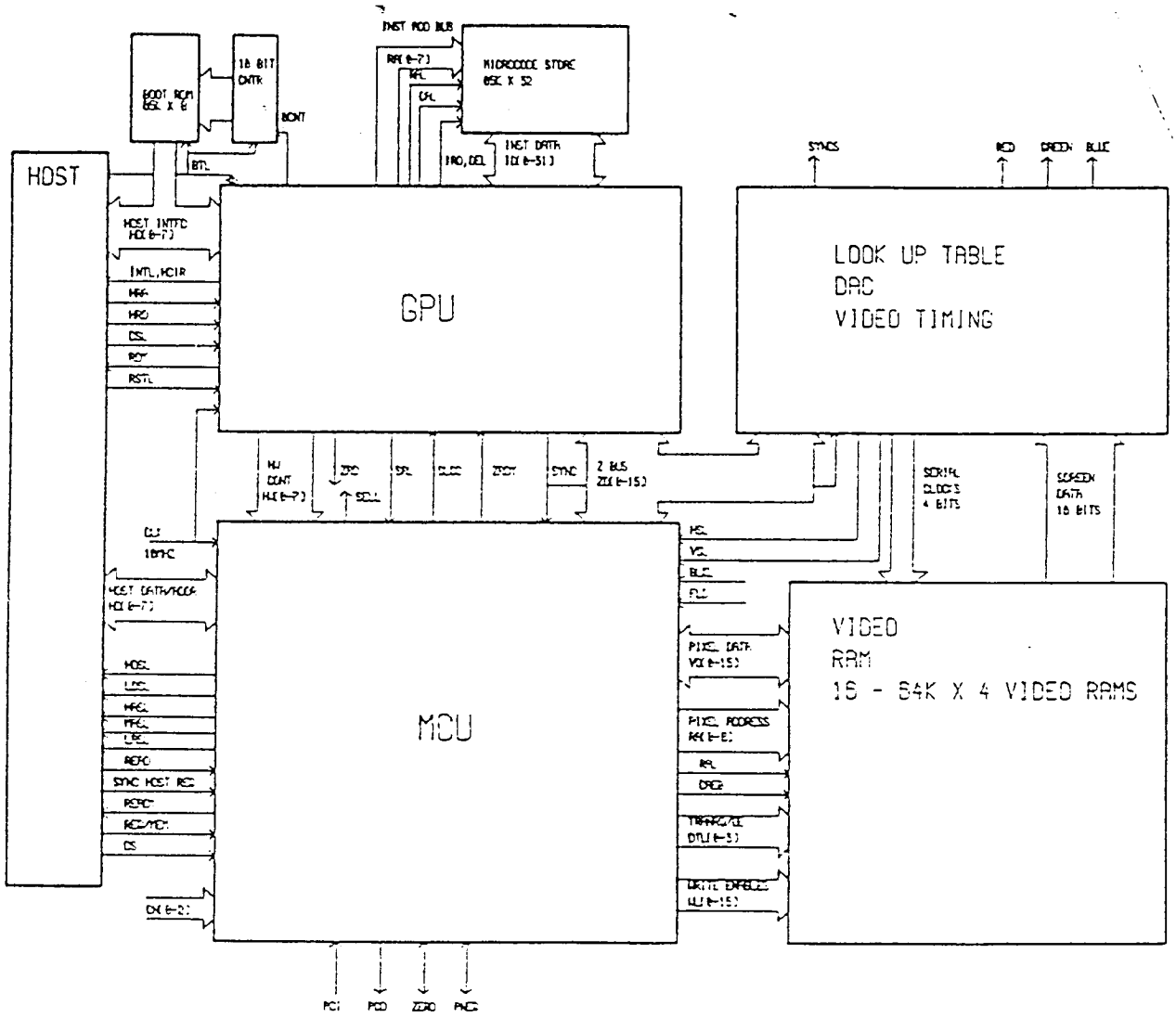
Functional Description

The OMEGA-MCU executes graphics oriented memory operations under control of an OMEGA-GPU or a host. The OMEGA-MCU has four interfaces:

- Interface to the OMEGA-GPU via the Z-Bus.
- Interface to the host.
- Interface to the frame-buffer.
- Interface to the video output.

MCU Based Graphics System Block Diagram
Four Bits per Pixel



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Functional Description (continued)

Z-Bus Interface

The Z-Bus interface supports the high speed synchronous bus used by the OMEGA-GPU to control the graphics subsystem. From the OMEGA-GPU, the OMEGA-MCU receives set-up and control information for it's internal registers over the data lines and receives execution type information over the hardware control lines. This setup and control may occur in parallel to minimize execution times.

The Z-Bus register interface operation is initiated by the ZADR signal. The GPU follows a ZADR by placing the next Z-Bus register address and direction (read or write) on the Z-Bus data lines for two system clocks. The Z-Bus slave, in this case the MCU, latches this address on the second system clock. Assuming the MCU is the selected Zbus slave, during the next two to n system clocks data are transferred from/to the GPU and the addressed register. Either the GPU or the MCU may extend this data cycle beyond the two clock minimum. The GPU signals the end of the data cycle by asserting the SYNC signal.

The Z-Bus hardware control lines are interpreted by the MCU at the end of the data cycle on the positive edge of the system clock when SYNC is active. The MCU uses these controls to activate eight internal operations which transfer data to and from the memory, increment/decrement registers and shift data within the MCU.

The MCU can control the flow of data on the Z-Bus by delaying the return of ZRDY to the GPU. This would occur if a register transfer were attempted while a previously requested operation was still in process.

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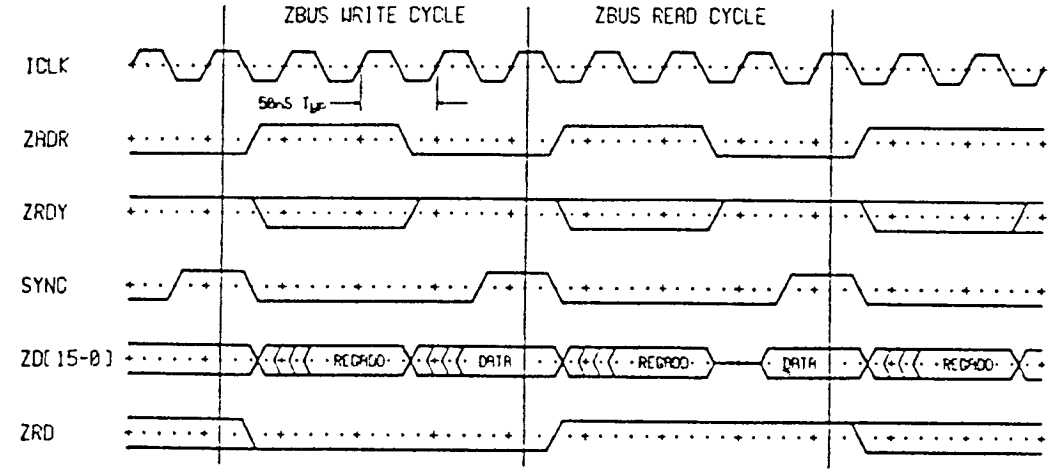
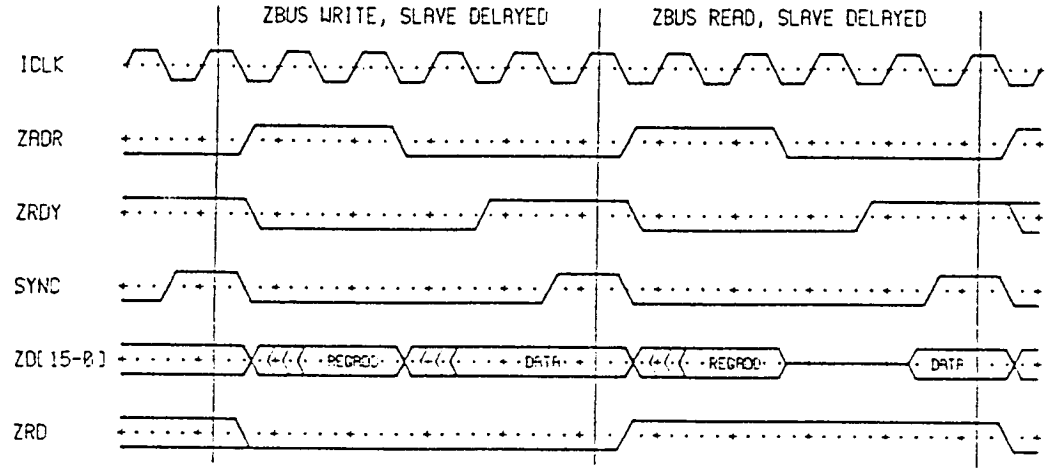
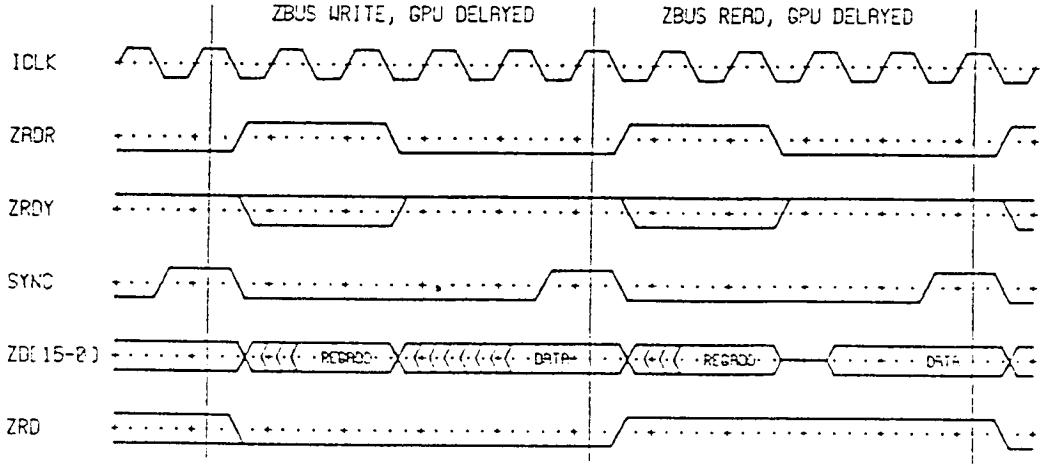
Typical Zbus Cycles







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Functional Description (continued)

Host Interface

The host interface allows the host to directly access the frame buffer controlled through the MCU. The host may have an 8-bit or 16-bit data path and use two types of transfers: I/O and Memory. The host interface is byte serial on this MCU to minimize pin count.

The I/O transfer allows the Graphics Subsystem to map up to 256 bytes of frame buffer into the host I/O space. This area may be used for a command/data communication area or to replace registers required to emulate another graphic system (such as CGA on a IBM PC). For the I/O transfer, the MCU will request only one byte of address following the Host Request (HRQ) before beginning the requested operation.

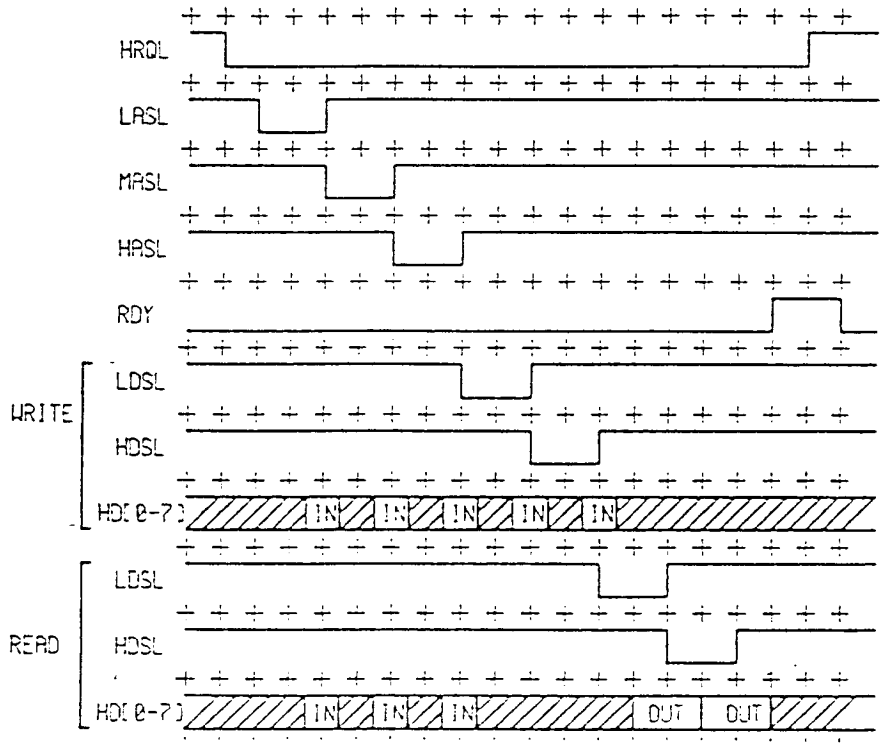
The memory transfer allows the host access to the entire MCU frame buffer (up to 8 Megabytes). A memory transfer request prompts the MCU to ask for three bytes of address before beginning the operation.

In the case of a read once the address is read into the MCU the read operation is carried out in MCU memory. When the memory read is complete the MCU strobes the data out on the Host Interface bus with the appropriate strobes.

In the case of a write once the address is read into the MCU the MCU requests one or two data bytes depending on the H16 signal. After the data is in the MCU will initiate a memory write operation into the video frame buffer.

In both the read and the write case the MCU returns the HRDY signal when the operation is complete.

Typical Host Operation (16 bit memory op)



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Functional Description (continued)

Frame-Buffer Interface

The frame-buffer interface of the MCU is designed to connect directly to 150ns 64K x 4-bit or 256K x 4-bit Video Dynamic RAMs (VDRAM). The MCU drives 9 address lines, RAS, CAS, write enables, and output enables according to the specifications of a 150ns VDRAM. The MCU requires VDRAM with the "Page Mode Access" feature. These memories are available from Fujitsu, NEC, TI and Mitsubishi.

Video Interface

The MCU requires the video sync and blanking signals to support the video data-transfer operations from the VDRAM. This interface may also supply a field input (FLD) in the case of interlaced displays.

The MCU fully implements transfer address manipulations required for interlace, pan and zoom.

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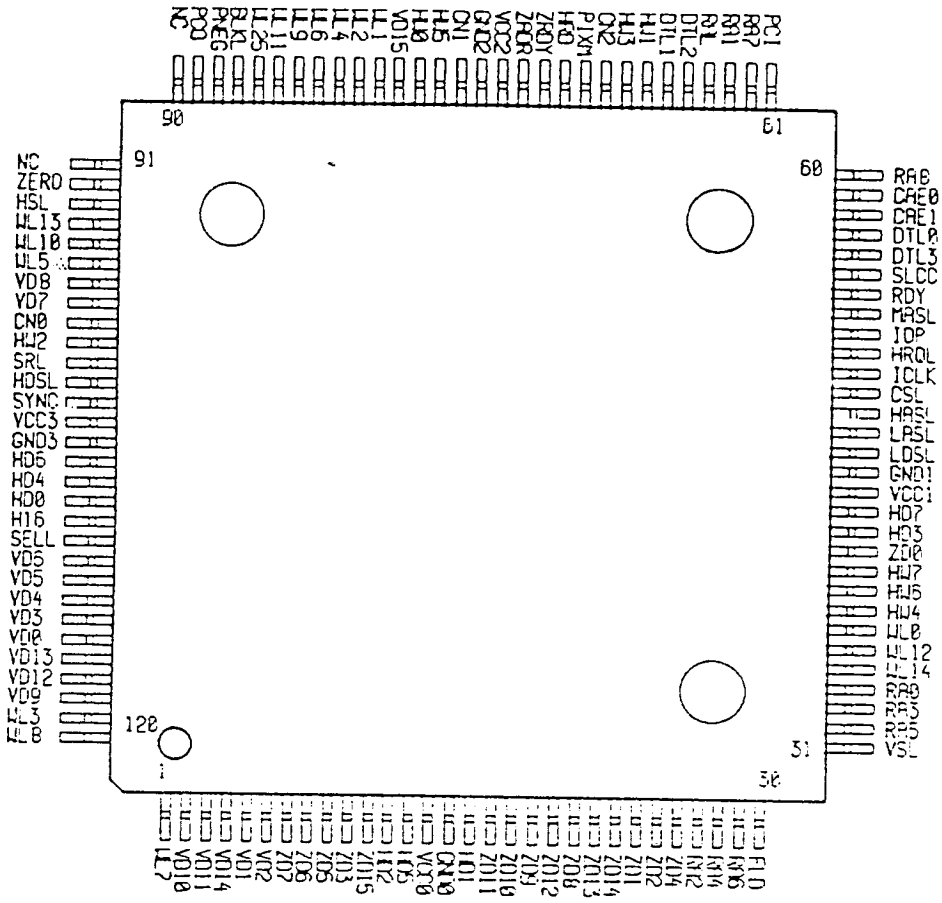
Pin Descriptions

120 Pin Plastic Flat Pack Pinout



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Pin Description (continued)

Pin Names to Pin Numbers Alphabetically

BLKL	87	HD2	12	LASL	47	SRL	101	VCC1	44	ZD0	41
CAE0	59	HD3	42	LDSL	46	SYNC	103	VCC2	74	ZD1	24
CAE1	58	HD4	107	MASL	53	VD0	115	VCC3	104	ZD10	18
CN0	99	HD5	13	PC1	61	VD1	5	WL0	37	ZD11	17
CN1	76	HD6	106	PCO	89	VD10	2	WL1	80	ZD12	20
CN2	69	HD7	43	PIXM	70	VD11	3	WL10	95	ZD13	22
CSL	49	HDSL	102	PNEG	68	VD12	117	WL11	85	ZD14	23
DTL0	57	HRD	71	RA0	34	VD13	116	WL12	36	ZD15	11
DTL1	66	HRDL	51	RA1	63	VD14	4	WL13	94	ZD2	25
DTL2	65	HSL	93	RA2	27	VD15	79	WL14	35	ZD3	10
DTL3	56	HW0	78	RA3	33	VD2	6	WL15	86	ZD4	26
FLD	30	HW1	67	RA4	28	VD3	114	WL2	81	ZD5	9
GND0	15	HW2	100	RA5	32	VD4	113	WL3	119	ZD6	8
GND1	45	HW3	68	RA6	29	VD5	112	WL4	82	ZD7	7
GND2	75	HW4	38	RA7	62	VD6	111	WL5	96	ZD8	21
GND3	105	HW5	77	RAB	60	VD7	98	WL6	83	ZD9	19
H16	109	HW6	39	RAL	64	VD8	97	WL7	1	ZERO	92
HASL	48	HW7	40	RDY	54	VD9	118	WL8	120	ZROY	72
HD0	108	ICLK	50	SELL	110	VSL	31	WL9	84		
HD1	16	IOP	52	SLCC	55	VCC0	14	ZADR	73		

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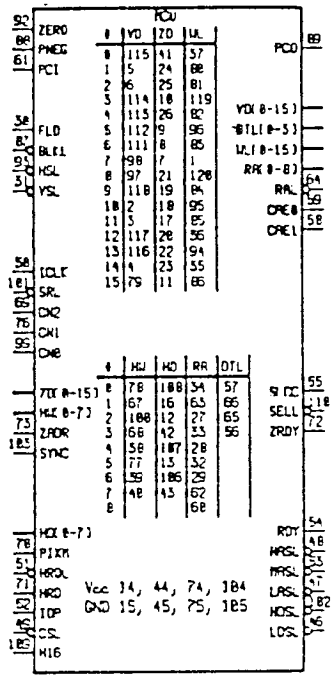
Pin Description (continued)

MCU Schematic Symbol



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Pin Description (continued)

OMEGA-MCU Signals for Video Memory		
Signal	Direction	Description
DTL[0-3]	Output	The Data Transfer pins are connected directly to the Transfer Enable/Output Enable pins of the video memory chips. These signals are negative true and, when true with RAL, indicates a transfer to the internal shift register. When either CAE0 or CAE1 is true, they turn on the VRAM output buffers.
RA[0-8]	Output	The video RAM Address pins communicate the address to be read or written to the video RAM. The address is a 18-bit address that is multiplexed out using the CAE and RAL strobes as required. During a transfer cycle the transfer address is output on these pins during RAL high to low transition.
RAL	Output	The Row Address strobe indicates a valid row address or transfer address is present on the RA-bus. RAL is also used for cas before ras refresh cycles. This is a low true signal.
CAE[0-1]	Output	The Column Address Enables indicate that a valid column address will be present on the next ICLK low to high transition. Bank 0 is addressed by CAE[0] and bank 1 is addressed by CAE[1]. This is a positive true signal. The CAS signal for the VDRAMs must be generated by this signal delayed through a D flipflop clocked with ICLK.
WL[0-15]	Output	The Write Enable pins are low true signals that individually enable writing for each video RAM. The VDRAM Delayed write operation is used.
VD[0-15]	I/O	The Video Data pins transfer pixel data to and from the Video Memory four pixels at a time.

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Pin Description (continued)

OMEGA-MCU Signals for Z-bus		
Signal	Direction	Description
SRL	Input	The Synchronous Reset pin is a low true input signal used to reset the MCU. All MCUs controlled by one GPU must get the same reset synchronized with the system clock.
ZADR	Input	The ZADR pin is used to indicate the start of a Z bus cycle. The ZADR signal will be present for two ICLK cycles, the Z bus address will be valid on the rising edge of the second ICLK.
SYNC	Input	The bus SYNC pin is used to synchronize the Z-bus slaves with the GPU. Z-bus data is accepted by the MCU(read) or the GPU(write) on the positive edge of the system clock while SYNC is high.
ZD[0-15]	I/O	The 16 Z-bus Data pins transfer the read/write mode, the register address and then the register data over the Z-bus to (or from) the MCU.
ZRDY	Output	The Z-bus ReaDY pin is either driven by the MCU when it is ready to accept data on a write or after data has been valid two ICLK cycles on a read. At the next clock cycle after ZRDY, the GPU will assert SYNC to terminate the Z-bus cycle if all of the GPU internal processing is complete. The MCU will use ZRDY to hold off execution when waiting for memory operations to complete.
SLCC	Output	The SLave Condition Code pin is driven by the MCU if selected. Internal MCU registers select the condition that enables this open drain output true. SLCC may be driven by Raster-Op Compare, or Bresenham Processor busy.
SELL	Output	The Select output is a negative true signal that indicates this MCU is the selected Z-bus Slave. This signal is used to enable buffers if the Z-bus must be expanded.
CN[0-2]	Input	The Chip Number inputs are used to encode the Z-bus address of this MCU.
HW[0-7]	Input	The Hardware Command Inputs are used to command MCU internal operations. Please see the Z-bus Command description for the detail on each of these inputs.

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Pin Description (continued)

OMEGA-MCU Signals for the Host Interface		
Signal	Direction	Description
HRQ	Input	The Host Request pin is the initial signal used by the host to request a memory cycle in the Video Memory. All MCUs on a common GPU must receive this signal, and it must be synchronized to the system clock.
CSL	Input	The Chip Select pin is used to select which of the MCUs in a system the host wishes to address. The signal is low true.
HRD	Input	The Host Read pin is driven by the host to select either a read (high) or write operation to video memory.
H16	Input	The Host 16 input when true tells the MCU to do 16-bit data operations for the host.
IOP	Input	The I/O Page enable input tells the MCU that the current host read or write operation must occur in the Host I/O Page of Video Memory. This I/O operation is used by hosts that require emulation of a number of I/O mapped registers.
PIXM	Input	The PIXel Mode signal when true at HRQ causes the MCU to operate only on four bits of the host data. If the chip number of the MCU is even the pixel will transfer on HD[0-3] and if the number is odd HD[4-7]. In either case the unused data lines are high impedance.
HASL	Output	The High Address Strobe is a negative true signal that should enable bits 16-23 of the Host Address onto the Host Data (HD) bus for the current memory operation.
MASL	Output	The Middle Address Strobe is a negative true signal that should enable bits 8-15 of the Host Address onto the Host Data (HD) bus for the current memory operation.
LASL	Output	The Lower Address Strobe is a negative true signal that should enable bits 0-7 of the Host Address onto the Host Data (HD) bus for the current memory or I/O operation.
LDSL	Output	The Lower Data Strobe is a negative true signal that should enable the lower 8-bits of data from the Host onto the Host Data (HD) bus on a write or latches the lower 8 data bits on a read.
HDSL	Output	The High Data Strobe is a negative true signal used when 16-bit mode is enabled (H16 pin). HDSL either enables the higher 8 bits of data from the host onto the Host Data (HD) bus on a write or latches the higher 8 data bits on a read.
HD[0-7]	I/O	The 8 Host Data pins are used to transfer address and data between Video Memory and the Host.
RDY	Output	The ReaDY pin returns a signal to the host when the current host operation is complete.

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Pin Description (continued)

OMEGA-MCU Clock Signal		
Signal	Direction	Description
ICLK	Input	The Input CLocK pin is used to input the basic system clock. Most operations internal and external to the MCU occur on the positive transition of ICLK.

OMEGA-MCU Pixel ALU Signals		
Signal	Direction	Description
PNEG	I/O	The Pixel NEGative pin is driven high by the most significant MCU (register programmed) if the most significant bit of the pixel ALU is high. All of the MCU chips use this pin as an input to see if a Raster-Op Compare is less than zero.
PCO	Output	The Pixel Carry Out pin transmits the pixel ALU carry to the next most significant MCU carry-in.
ZERO	I/O	The Zero pin is high impedance if the current output of the MCU pixel ALU is zero. All of the MCU chips use this wired or signal as an input to test if a raster-op compare is equal to zero. This signal must be pulled-up with an external resistor.
PCI	Input	The Pixel Carry In input passes the carry of the previous MCU into this MCU.

OMEGA-MCU Video Output Interface		
Signal	Direction	Description
BLKL	Input	The BLanKing input signals the MCU when the video display is blanked. The MCU uses this information to determine when to update the internal screen refresh Y counter. The BLKL signal is low true.
FLD	Input	The Field input is used when using a interlaced display to signal the MCU to display the even Field.
HSL	Input	The Horizontal Sync input signals the MCU when horizontal sync is occurring. If programmed for external hsync the MCU will do transfer and then a programmed number of refresh cycles. HSL is low true.
VSL	Input	The Vertical Sync input signals the MCU when vertical sync is occurring. The internal display row counters are reset during vertical sync. VSL is low true.

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