

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH LATCH

FEATURES

- Wide analog input voltage range: $\pm 5\text{ V}$
- Low "ON" resistance:
 $80\ \Omega$ (typ.) at $V_{CC} - V_{EE} = 4.5\text{ V}$
 $70\ \Omega$ (typ.) at $V_{CC} - V_{EE} = 6.0\text{ V}$
 $60\ \Omega$ (typ.) at $V_{CC} - V_{EE} = 9.0\text{ V}$
- Logic level translation:
to enable 5 V logic to communicate
with $\pm 5\text{ V}$ analog signals
- Typical "break before make" built in
- Address latches provided
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4352 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4352 are dual 4-channel analog multiplexers/demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (nY_0 to nY_3) and a common input/output (nZ).

The common channel select logics include two select inputs (S_0 and S_1), an active LOW enable input ($\bar{E}_1$), an active HIGH enable input (E_2) and a latch enable input ($\bar{LE}$).

With $\bar{E}_1$ LOW and E_2 HIGH, one of the four switches is selected (low impedance ON-state) by S_0 and S_1 . The data at the select inputs may be latched by using the active LOW latch enable input ($\bar{LE}$). When $\bar{LE}$ is HIGH, the latch is transparent. When either of the two enable inputs, $\bar{E}_1$ (active LOW) and E_2 (active HIGH), is inactive, all analog switches are turned off.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/t_{PZL}	turn "ON" time $\bar{E}_1, E_2$ or S_n to V_{OS}	$C_L = 15\text{ pF}$ $R_L = 1\text{ k}\Omega$ $V_{CC} = 5\text{ V}$	31	33	ns
t_{PHZ}/t_{PLZ}	turn "OFF" time $\bar{E}_1, E_2$ or S_n to V_{OS}		20	20	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	55	55	pF
C_S	max. switch capacitance independent (Y) common (Z)		5 12	5 12	pF pF

$V_{EE} = \text{GND} = 0\text{ V}$; $T_{\text{amb}} = 25\text{ }^\circ\text{C}$; $t_r = t_f = 6\text{ ns}$

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz
 f_o = output frequency in MHz
 $\sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs
 C_L = output load capacitance in pF
 C_S = max. switch capacitance in pF
 V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND}$ to V_{CC}
For HCT the condition is $V_I = \text{GND}$ to $V_{CC} - 1.5\text{ V}$

PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).
20-lead mini-pack; plastic (SO20; SOT163A).

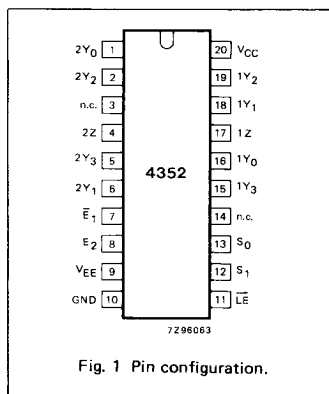


Fig. 1 Pin configuration.

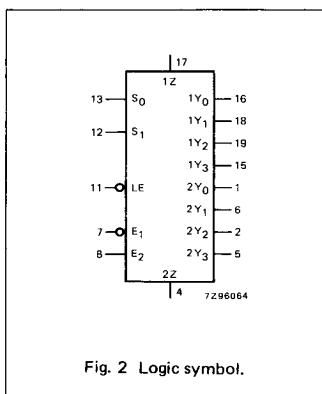


Fig. 2 Logic symbol.

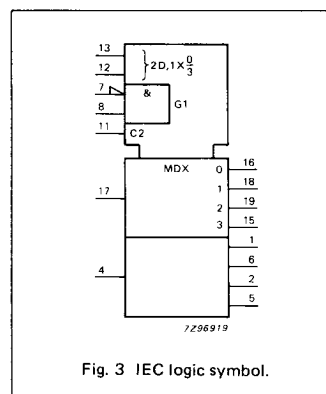


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 6, 2, 5	2Y ₀ to 2Y ₃	independent inputs/outputs
3, 14	n.c.	not connected
7	$\overline{E}_1$	enable input (active LOW)
8	E ₂	enable input (active HIGH)
9	V _{EE}	negative supply voltage
10	GND	ground (0 V)
11	$\overline{LE}$	latch enable input (active LOW)
13, 12	S ₀ , S ₁	select inputs
16, 18, 19, 15	1Y ₀ to 1Y ₃	independent inputs/outputs
17, 4	1Z, 2Z	common inputs/outputs
20	V _{CC}	positive supply voltage

GENERAL DESCRIPTION

V_{CC} and GND are the supply voltage pins for the digital control inputs (S₀, S₁, $\overline{LE}$, E₁ and E₂). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY₀ to nY₃, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. V_{CC} - V_{EE} may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

FUNCTION TABLE

INPUTS					CHANNEL ON
E ₁	E ₂	$\overline{LE}$	S ₁	S ₀	
H	X	X	X	X	none
X	L	X	X	X	none
L	H	H	L	L	nY ₀ - nZ
L	H	H	L	H	nY ₁ - nZ
L	H	H	H	L	nY ₂ - nZ
L	H	H	H	H	nY ₃ - nZ
L	H	L	X	X	*
X	X	↓	X	X	**

H = HIGH voltage level

L = LOW voltage level

X = don't care

↓ = HIGH-to-LOW $\overline{LE}$ transition

* Last selected channel "ON".

** Selected channels latched.

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

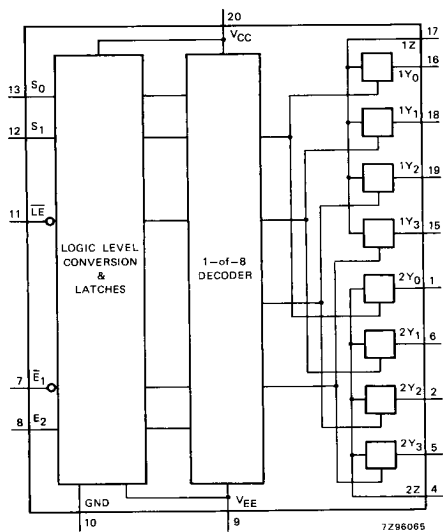


Fig. 4 Functional diagram.

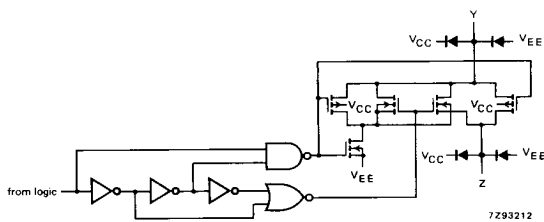


Fig. 5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to $V_{EE} = \text{GND}$ (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
$\pm I_S$	DC switch current		25	mA	for $-0.5 \text{ V} < V_S < V_{CC} + 0.5 \text{ V}$
$\pm I_{EE}$	DC V_{EE} current		20	mA	
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	-65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 6 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminals nZ, when switch current flows in terminals nY_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no V_{CC} current will flow out of terminals nY_n. In this case there is no limit for the voltage drop across the switch, but the voltages at nY_n and nZ may not exceed V_{CC} or V_{EE} .

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage $V_{CC}-\text{GND}$	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V_{CC}	DC supply voltage $V_{CC}-V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ $V_{CC} = 10.0 \text{ V}$

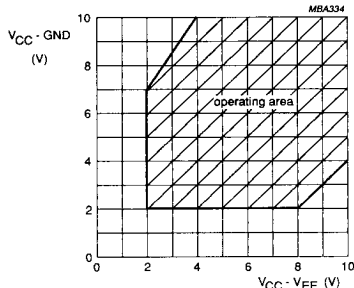


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4352.

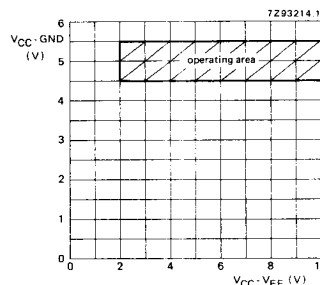


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4352.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: $V_{CC} - GND$ or $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$ and 9.0 V

For 74HCT: $V_{CC} - GND = 4.5$ and 5.5 V; $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$ and 9.0 V

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS					
		74HC/HCT							V _{CC} V	V _{EE} V	I _S μA	V _{is}	V _I	
		+25			−40 to +85		−40 to +125							
		min.	typ.	max.	min.	max.	min.							max.
R _{ON}	ON resistance (peak)		—	—		—		—	Ω	2.0	0	100	V _{CC} to V _{EE}	V _{IN} or V _{IL}
			100	180		225		270	Ω	4.5	0	1000		
			90	160		200		240	Ω	6.0	0	1000		
			70	130		165		195	Ω	4.5	−4.5	1000		
R _{ON}	ON resistance (rail)		150	—		—		—	Ω	2.0	0	100	V _{EE}	V _{IH} or V _{IL}
			80	140		175		210	Ω	4.5	0	1000		
			70	120		150		180	Ω	6.0	0	1000		
			60	105		130		160	Ω	4.5	−4.5	1000		
R _{ON}	ON resistance (rail)		150	—		—		—	Ω	2.0	0	100	V _{CC}	V _{IH} or V _{IL}
			90	160		200		240	Ω	4.5	0	1000		
			80	140		175		210	Ω	6.0	0	1000		
			65	120		150		180	Ω	4.5	−4.5	1000		
ΔR _{ON}	maximum ΔON resistance between any two channels		—						Ω	2.0	0		V _{CC} to V _{EE}	V _{IH} or V _{IL}
			9						Ω	4.5	0			
			8						Ω	6.0	0			
			6						Ω	4.5	−4.5			

Notes to DC characteristics

- At supply voltages ($V_{CC} - V_{EE}$) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring R_{ON} see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS			
		74HC									V _{CC} V	V _{EE} V	V _I	OTHER
		+25			−40 to +85		−40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
V _{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0				
V _{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0				
±I _I	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V _{CC} or GND		
±I _S	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} − V _{EE} (see Fig. 10)	
±I _S	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} − V _{EE} (see Fig. 10)	
±I _S	analog switch ON-state current			0.2		2.0		2.0	μA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} − V _{EE} (see Fig. 11)	
I _{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V _{CC} or GND	V _{IS} = V _{EE} or V _{CC} ; V _{OS} = V _{CC} or V _{EE}	

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS		
		74HC									V _{CC} V	V _{EE} V	OTHER
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
t _{PHL} / t _{PLH}	propagation delay V _{is} to V _{os}		17 6 5 5	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = ∞; C _L = 50 pF (see Fig. 18)	
t _{PZH} / t _{PZL}	turn "ON" time E ₁ ; E ₂ to V _{os} LE to V _{os}		99 36 29 25	325 65 55 46		405 81 69 58		490 98 83 69	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 19)	
t _{PZH} / t _{PZL}	turn "ON" time S _n to V _{os}		99 36 29 25	325 65 55 46		405 81 69 58		490 98 80 69	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 19)	
t _{PHZ} / t _{PLZ}	turn "OFF" time E ₁ ; E ₂ to V _{os} LE to V _{os}		58 21 17 21	200 40 34 40		250 50 43 50		300 60 51 60	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 19)	
t _{PHZ} / t _{PLZ}	turn "OFF" time S _n to V _{os}		63 23 18 24	200 40 34 40		250 50 43 50		300 60 51 60	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 19)	
t _{su}	set-up time S _n to LE	90 18 15 18	17 6 5 9		115 23 20 23		135 27 23 27		ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 20)	
t _h	hold time S _n to LE	5 5 5 5	-6 -2 -2 -3		5 5 5 5		5 5 5 5		ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 20)	
t _w	LE minimum pulse width HIGH	80 16 14 16	11 4 3 4		100 20 17 20		120 24 20 24		ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 20)	

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS			
		74HCT								V _{CC} V	V _{EE} V	V _I	OTHER
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V _{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V _{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
±I _I	input leakage current			0.1		1.0		1.0	μA	5.5	0	V _{CC} or GND	
±I _S	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EE} (see Fig. 10)
±I _S	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EE} (see Fig. 10)
±I _S	analog switch ON-state current			0.2		2.0		2.0	μA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EE} (see Fig. 11)
I _{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 -5.0	V _{CC} or GND	V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}
ΔI _{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V _{CC} - 2.1V	other inputs at V _{CC} or GND

Note to HCT types

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
E ₁ , E ₂	0.50
S _n	0.50
LE	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V _{CC} V	V _{EE} V	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay V _{IS} to V _{OS}		6 5	12 8		15 10		18 12	ns	4.5 4.5	0 -4.5	R _L = ∞; C _L = 50 pF (see Fig. 18)
t _{PZH} / t _{PZL}	turn "ON" time E ₁ ; E ₂ to V _{OS} LE to V _{OS}		38 28	65 46		81 58		98 69	ns	4.5 4.5	0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 19)
t _{PZH} / t _{PZL}	turn "ON" time S _N to V _{OS}		38 27	65 46		81 58		98 69	ns	4.5 4.5	0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 19)
t _{PHZ} / t _{PLZ}	turn "OFF" time E ₁ to V _{OS} LE to V _{OS}		20 20	40 40		50 50		60 60	ns	4.5 4.5	0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 19)
t _{PHZ} / t _{PLZ}	turn "OFF" time E ₂ , S _N to V _{OS}		25 25	43 43		54 54		65 65	ns	4.5 4.5	0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 19)
t _{su}	set-up time S _N to LE	16 18	7 9		20 23		24 27		ns	4.5 4.5	0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 20)
t _h	hold time S _N to LE	5 5	-1 -1		5 5		5 5		ns	4.5 4.5	0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 20)
t _w	LE minimum pulse width HIGH	16 16	3 4		20 20		24 24		ns	4.5 4.5	0 -4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig. 20)

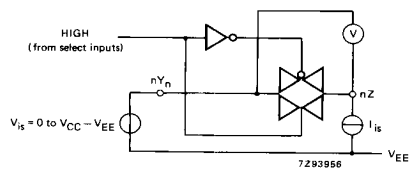
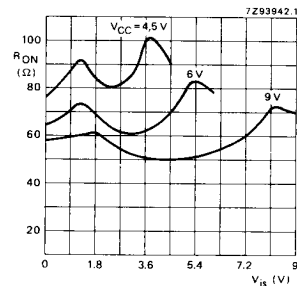
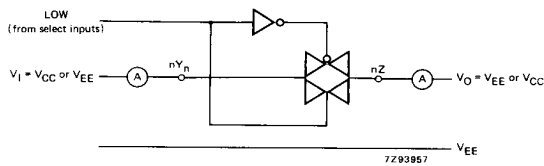
Fig. 8 Test circuit for measuring R_{ON} .Fig. 9 Typical R_{ON} as a function of input voltage V_{is} for $V_{is} = 0$ to $V_{CC} - V_{EE}$.

Fig. 10 Test circuit for measuring OFF-state current.

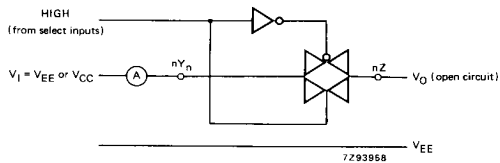


Fig. 11 Test circuit for measuring ON-state current.

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; $T_{amb} = 25^\circ\text{C}$

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} V	V_{EE} V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion $f = 1\text{ kHz}$	0.04 0.02	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ (see Fig. 14)
	sine-wave distortion $f = 10\text{ kHz}$	0.12 0.06	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600\ \Omega$; $C_L = 50\text{ pF}$ $f = 1\text{ MHz}$ (see Figs 12 and 15)
	crosstalk between any two switches/ multiplexers	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600\ \Omega$; $C_L = 50\text{ pF}$; $f = 1\text{ MHz}$ (see Fig. 16)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5		$R_L = 600\ \Omega$; $C_L = 50\text{ pF}$; $f = 1\text{ MHz}$ (E_1 , E_2 or S_n , square-wave between V_{CC} and GND, $t_r = t_f = 6\text{ ns}$) (see Fig. 17)
f_{max}	minimum frequency response (-3dB)	160 170	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	$R_L = 50\ \Omega$; $C_L = 10\text{ pF}$ (see Figs 13 and 14)
C_S	maximum switch capacitance independent (Y) common (Z)	5 12	pF pF				

Notes to AC characteristics

General note

 V_{is} is the input voltage at an nY_n or nZ terminal, whichever is assigned as an input. V_{os} is the output voltage at an nY_n or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

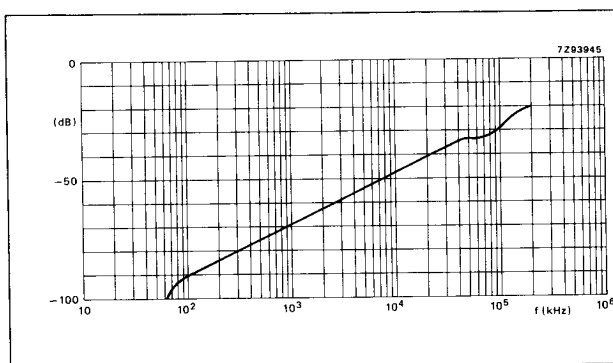
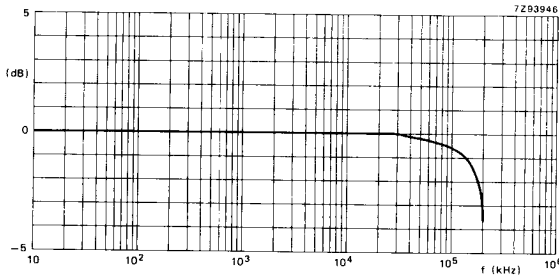


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions:
 $V_{CC} = 4.5 \text{ V}$; $GND = 0 \text{ V}$; $V_{EE} = -4.5 \text{ V}$;
 $R_L = 50 \Omega$; $R_{source} = 1 \text{ k}\Omega$.

Fig. 13 Typical frequency response.

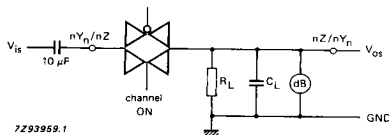


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

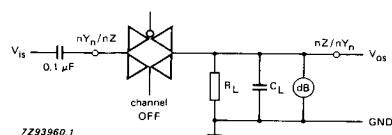


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

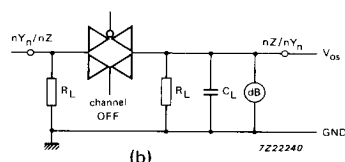
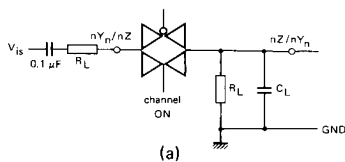


Fig. 16 Test circuits for measuring crosstalk between any two switches/multiplexers.
(a) channel ON condition; (b) channel OFF condition.

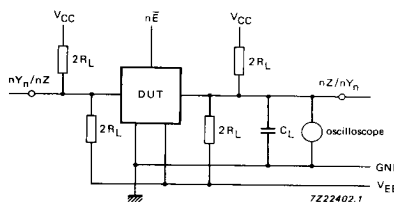
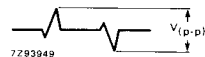


Fig. 17 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 17

The crosstalk is defined as follows
(oscilloscope output):



AC WAVEFORMS

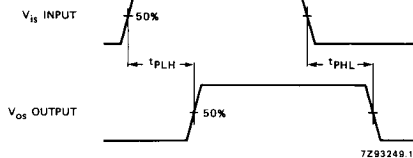


Fig. 18 Waveforms showing the input (V_{1S}) to output (V_{O5}) propagation delays.

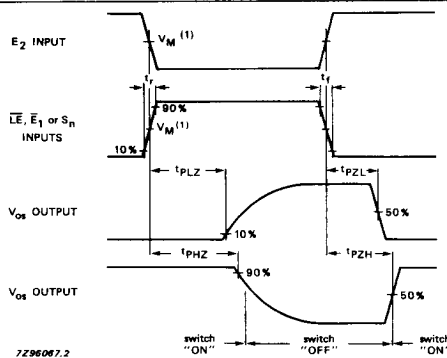


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 19

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

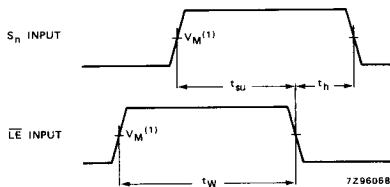


Fig. 20 Waveforms showing the set-up and hold times from S_n inputs to $\overline{LE}$ input, and minimum pulse width of $\overline{LE}$.

Note to Fig. 20

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

TEST CIRCUIT AND WAVEFORMS

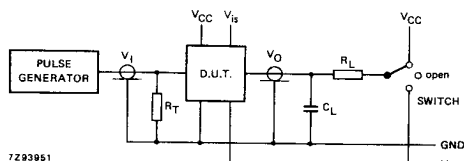


Fig. 21 Test circuit for measuring AC performance.

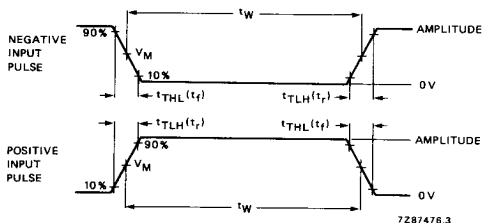


Fig. 22 Input pulse definitions.

Conditions

TEST	SWITCH	V _{is}
t _{pZH}	V _{EE}	V _{CC}
t _{pZL}	V _{CC}	V _{EE}
t _{pHZ}	V _{EE}	V _{CC}
t _{pLZ}	V _{CC}	V _{EE}
others	open	pulse

FAMILY	AMPLITUDE	V _M	t _r ; t _f	
			f _{max} ; PULSE WIDTH	OTHER
74HC	V _{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 21 and 22:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.