

DUAL D-TYPE FLIP-FLOP WITH SET AND RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Output capability: standard
- I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT74 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT74 are dual positive-edge triggered, D-type flip-flops with individual data (D) inputs, clock (CP) inputs, set (S_D) and reset (R_D) inputs; also complementary Q and Q̄ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|--|--|---|----------------|----------------|----------------|
| | | | HC | HCT | |
| t _{PHL} / t _{PLH} | propagation delay n _C P to n _Q , n _{Q̄} n _{SD} to n _Q , n _{Q̄} n _{R_D} to n _Q , n _{Q̄} | C _L = 15 pF V _{CC} = 5 V | 14 15 16 | 15 18 18 | ns ns ns |
| f _{max} | maximum clock frequency | | 76 | 59 | MHz |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| CPD | power dissipation capacitance per flip-flop | notes 1 and 2 | 24 | 29 | pF |

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = CPD \times V_{CC}^2 \times f_1 + \sum (C_L \times V_{CC}^2 \times f_0)$$

f₁ = input frequency in MHz

C_L = output load capacitance in pF

f₀ = output frequency in MHz

V_{CC} = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_0)$ = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}.

For HCT the condition is V_I = GND to V_{CC} - 1.5 V

PACKAGE OUTLINES

14-lead DIL; plastic (SOT27).

14-lead mini-pack; plastic (SO14; SOT108A).

PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---------|-------------------------------------|--|
| 1, 13 | 1̄R _D , 2̄R _D | asynchronous reset-direct input (active LOW) |
| 2, 12 | 1D, 2D | data inputs |
| 3, 11 | 1CP, 2CP | clock input (LOW-to-HIGH, edge-triggered) |
| 4, 10 | 1̄S _D , 2̄S _D | asynchronous set-direct input (active LOW) |
| 5, 9 | 1Q, 2Q | true flip-flop outputs |
| 6, 8 | 1̄Q, 2̄Q | complement flip-flop outputs |
| 7 | GND | ground (0 V) |
| 14 | V _{CC} | positive supply voltage |

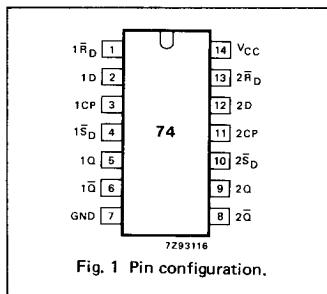


Fig. 1 Pin configuration.

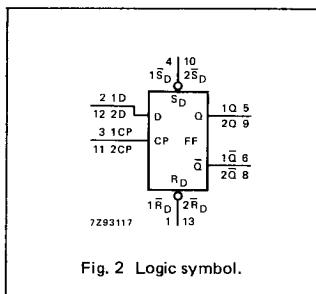


Fig. 2 Logic symbol.

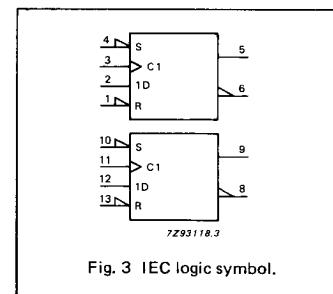


Fig. 3 IEC logic symbol.

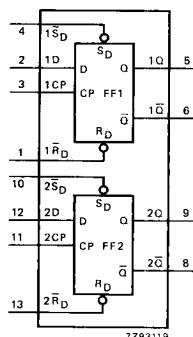


Fig. 4 Functional diagram.

FUNCTION TABLE

| INPUTS | | | OUTPUTS | | |
|-------------|-------------|----|---------|---|-----------|
| \bar{S}_D | \bar{R}_D | CP | D | Q | \bar{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |

| INPUTS | | | OUTPUTS | | |
|-------------|-------------|------------|---------|-----------|-----------------|
| \bar{S}_D | \bar{R}_D | CP | D | Q_{n+1} | \bar{Q}_{n+1} |
| H | H | \uparrow | L | L | H |
| H | H | \uparrow | H | H | L |

H = HIGH voltage level

L = LOW voltage level

X = don't care

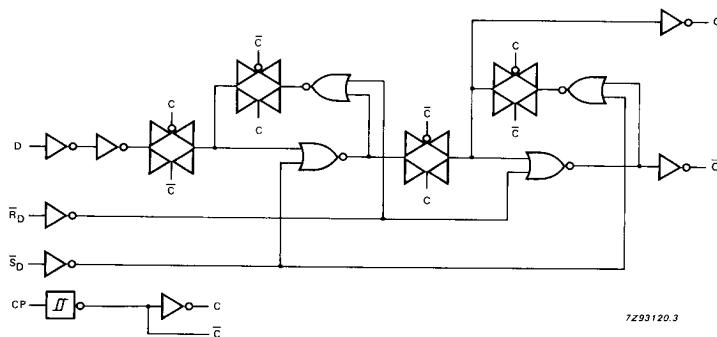
 \uparrow = LOW-to-HIGH CP transition Q_{n+1} = state after the next LOW-to-HIGH CP transition

Fig. 5 Logic diagram (one flip-flop).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | | | | |
|---|---|-----------------------|-----------------|------|-----------------|------|-----------------|------|------|----------------------|-----------|--|--|--|
| | | 74HC | | | | | | | | V _{CC} V | WAVEFORMS | | | |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | | | |
| t _{PHL} / t _{PLH} | propagation delay nCP to nQ, n \bar{Q} | 47 17 14 | 175 35 30 | | 220 44 37 | | 265 53 45 | | ns | 2.0 4.5 6.0 | Fig. 6 | | | |
| t _{PHL} / t _{PLH} | propagation delay n \bar{S}_D to nQ, n \bar{Q} | 50 18 14 | 200 40 34 | | 250 50 43 | | 300 60 51 | | ns | 2.0 4.5 6.0 | Fig. 7 | | | |
| t _{PHL} / t _{PLH} | propagation delay n \bar{R}_D to nQ, n \bar{Q} | 52 19 15 | 200 40 34 | | 250 50 43 | | 300 60 51 | | ns | 2.0 4.5 6.0 | Fig. 7 | | | |
| t _{THL} / t _{T LH} | output transition time | 19 7 6 | 75 15 13 | | 95 19 16 | | 110 22 19 | | ns | 2.0 4.5 6.0 | Fig. 6 | | | |
| t _W | clock pulse width HIGH or LOW | 80 16 14 | 19 7 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig. 6 | | | |
| t _W | set or reset pulse width LOW | 80 16 14 | 19 7 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig. 7 | | | |
| t _{rem} | removal time set or reset | 30 6 5 | 3 1 1 | | 40 8 7 | | 45 9 8 | | ns | 2.0 4.5 6.0 | Fig. 7 | | | |
| t _{su} | set-up time nD to nCP | 60 12 10 | 6 2 2 | | 75 15 13 | | 90 18 15 | | ns | 2.0 4.5 6.0 | Fig. 6 | | | |
| t _h | hold time nCP to nD | 3 3 3 | −6 −2 −2 | | 3 3 3 | | 3 3 3 | | ns | 2.0 4.5 6.0 | Fig. 6 | | | |
| f _{max} | maximum clock pulse frequency | 6.0 30 35 | 23 69 82 | | 4.8 24 28 | | 4.0 20 24 | | MHz | 2.0 4.5 6.0 | Fig. 6 | | | |

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|---------------|-----------------------|
| nD | 0.70 |
| n \bar{R}_D | 0.70 |
| n S_D | 0.80 |
| nCP | 0.80 |

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | | |
|---|---|-----------------------|------|------|------------|------|-------------|------|-------------------|-----------|--------|--|
| | | 74HCT | | | | | | | V _{CC} V | WAVEFORMS | | |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| t _{PHL} / t _{PLH} | propagation delay nCP to nQ, n \bar{Q} | | 18 | 35 | | 44 | | 53 | ns | 4.5 | Fig. 6 | |
| t _{PHL} / t _{PLH} | propagation delay n S_D to nQ, n \bar{Q} | | 23 | 40 | | 50 | | 60 | ns | 4.5 | Fig. 7 | |
| t _{PHL} / t _{PLH} | propagation delay n \bar{R}_D to nQ, n \bar{Q} | | 24 | 40 | | 50 | | 60 | ns | 4.5 | Fig. 7 | |
| t _{THL} / t _{T LH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig. 6 | |
| t _W | clock pulse width HIGH or LOW | 18 | 9 | | 23 | | 27 | | ns | 4.5 | Fig. 6 | |
| t _W | set or reset pulse width LOW | 16 | 9 | | 20 | | 24 | | ns | 4.5 | Fig. 7 | |
| t _{rem} | removal time set or reset | 6 | 1 | | 8 | | 9 | | ns | 4.5 | Fig. 7 | |
| t _{su} | set-up time nD to nCP | 12 | 5 | | 15 | | 18 | | ns | 4.5 | Fig. 6 | |
| t _h | hold time nD to nCP | 3 | −3 | | 3 | | 3 | | ns | 4.5 | Fig. 6 | |
| f _{max} | maximum clock pulse frequency | 27 | 54 | | 22 | | 18 | | MHz | 4.5 | Fig. 6 | |

AC WAVEFORMS

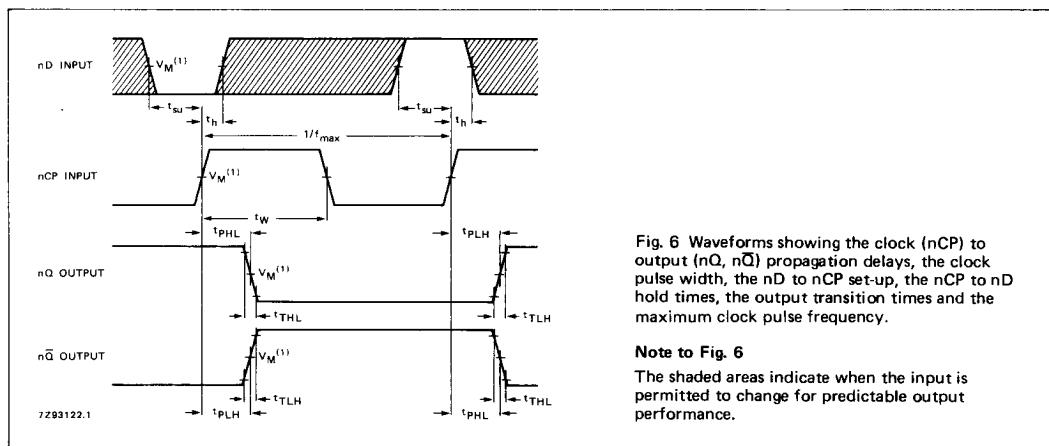


Fig. 6 Waveforms showing the clock (nCP) to output (nQ , $n\bar{Q}$) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

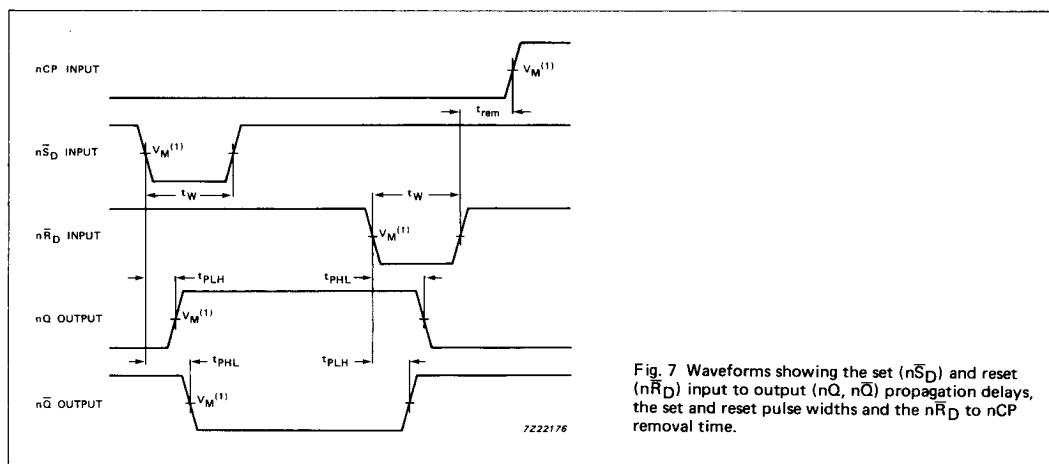


Fig. 7 Waveforms showing the set ($n\bar{S}_D$) and reset ($n\bar{R}_D$) input to output (nQ , $n\bar{Q}$) propagation delays, the set and reset pulse widths and the $n\bar{R}_D$ to nCP removal time.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3V$; $V_I = \text{GND to } 3V$.