

Quad 2-input NAND gate

74LV03

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between $V_{CC} = 2.7V$ and $V_{CC} = 3.6V$
- Typical V_{OLP} (output ground bounce) $< 0.8V$ @ $V_{CC} = 3.3V$, $T_{amb} = 25^{\circ}C$
- Typical V_{OHV} (output V_{OH} undershoot) $> 2V$ @ $V_{CC} = 3.3V$, $T_{amb} = 25^{\circ}C$
- Level shifter capability
- Output capability: standard (open drain)
- I_{CC} category: SSI

QUICK REFERENCE DATA

$GND = 0V$; $T_{amb} = 25^{\circ}C$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZL}/t_{PLZ}	Propagation delay nA, nB to nY	$C_L = 15pF$ $V_{CC} = 3.3V$	8	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	4	pF

NOTES:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacitance in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
- The condition is $V_I = GND$ to V_{CC}
- The given value of C_{PD} is obtained with : $C_L = 0$ pF and $R_L = \infty$

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	$-40^{\circ}C$ to $+125^{\circ}C$	74LV03 N	74LV03 N	SOT27-1
14-Pin Plastic SO	$-40^{\circ}C$ to $+125^{\circ}C$	74LV03 D	74LV03 D	SOT108-1
14-Pin Plastic SSOP Type II	$-40^{\circ}C$ to $+125^{\circ}C$	74LV03 DB	74LV03 DB	SOT337-1
14-Pin Plastic TSSOP Type I	$-40^{\circ}C$ to $+125^{\circ}C$	74LV03 PW	74LV03PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 9, 12	1A to 4A	Data inputs
2, 5, 10, 13	1B to 4B	Data inputs
3, 6, 8, 11	1Y to 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

DESCRIPTION

The 74LV03 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT03.

The 74LV03 provides the 2-input NAND function.

The 74LV03 has open-drain N-transistor outputs, which are not clamped by a diode connected to V_{CC} . In the OFF-state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and V_{Omax} . This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

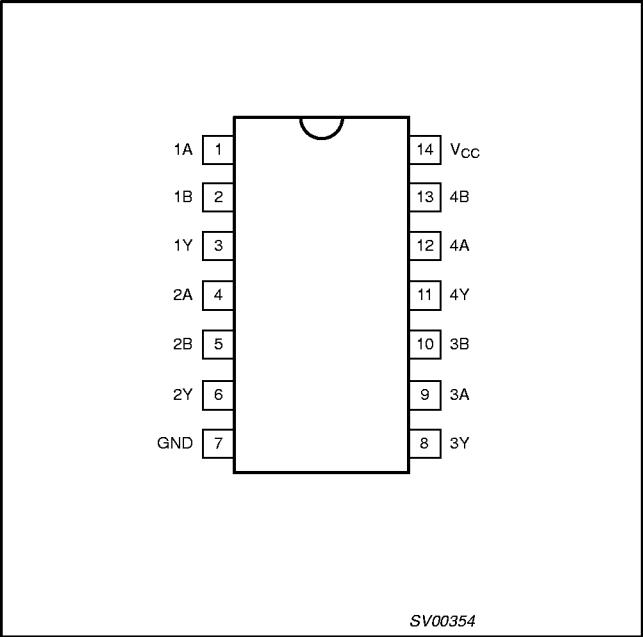
NOTES:

H = HIGH voltage level
 L = LOW voltage level
 Z = High impedance OFF-state

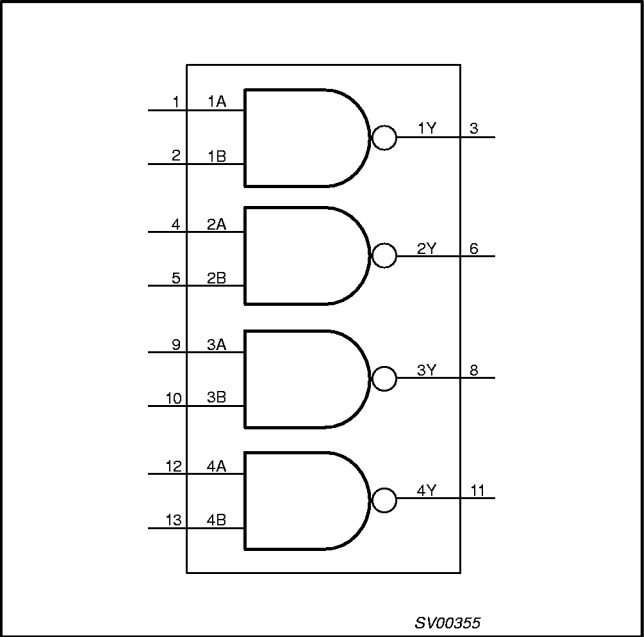
Quad 2-input NAND gate

74LV03

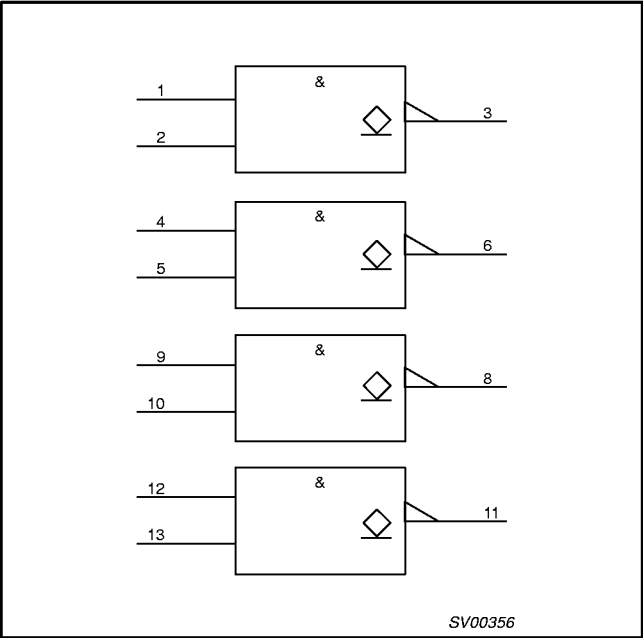
PIN CONFIGURATION



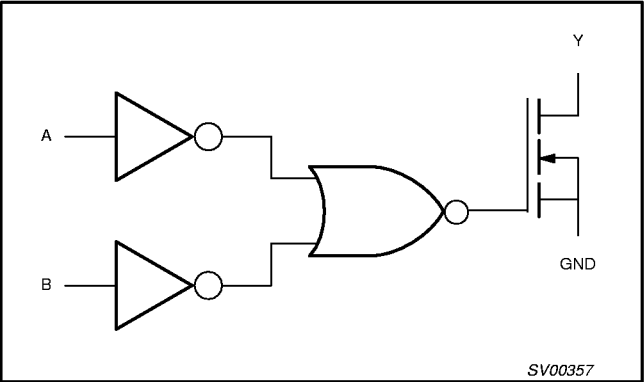
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



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74LV03

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$ $V_{CC} = 3.6V$ to $5.5V$	– – – –	– – – –	500 200 100 50	ns/V

NOTES:

1 The LV is guaranteed to function down to $V_{CC} = 1.0V$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2V$ to $V_{CC} = 5.5V$.

ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND},$ $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Quad 2-input NAND gate

74LV03

DC CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP ¹	MAX	MIN	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	0.9			0.9		V
		V _{CC} = 2.0V	1.4			1.4		
		V _{CC} = 2.7 to 3.6V	2.0			2.0		
		V _{CC} = 4.5 to 5.5V	0.7*V _{CC}			0.7*V _{CC}		
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			0.3		0.3	V
		V _{CC} = 2.0V			0.6		0.6	
		V _{CC} = 2.7 to 3.6V			0.8		0.8	
		V _{CC} = 4.5 to 5.5			0.3*V _{CC}		0.3*V _{CC}	
V _{OH}	HIGH level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA		1.2				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	1.8	2.0		1.8		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	2.5	2.7		2.5		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	2.8	3.0		2.8		
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	4.3	4.5		4.3		
V _{OH}	HIGH level output voltage; STANDARD outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 6mA	2.40	2.82		2.20		V
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; -I _O = 12mA	3.60	4.20		3.50		
V _{OL}	LOW level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
V _{OL}	LOW level output voltage; STANDARD outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.25	0.40		0.50	V
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.35	0.55		0.65	
I _{OZ}	HIGH level output leakage current	V _{CC} = 2.0 to 3.6V; V _I = V _{IL} ; V _O = V _{CC} or GND			5.0		10	µA
I _{OZ}	HIGH level output leakage current	V _{CC} = 2.0 to 3.6V; V _I = V _{IL} ; V _O = 6.0V ²			10		20	µA
I _I	Input leakage current	V _{CC} = 5.5V; V _I = V _{CC} or GND			1.0		1.0	µA
I _{CC}	Quiescent supply current; SSI	V _{CC} = 5.5V; V _I = V _{CC} or GND; I _O = 0			20.0		40	µA
ΔI _{CC}	Additional quiescent supply current per input	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} -0.6V			500		850	µA

NOTES:

- 1 All typical values are measured at $T_{amb} = 25^\circ C$.
- 2 The maximum operating output voltage ($V_{O(max)}$) is 6.0V.

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74LV03

AC CHARACTERISTICS FOR 74LV03

GND = 0V; $t_r = t_f \leq 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 1\text{K}\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS −40 to +85 °C			LIMITS −40 to +125 °C		UNIT
			V _{CC} (V)	MIN	TYP ¹	MAX	MIN	MAX	
t _{PZL} /t _{PLZ}	Propagation delay nA, nB, to nY	Figures, 1, 2	1.2	–	50	–	–	–	ns
			2.0	–	17	26	–	31	
			2.7	–	13	19	–	23	
			3.0 to 3.6	–	10 ²	16	–	19	
			4.5 to 5.5	–	– ³	13	–	16	

- NOTE:**
- 1 Unless otherwise stated, all typical values are at T_{amb} = 25°C.
 - 2 Typical value measured at V_{CC} = 3.3V.
 - 3 Typical value measured at V_{CC} = 5.0V.

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 2.7V ≤ 3.6V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V and ≥ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_X = V_{OL} + 0.3V at V_{CC} ≥ 2.7V and ≤ 3.6V
V_X = V_{OL} + 0.1 * V_{CC} at V_{CC} < 2.7V and ≥ 4.5V

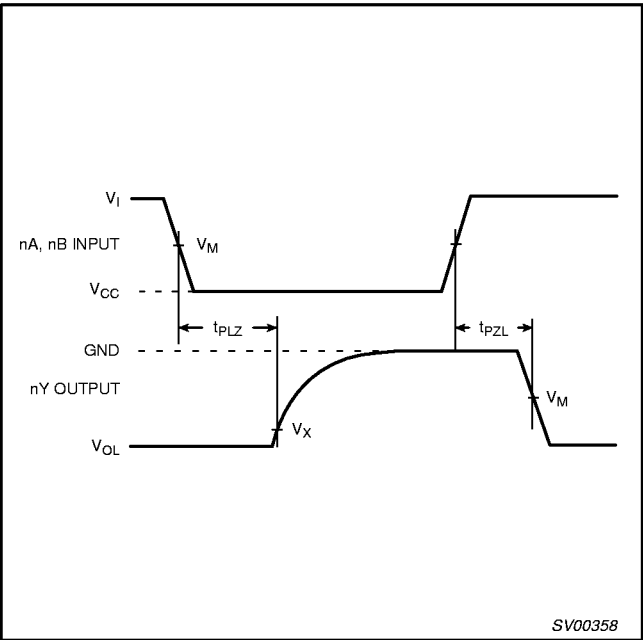


Figure 1. Input (nA, nB) to output (nY) propagation delays.

TEST CIRCUIT

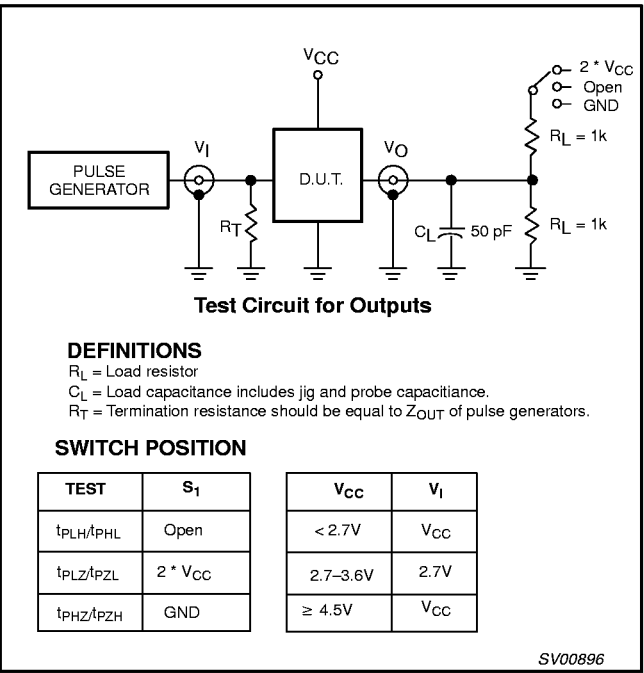


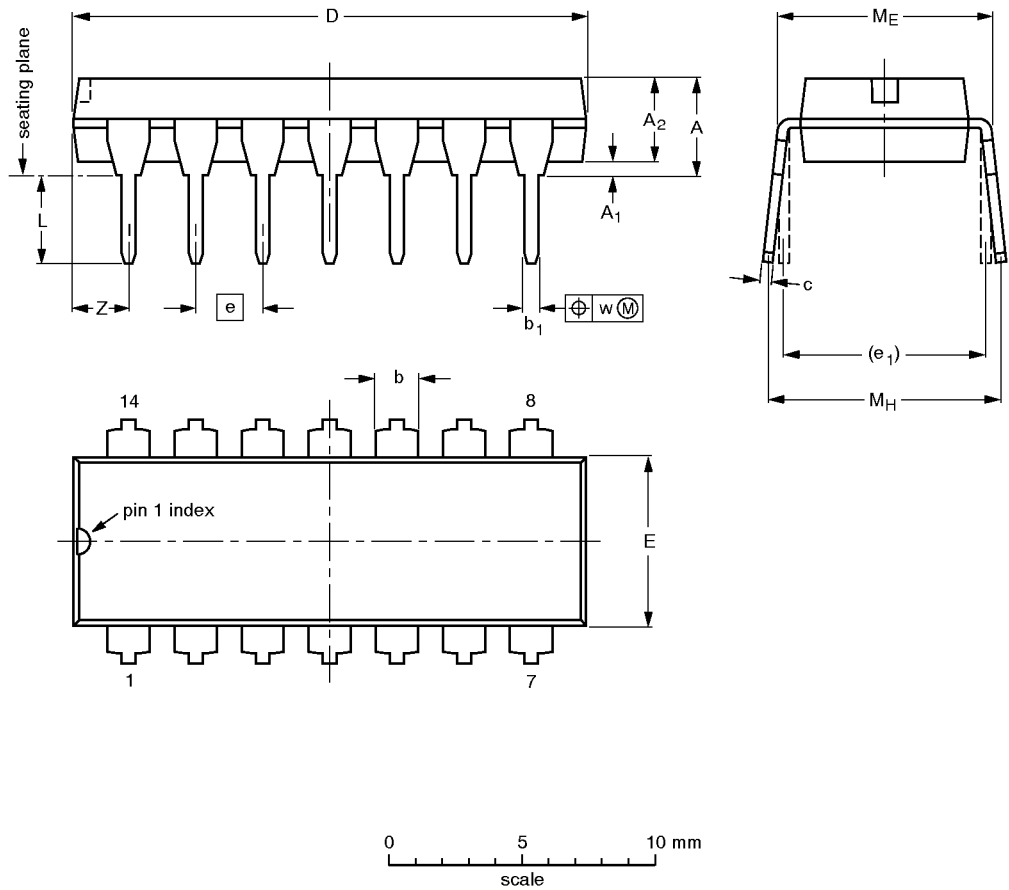
Figure 2. Load circuitry for switching times

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74LV03

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

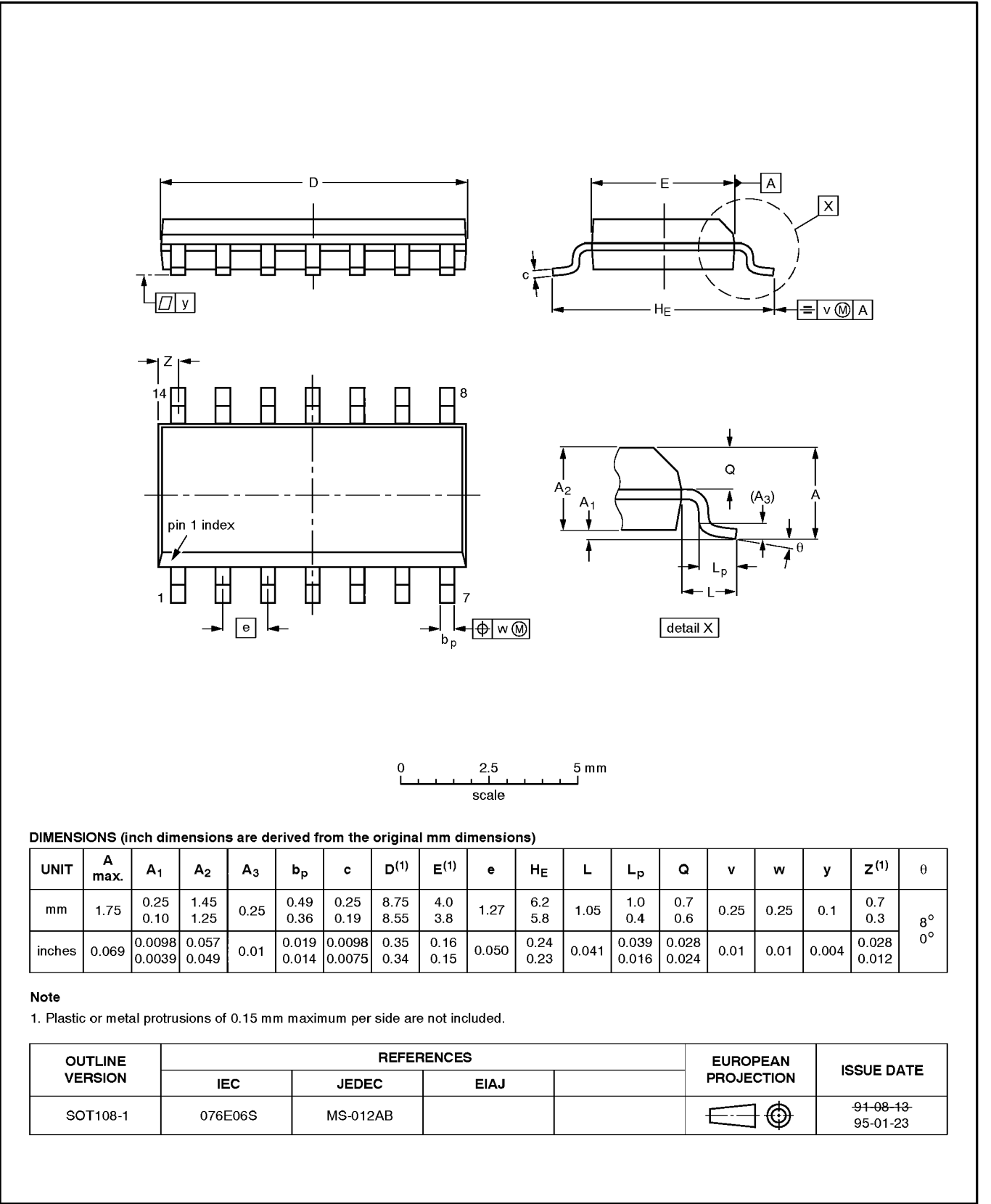
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				92-11-17 95-03-11

Quad 2-input NAND gate

74LV03

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

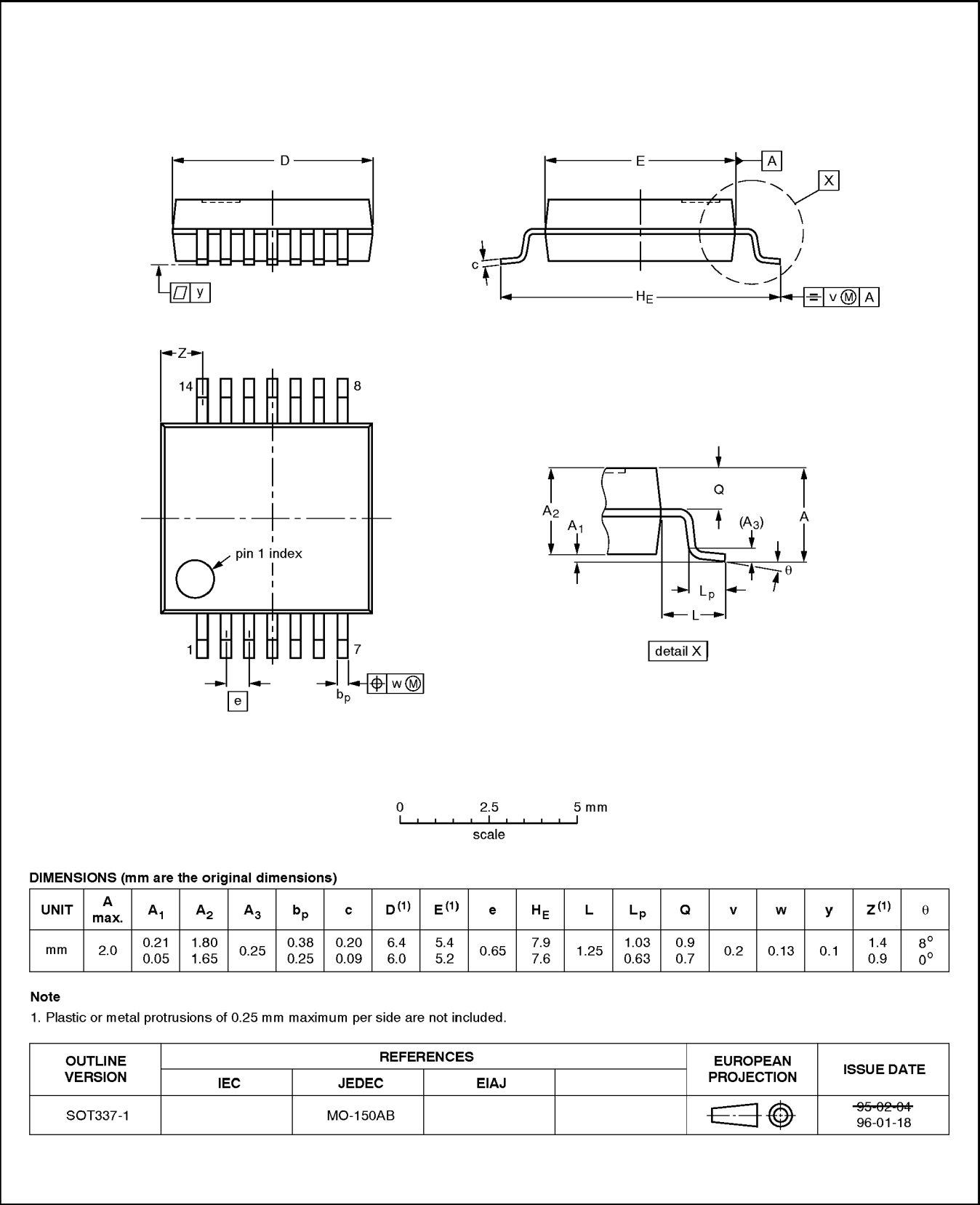


Quad 2-input NAND gate

74LV03

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



Quad 2-input NAND gate

74LV03

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

