

Triple 3-input AND gate

74LV11

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical V_{OLP} (output ground bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_{amb} = 25^{\circ}\text{C}$
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_{amb} = 25^{\circ}\text{C}$
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV11 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT11.

The 74LV11 provides the 3-input AND function.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB, nC to nY	$C_L = 15$ pF; $V_{CC} = 3.3$ V	10	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	See Notes 1 and 2	18	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacitance in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_I = \text{GND to } V_{CC}$.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	-40°C to $+125^{\circ}\text{C}$	74LV11 N	74LV11 N	SOT27-1
14-Pin Plastic SO	-40°C to $+125^{\circ}\text{C}$	74LV11 D	74LV11 D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to $+125^{\circ}\text{C}$	74LV11 DB	74LV11 DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to $+125^{\circ}\text{C}$	74LV11 PW	74LV11PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A – 3A	Data inputs
2, 4, 10	1B – 3B	Data inputs
7	GND	Ground (0 V)
12, 6, 8	1Y – 3Y	Data outputs
13, 5, 11	1C – 3C	Data inputs
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

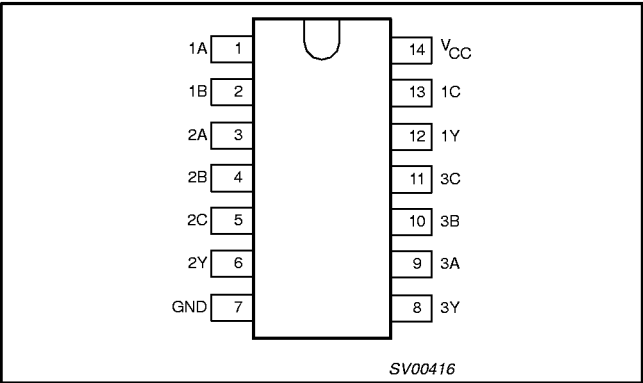
NOTES:

H = HIGH voltage level
L = LOW voltage level

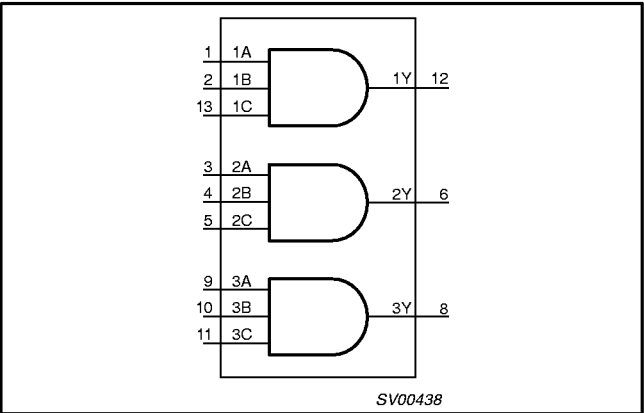
Triple 3-input AND gate

74LV11

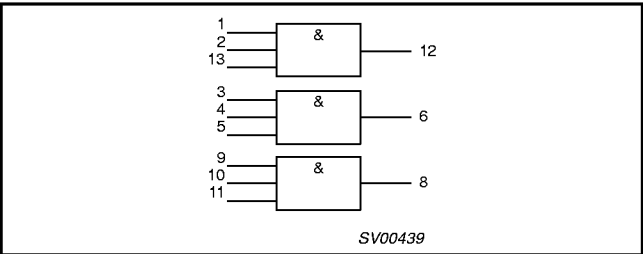
PIN CONFIGURATION



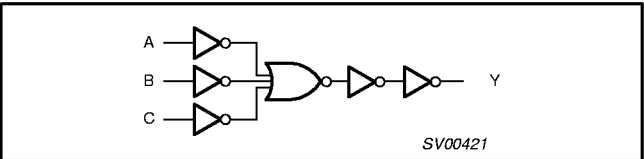
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V _{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V _I	Input voltage		0	–	V _{CC}	V
V _O	Output voltage		0	–	V _{CC}	V
T _{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t _r , t _f	Input rise and fall times	V _{CC} = 1.0V to 2.0V V _{CC} = 2.0V to 2.7V V _{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

Triple 3-input AND gate

74LV11

ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND},$ $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: -40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP ¹	MAX	MIN	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	0.9			0.9		V
		V _{CC} = 2.0V	1.4			1.4		
		V _{CC} = 2.7 to 3.6V	2.0			2.0		
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			0.3		0.3	V
		V _{CC} = 2.0V			0.6		0.6	
		V _{CC} = 2.7 to 3.6V			0.8		0.8	
V _{OH}	HIGH level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; -I _O = 100μA		1.2				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100μA	1.8	2.0		1.8		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; -I _O = 100μA	2.5	2.7		2.5		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100μA	2.8	3.0		2.8		
V _{OH}	HIGH level output voltage; STANDARD outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 6mA	2.40	2.82		2.20		V
V _{OL}	LOW level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		0				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		0	0.2		0.2	
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		0	0.2		0.2	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		0	0.2		0.2	
V _{OL}	LOW level output voltage; STANDARD outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.25	0.40		0.50	V
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND			1.0		1.0	μA

Triple 3-input AND gate

74LV11

DC CHARACTERISTICS FOR THE LV FAMILY (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
I _{CC}	Quiescent supply current; SSI	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0			20.0		40	μA
ΔI _{CC}	Additional quiescent supply current per input	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V			500		850	μA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_r = t_f ≤ 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85 °C			−40 to +125 °C		
			V _{CC} (V)	MIN	TYP ¹	MAX	MIN	MAX	
t _{PHL} /PLH	Propagation delay nA, nB, nC to nY	Figures 1, 2	1.2		60				ns
			2.0		20	39		46	
			2.7		15	29		34	
			3.0 to 3.6		11 ²	23		27	

NOTES:

1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C.
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at V_{CC} ≥ 2.7 V

V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

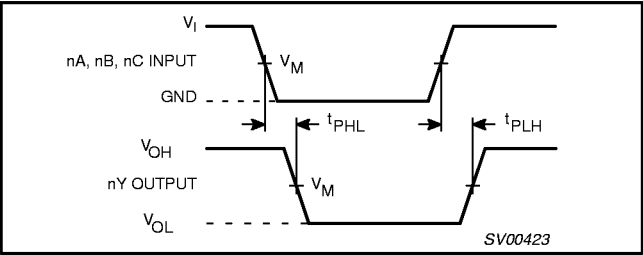


Figure 1. Input (nA, nB, nC) to output (nY) propagation delays.

TEST CIRCUIT

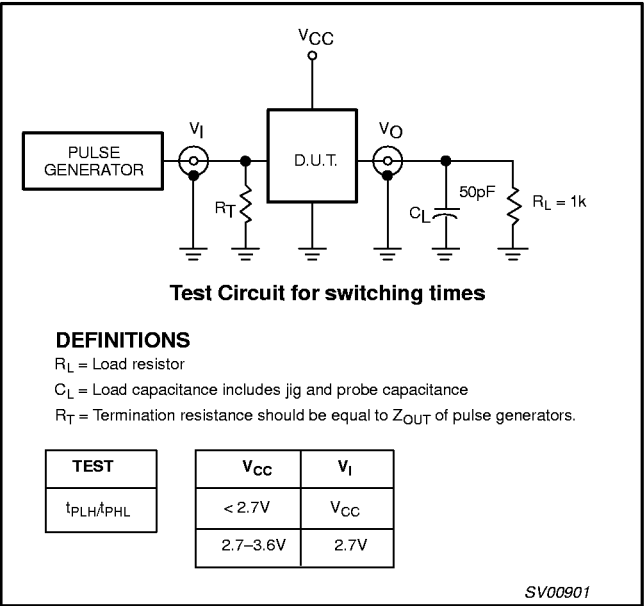


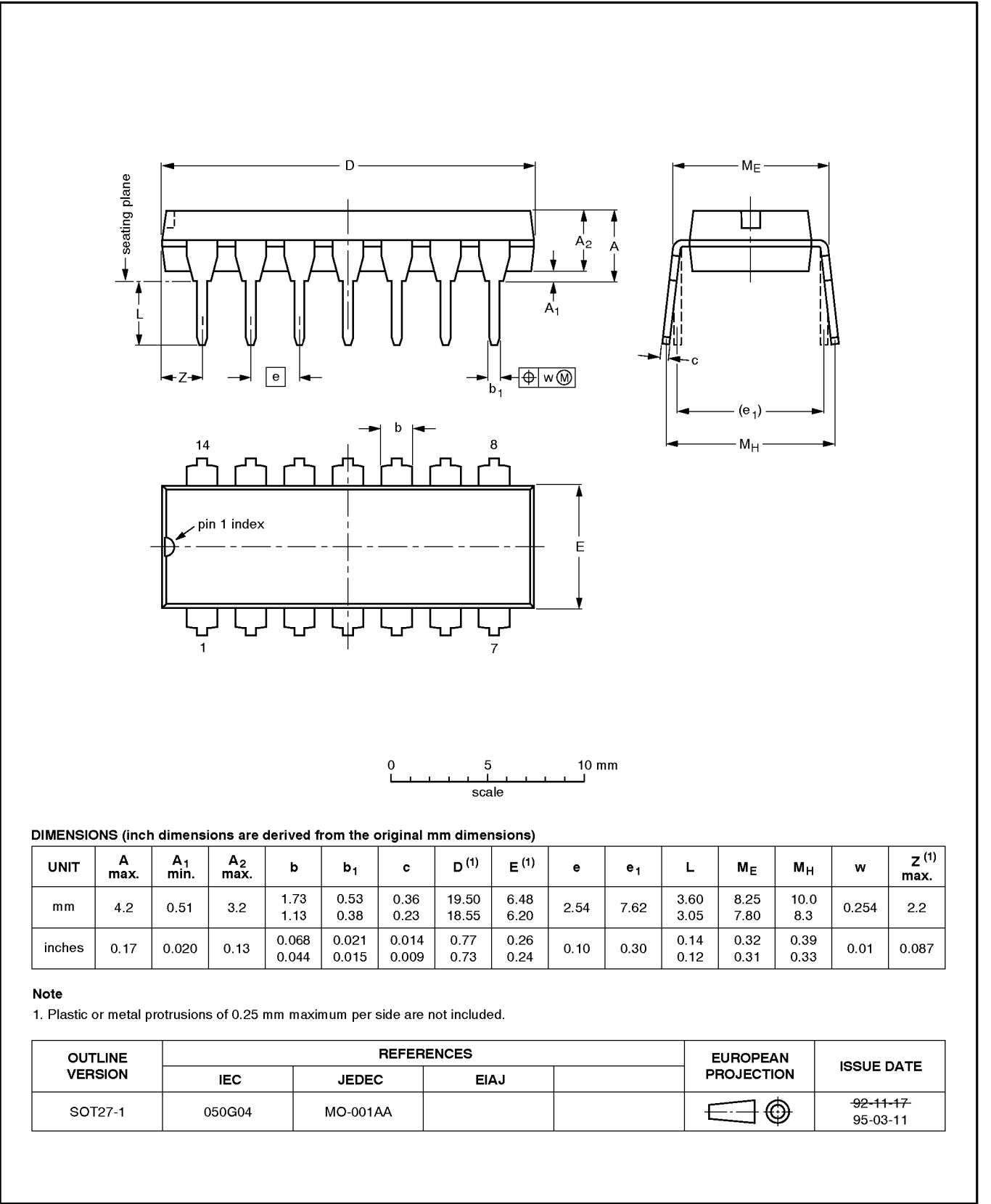
Figure 2. Load circuitry for switching times.

Triple 3-input AND gate

74LV11

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

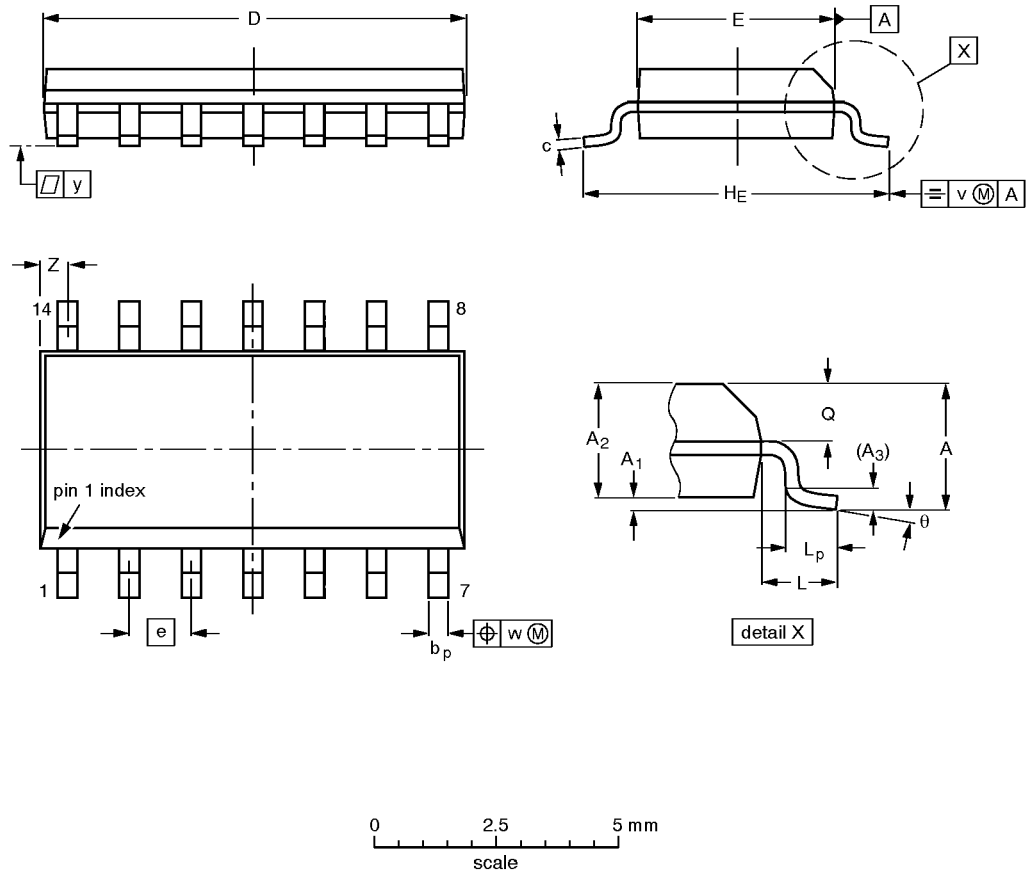


Triple 3-input AND gate

74LV11

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

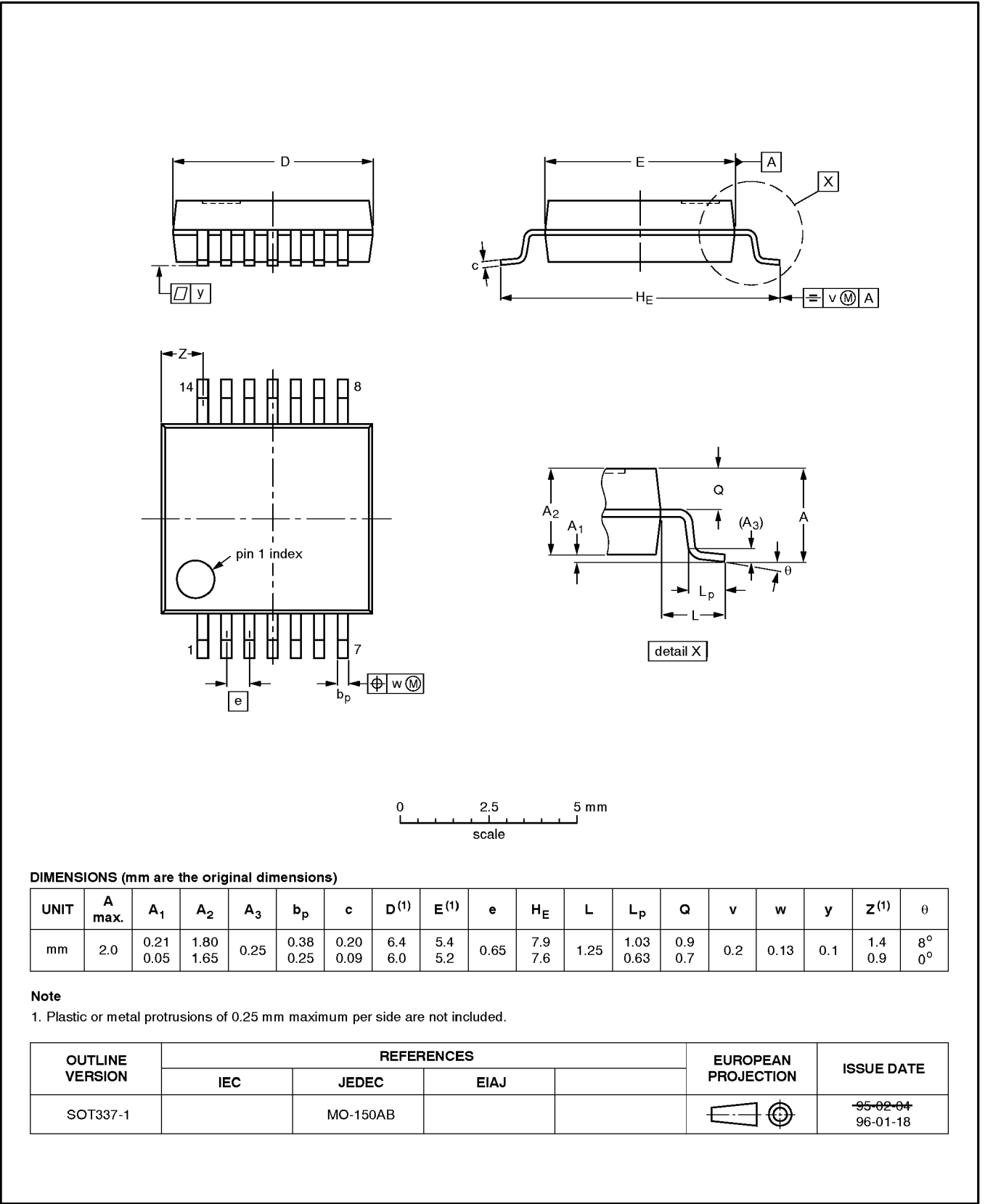
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				91-08-13 95-01-23

Triple 3-input AND gate

74LV11

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

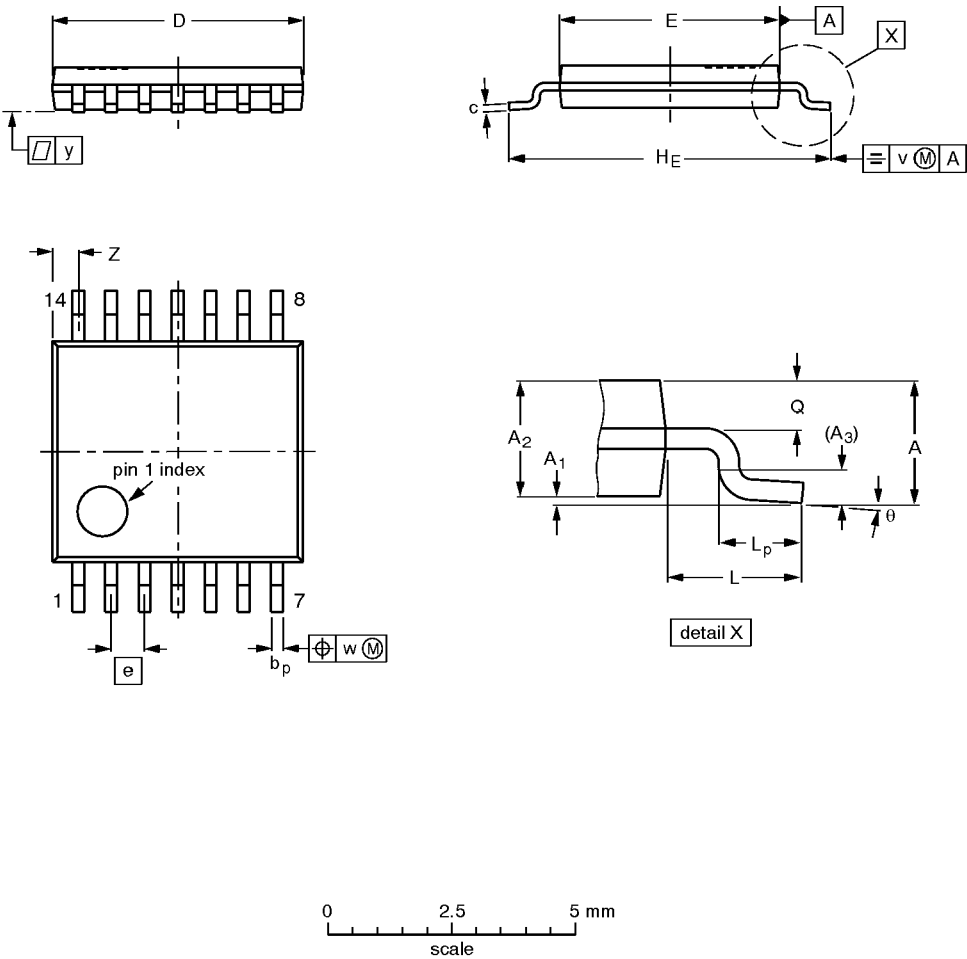


Triple 3-input AND gate

74LV11

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

- Notes
- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 - 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				94-07-12 95-04-04