Presettable synchronous 4-bit binary counter; synchronous reset

74LV163

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV163 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT163.

The 74LV163 is a synchronous presettable binary counter which features an internal look-head carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET). A low level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for $\overline{MR}$ are met).

This action occurs regardless of the levels at $\overline{PE}$, CET and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate. The look ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascading stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{tp_{(max)}\ (CP\ to\ TC) + t_{su}(CEP\ to\ CP)}$$

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n CP to TC CET to TC	C_L = 15 pF; V_{CC} = 3.3 V	 15 18 9	ns
f_{max}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC}[1]	25	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV163 N	74LV163 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV163 D	74LV163 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV163 DB	74LV163 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV163 PW	74LV163PW DH	SOT403-1

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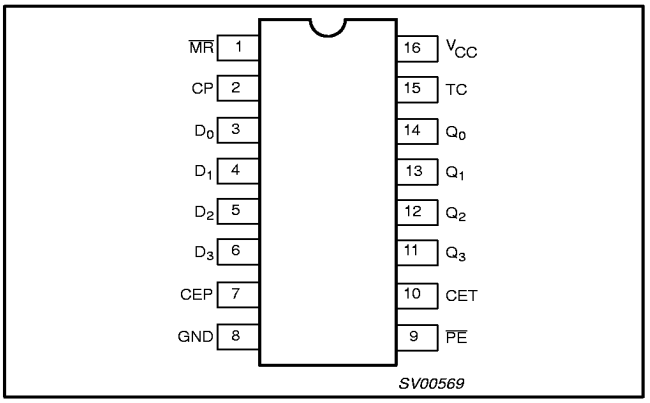
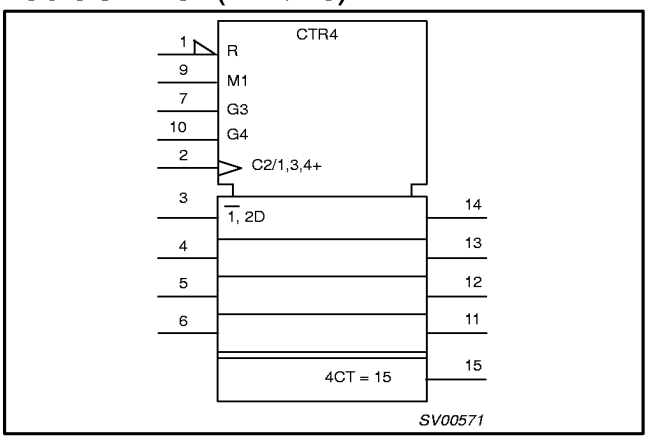
PIN CONFIGURATION



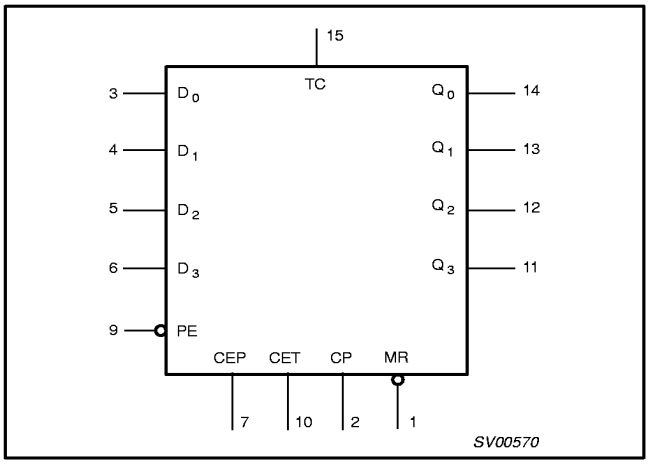
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{MR}$	Asynchronous master reset (active LOW)
2	CP	Clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	Data inputs
7	CEP	Count enable inputs
8	GND	Ground (0 V)
9	$\overline{PE}$	Parallel enable input (active LOW)
10	CET	Count enable carry input
14, 13, 12, 11	Q_0 to Q_3	Flip-flop outputs
15	TC	Terminal count output
16	V_{CC}	Positive supply voltage

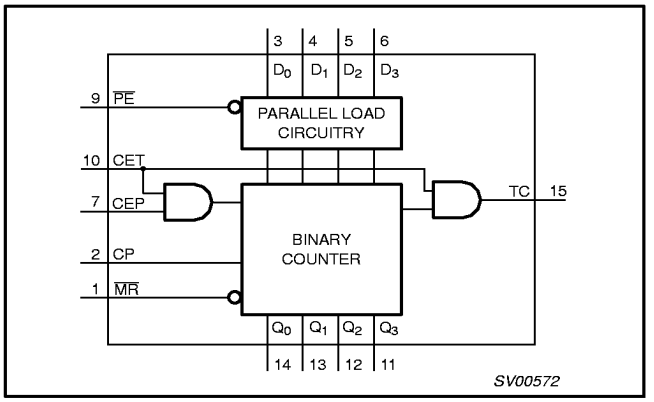
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTIONAL DIAGRAM



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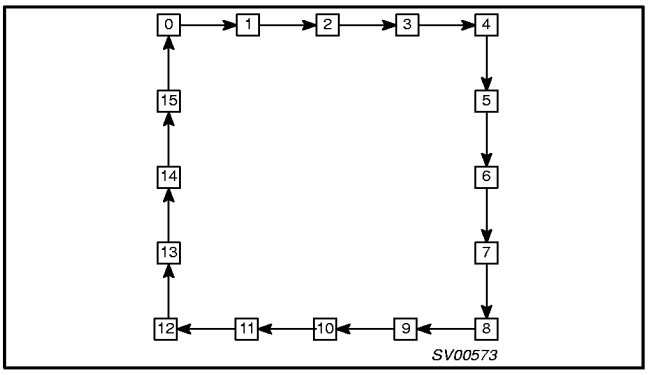
FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
Count	h	↑	h	h	h	X	Count	*
Hold (do nothing)	h	X	l	X	h	X	q_n	*
	h	X	X	l	h	X	q_n	L

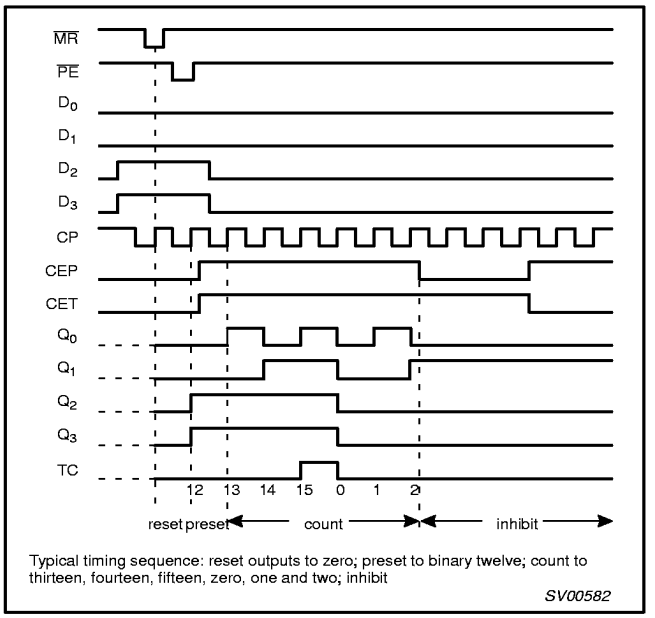
NOTES:

* = The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH)
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition

STATE DIAGRAM



TYPICAL TIMING SEQUENCE



Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit

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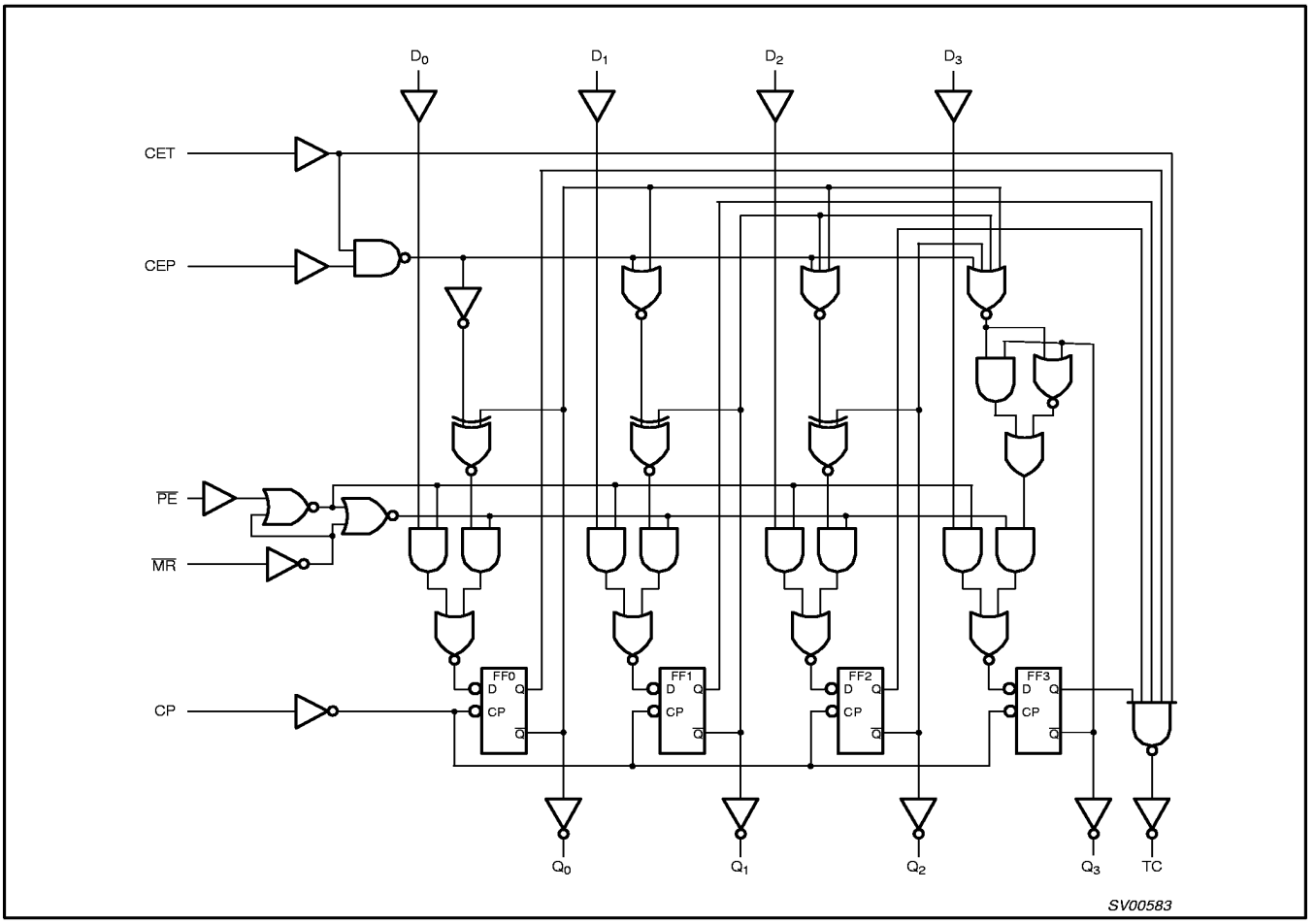
LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

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AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	Figures 1	1.2		95				ns
			2.0		32	61		75	
			2.7		24	45		55	
			3.0 to 3.6		18[2]	36		44	
t_{PHL}/t_{PLH}	Propagation delay CP to $\overline{TC}$	Figures 1	1.2		115				ns
			2.0		39	75		90	
			2.7		29	55		66	
			3.0 to 3.6		22[2]	44		53	
t_{PHL}/t_{PLH}	Propagation delay CET to $\overline{TC}$	Figures 2	1.2		55				ns
			2.0		19	36		44	
			2.7		14	26		33	
			3.0 to 3.6		10[2]	21		26	
t_w	Clock pulse width HIGH or LOW	Figures 1	2.0	34	10		41		ns
			2.7	25	8		30		
			3.0 to 3.6	20	6[2]		24		
t_{su}	Set-up time MR, D_n to CP	Figures 3, 4	1.2		25				ns
			2.0	22	9		26		
			2.7	16	6		19		
			3.0 to 3.6	13	5[2]		15		
t_{su}	Set-up time $\overline{PE}$ to CP	Figures 3	1.2		30				ns
			2.0	22	10		26		
			2.7	16	8		19		
			3.0 to 3.6	13	6[2]		15		
t_{su}	Set-up time CEP, CET to CP	Figures 5	1.2		30				ns
			2.0	22	10		26		
			2.7	16	8		19		
			3.0 to 3.6	13	6[2]		15		
t_h	Hold time D_n, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	Figures 3, 4, 5	1.2		–35				ns
			2.0	0	–12		0		
			2.7	0	–9		0		
			3.0 to 3.6	0	–7		0		
f_{max}	Maximum clock pulse frequency	Figures 1	2.0	14	40		12		MHz
			2.7	19	58		16		
			3.0 to 3.6	24	70		20		

NOTES:

1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

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AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} <$ 2.7 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

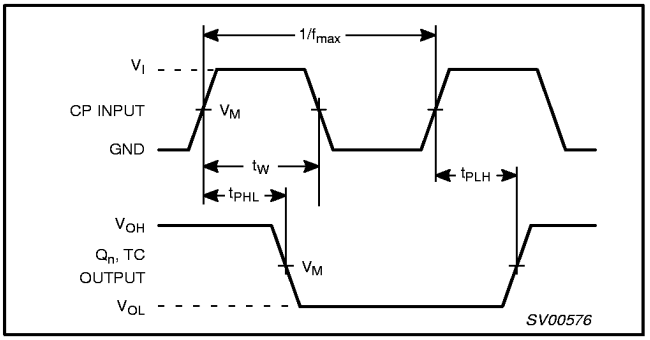


Figure 1. Clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width and the maximum clock frequency.

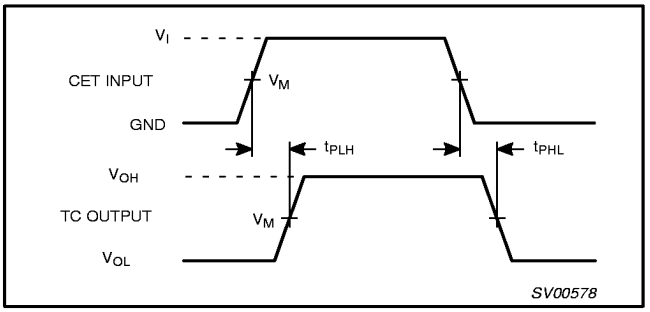


Figure 2. Input (CET) to output (TC) propagation delays and output transition times.

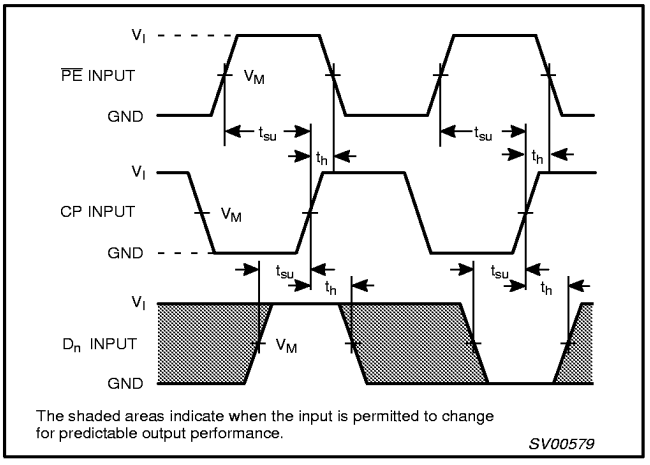


Figure 3. Set-up and hold times for input (D_n) and parallel enable input ($\overline{PE}$).

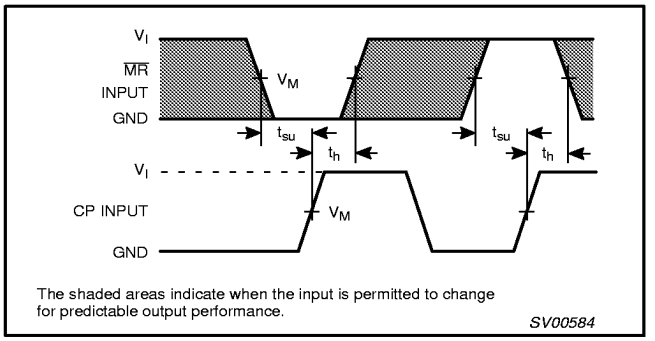


Figure 4. $\overline{MR}$ set-up and hold times.

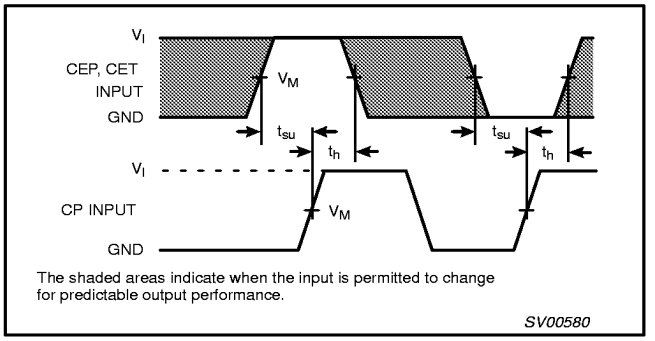
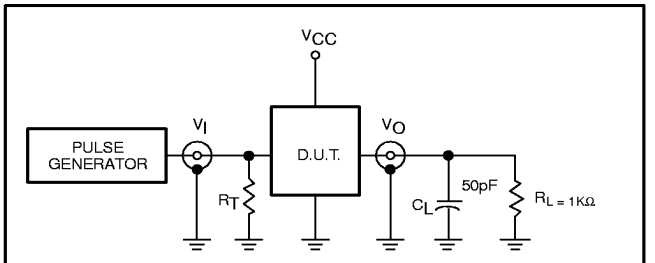


Figure 5. CEP and CET set-up and hold times.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST
t_{PLH}/t_{PHL}

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00901

Figure 6. Load circuitry for switching times.

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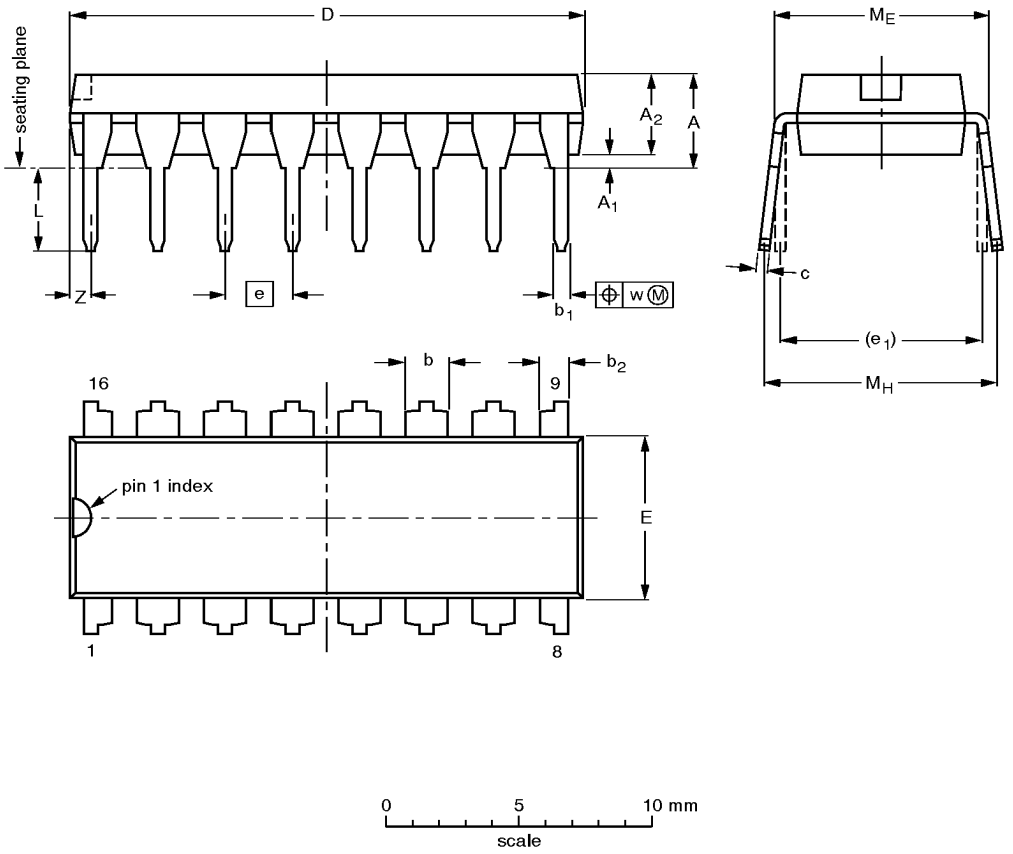
DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

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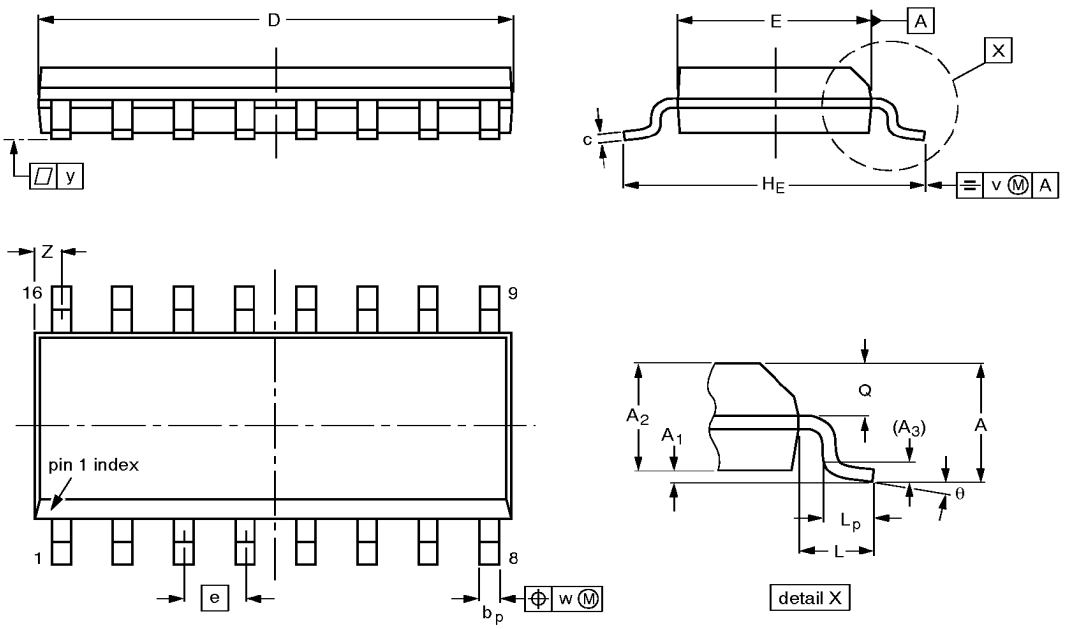
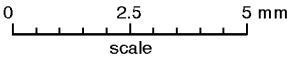
SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

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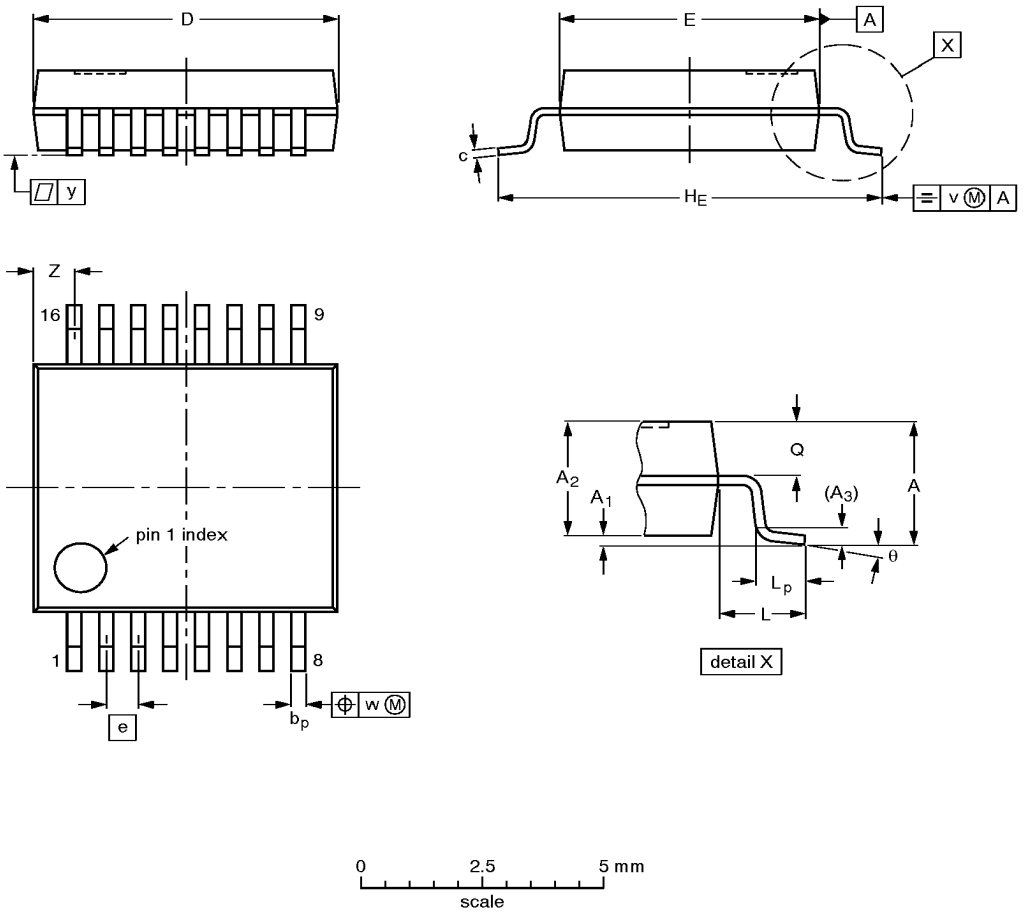
SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

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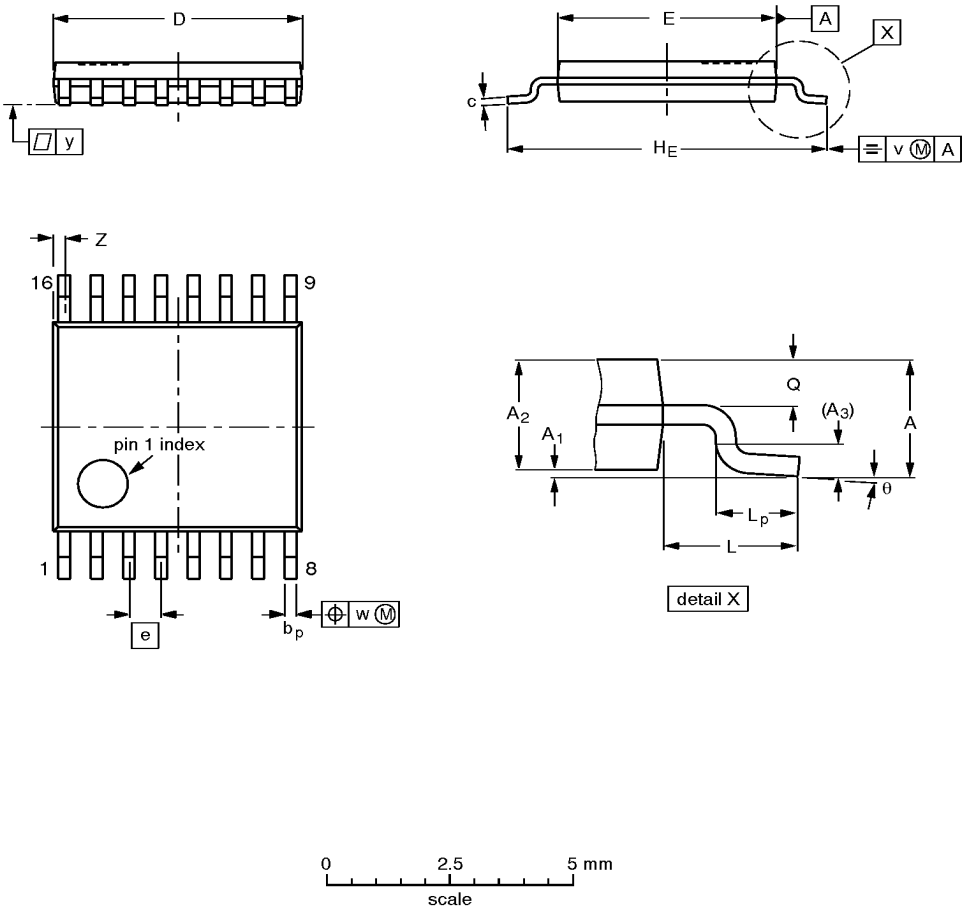
TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

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