calogic
CORPORATION

Ultra-Low Offset Voltage Operational Amplifier

OP-77

FEATURES

- Low V_{OS} ..... 25μV Max.
- Low V_{OS} Drift ..... 0.3μV/°C Max.
- High Gain ..... 5,000,000 Min.
- Fits 725, 108A, 308A, AD510, OP-05, OP-07 & 741 Sockets
- Low Power Consumption ..... 60mW Max.
- High PSRR ..... 110dB Min.
- High CMRR ..... 1μV/V Max.

APPLICATIONS

- High-Stability Instrumentation Amplifiers
- Precision Absolute Value Circuits
- Adjustment-Free Precision Summing Amplifiers

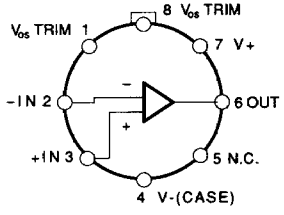
DESCRIPTION

The OP-77 represents a significant improvement in precision operational amplifiers. The low initial V_{OS} drift and exceptional TCV_{OS} of 0.3μV/°C maximum and the low V_{OS} of 25μV maximum, eliminates the need for V_{OS} adjustment. With only 50mW power consumption, 110dB PSRR and 120dB CMRR virtually eliminate errors caused by power supply drifts and common mode signals. These characteristics combined with an impressive open loop gain of 5V/μV minimum and a great linearity, makes the OP-77 ideally suited for precision instrumentation applications.

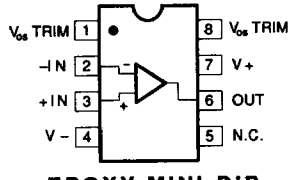
ORDERING INFORMATION

T_A=25°C V_{OS} MAX (μV)	PACKAGE: TO-99 8-PIN	PACKAGE: PLASTIC DIP 8-PIN	PACKAGE: PLASTIC SOIC 8-PIN	OPER. TEMP. RANGE
25	OP77EJ	—	—	IND
25	—	OP77EP	OP77ES	COM
60	OP77FJ	—	—	IND
60	—	OP77FP	OP77FS	COM
100	—	OP77GP	OP77GS	COM

Pin Connections (Top View)



TO-99 (J-Suffix)



EPOXY MINI-DIP (P-Suffix)

8-PIN PLASTIC SOIC (S-Suffix)

OP Amps

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 3) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
J ..... −65°C to +150°C
P and SO Packages ..... −65°C to +125°C
Operating Temperature Range
OP-77A, OP-77B (J) ..... −55°C to +125°C
OP-77E, OP-77F (J) ..... −25°C to +85°C
OP-77E, OP-77F, OP-77G (P or S) ..... 0°C to 70°C
Lead Temperature (Soldering, 60 sec.) ..... 300°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C

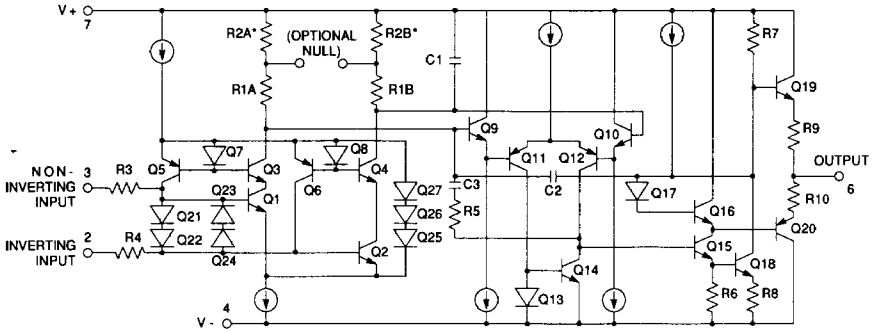
NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C

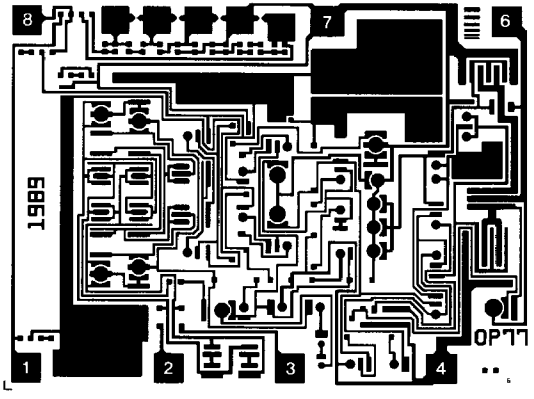
2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Simplified Schematic



*NOTE: R2A AND R2B ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY FOR MINIMUM INPUT OFFSET VOLTAGE.

Die Characteristics



1. TRIM
2. (−) INPUT
3. (+) INPUT
4. V−
6. OUTPUT
7. V+
8. TRIM

DIE SIZE 0.079×0.060 inch, 4740 sq. mils
(2.007×1.524mm, 3.058 sq. mm)

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77A MIN.	OP-77A TYP.	OP-77A MAX.	OP-77B MIN.	OP-77B TYP.	OP-77B MAX.	UNITS
Input Offset Voltage	V_{OS}		—	10	25	—	20	60	μV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)	—	0.2	—	—	0.2	—	mV
Input Offset Current	I_{OS}		—	0.3	1.5	—	0.3	2.8	nA
Input Bias Current	I_B		−0.2	1.2	2.0	−0.2	1.2	2.8	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 2) f_O = 100Hz (Note 2) f_O = 1000Hz (Note 2)	— — —	10.3 10.0 9.6	18.0 13.0 11.0	— — —	10.3 10.0 9.6	18.0 13.0 11.0	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz (Note 2) f_O = 100Hz (Note 2) f_O = 1000Hz (Note 2)	— — —	0.32 0.14 0.12	0.80 0.23 0.17	— — —	0.32 0.14 0.12	0.80 0.23 0.17	pA/√Hz
Input Resistance—Differential-Mode	R_{IN}	(Note 3)	26	45	—	18.5	45	—	MΩ
Input Resistance—Common-Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	—	0.1	1.0	—	0.1	1.6	μV/V
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	—	0.7	3	—	0.7	3	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	5000	12000	—	2000	8000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	— — —	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	— — —	V
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 (Note 2)	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O		—	60	—	—	60	—	Ω
Power Consumption	P_d	V_S = ±15V, No Load V_S = ±3V, No load	— —	50 3.5	60 4.5	— —	50 3.5	60 4.5	mW
Offset Adjustment Range		R_p = 20kΩ	—	±3	—	—	±3	—	mV

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
2. Sample tested.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77E MIN.	OP-77E TYP.	OP-77E MAX.	OP-77F MIN.	OP-77F TYP.	OP-77F MAX.	OP-77G MIN.	OP-77G TYP.	OP-77G MAX.	UNITS
Input Offset Voltage	V_{OS}		—	10	25	—	20	60	—	50	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 1)	—	0.3	—	—	0.4	—	—	0.4	—	μV/Mo
Input Offset Current	I_{OS}		—	0.3	1.5	—	0.3	2.8	—	0.3	2.8	nA
Input Bias Current	I_B		−0.2	1.2	2.0	−0.2	1.2	2.8	−0.2	1.2	2.8	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 2)	—	10.0	13.0	—	10.2	13.5	—	10.3	13.5	
		$f_O = 1000Hz$	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	15	35	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	$pA/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 2)	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		$f_O = 1000Hz$	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance—Differential-Mode	R_{IN}	(Note 3)	26	45	—	18.5	45	—	18.5	45	—	MΩ
Input Resistance—Common-Mode	R_{INCM}		—	200	—	—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	1.6	—	0.1	1.6	μV/V
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.7	3.0	—	0.7	3.0	—	0.7	3.0	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	5000	12000	—	2000	6000	—	2000	6000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±13.5	±14.0	—	±13.5	±14.0	—	±13.5	±14.0	—	V
		$R_L \geq 2k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	±12.5	±13.0	—	
		$R_L \geq 1k\Omega$	±12.0	±12.5	—	±12.0	±12.5	—	±12.0	±12.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$ (Note 2)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O		—	60	—	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	50	60	—	50	60	—	50	60	mW
		$V_S = \pm 3V$, No load	—	3.5	4.5	—	3.5	4.5	—	3.5	4.5	
Offset Adjustment Range		$R_p = 20k\Omega$	—	±3	—	—	±3	—	—	±3	—	mV

NOTES:

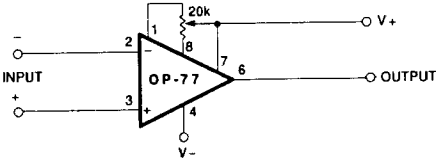
1. Long-Term Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
2. Sample tested.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \leq T_A \leq +85°C$ for OP-77E/FJ, $0°C \leq T_A \leq +70°C$ for OP-77E/F/GP and OP-77E/F/GS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77E MIN.	OP-77E TYP.	OP-77E MAX.	OP-77F MIN.	OP-77F TYP.	OP-77F MAX.	OP-77G MIN.	OP-77G TYP.	OP-77G MAX.	UNITS
Input Offset Voltage	V_{OS}	J, Z Packages P Package	— —	10 10	45 55	— —	20 20	100 100	— —	— 80	— 150	µV
Average Input Offset Voltage Drift	TCV_{OS}	J, Z Package (Note 1) P Package	— —	0.1 0.3	0.3 0.6	— —	0.2 0.4	0.6 1.0	— —	— 0.7	— 1.2	µV/°C
Input Offset Current	I_{OS}		—	0.5	2.2	—	0.5	4.5	—	0.5	4.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	1.5	40	—	1.5	85	—	1.5	85	pA/°C
Input Bias Current	I_B		−0.2	2.4	4.0	−0.2	2.4	6.0	−0.2	2.4	6.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	40	—	15	60	—	15	60	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	±13.0	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	3.0	—	0.1	3.0	µV/V
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	1.0	3.0	—	1.0	5.0	—	1.0	5.0	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	2000	6000	—	1000	4000	—	1000	4000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13.0	—	±12	±13.0	—	±12	±13.0	—	V
Power Consumption	P_D	$V_S = \pm 15V$, No Load	—	60	75	—	60	75	—	60	75	mW

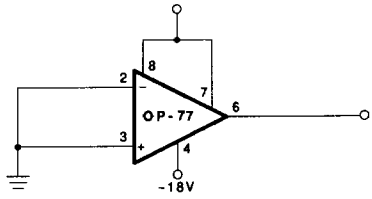
NOTES:
1. OP-77E: TCV_{OS} is 100% tested on J and Z packages.
2. Guaranteed by end-point limits.

Optional Offset Nulling Circuit



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

Burn-In Circuit



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

OP Amps