Octal D-type flip-flop; positive-edge trigger; 3-state — 74LV374

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Common 3-state output enable input**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV374 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT374.

The 74LV374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 3.3 V	13	ns
f_{max}	maximum clock frequency		77	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	25	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV374N	20	DIL	plastic	DIL20/SOT146
74LV374D	20	SO	plastic	SO20/SOT163A
74LV374DB	20	SSOP	plastic	SSOP20/SOT339
74LV374PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

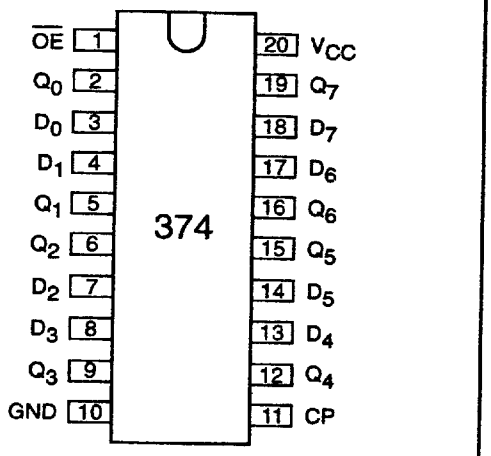


Fig.1 Pin configuration.

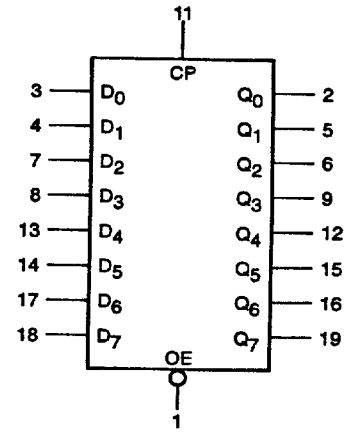


Fig.2 Logic symbol.

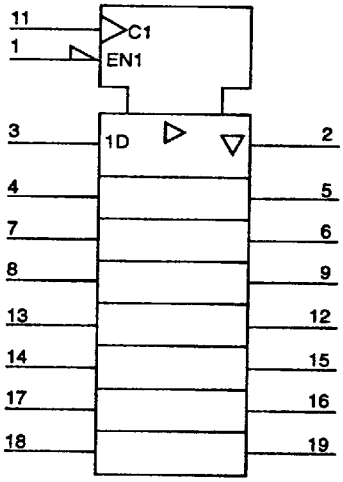


Fig3. IEC logic symbol.

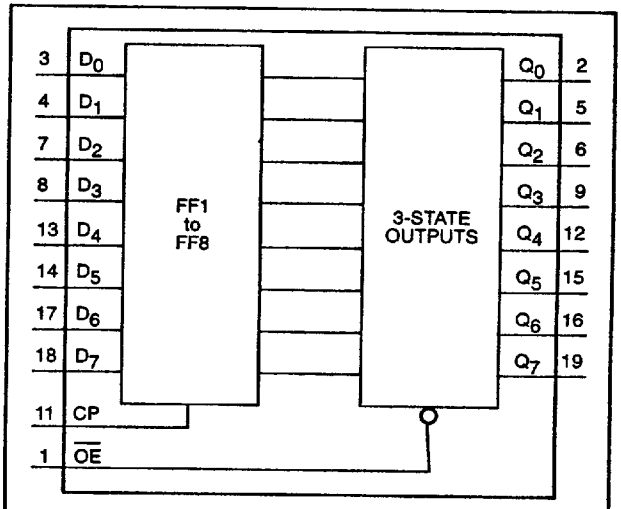


Fig.4 Functional diagram.

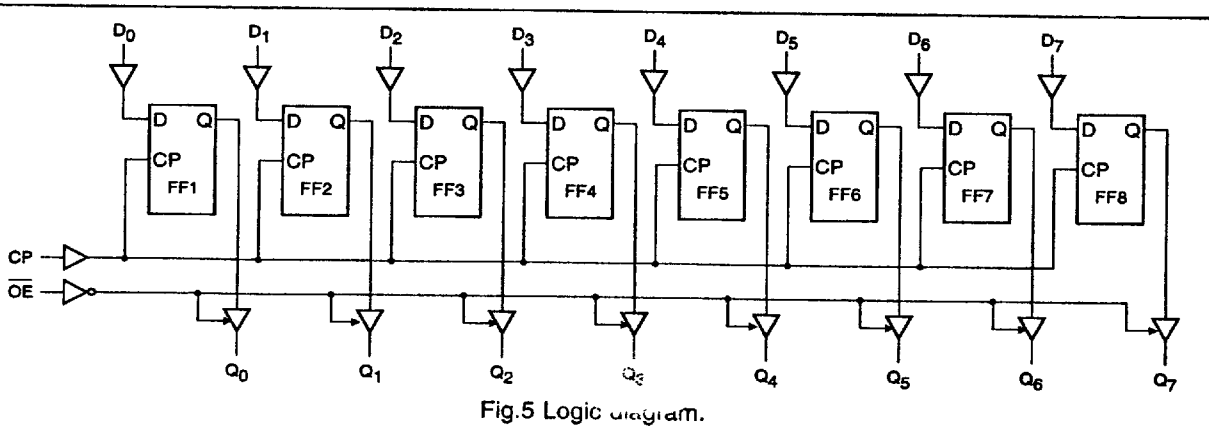


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L L	↑ ↑	l h	L H	L H
load register and disable outputs	H H	↑ ↑	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition

DC CHARACTERISTICS FOR 74LV374

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV374

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	– – – –	80 27 20 15*	– 51 38 30	– – – –	– 61 45 36	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– – – –	75 26 19 14*	– 49 36 29	– – – –	– 60 44 35	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– – – –	80 29 22 16*	– 48 36 29	– – – –	– 58 43 35	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.7

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS FOR 74LV374 *(Continued)*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_w	clock pulse width HIGH or LOW	34	12	–	41	–	ns	2.0	Fig.6
		25	9	–	30	–		2.7	
		20	7*	–	24	–		3.0 to 3.6	
t_{su}	set-up time D_n to CP	–	25	–	–	–	ns	1.2	Fig.8
		22	9	–	26	–		2.0	
		16	6	–	19	–		2.7	
		13	5*	–	15	–		3.0 to 3.6	
t_h	hold time D_n to CP	–	−10	–	–	–	ns	1.2	Fig.8
		5	−3	–	5	–		2.0	
		5	−2	–	5	–		2.7	
		5	−2*	–	5	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	15	40	–	12	–	MHz	2.0	Fig.6
		19	58	–	16	–		2.7	
		24	70*	–	20	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

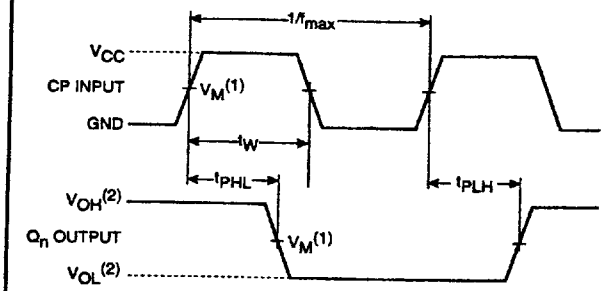


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

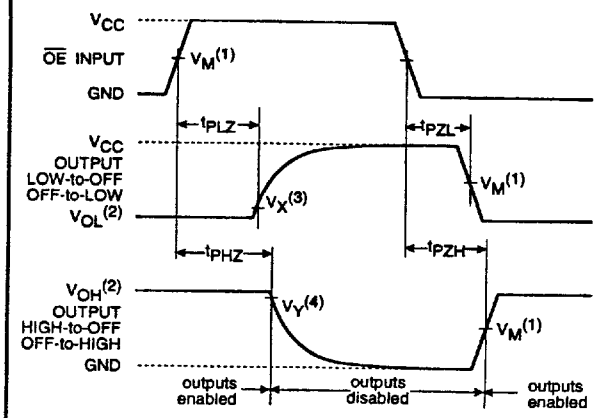


Fig.7 Waveforms showing the 3-state enable and disable times.

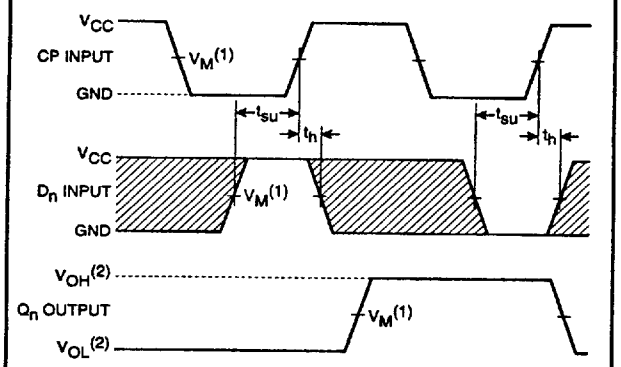
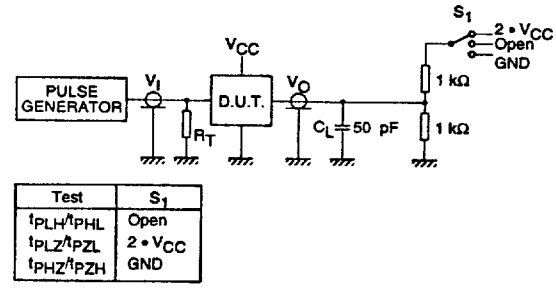


Fig.8 Waveforms showing the data set-up and hold times for the D_n input to the CP input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V