14-stage binary ripple counter — 74LV4020

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Frequency dividing circuits**
- **Time delay circuits**
- **Control counters**
- **Output capability: standard**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV4020 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT4020.

The 74LV4020 is a 14-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs (Q_0, Q_3 to Q_{13}). The counter is advanced on the HIGH-to-LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$. Each counter stage is a static toggle flip-flop.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0 Q_n to Q_{n+1} MR to Q_n	C_L = 15 pF V_{CC} = 3.3 V	 12 7 16	ns
f_{max}	maximum clock frequency		100	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4020N	16	DIL	plastic	SOT38-4
74LV4020D	16	SO	plastic	SOT109-1
74LV4020DB	16	SSOP	plastic	SOT338-1
74LV4020PW	16	TSSOP	plastic	SOT403-1

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	Q_0, Q_3 to Q_{13}	parallel outputs
8	GND	ground (0 V)
10	$\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
11	MR	master reset input (active HIGH)
16	V_{CC}	positive supply voltage

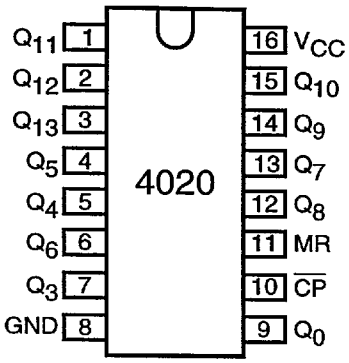


Fig.1 Pin configuration.

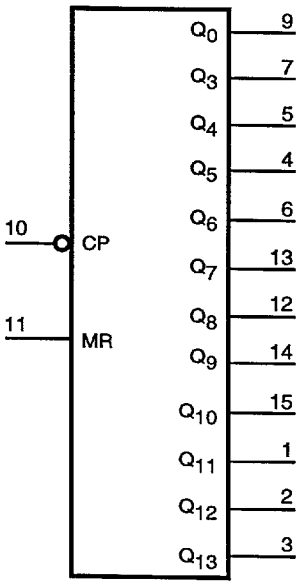


Fig.2 Logic symbol.

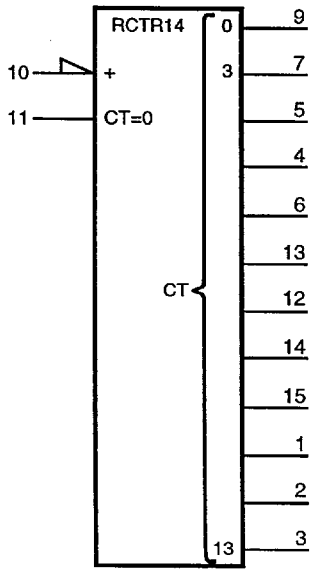


Fig.3 IEC Logic symbol.

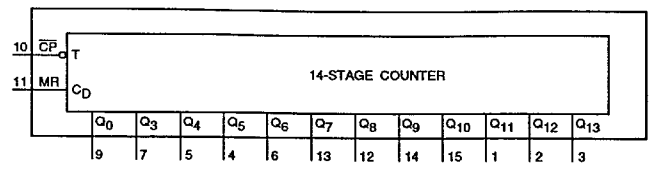


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	Q_0, Q_3 to Q_{13}
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

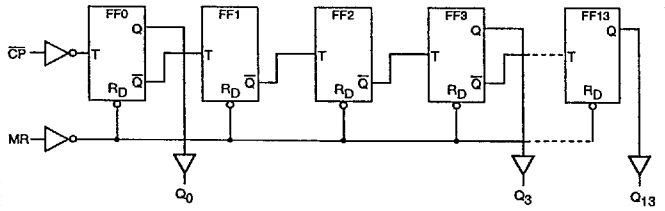


Fig. 5 Logic diagram.

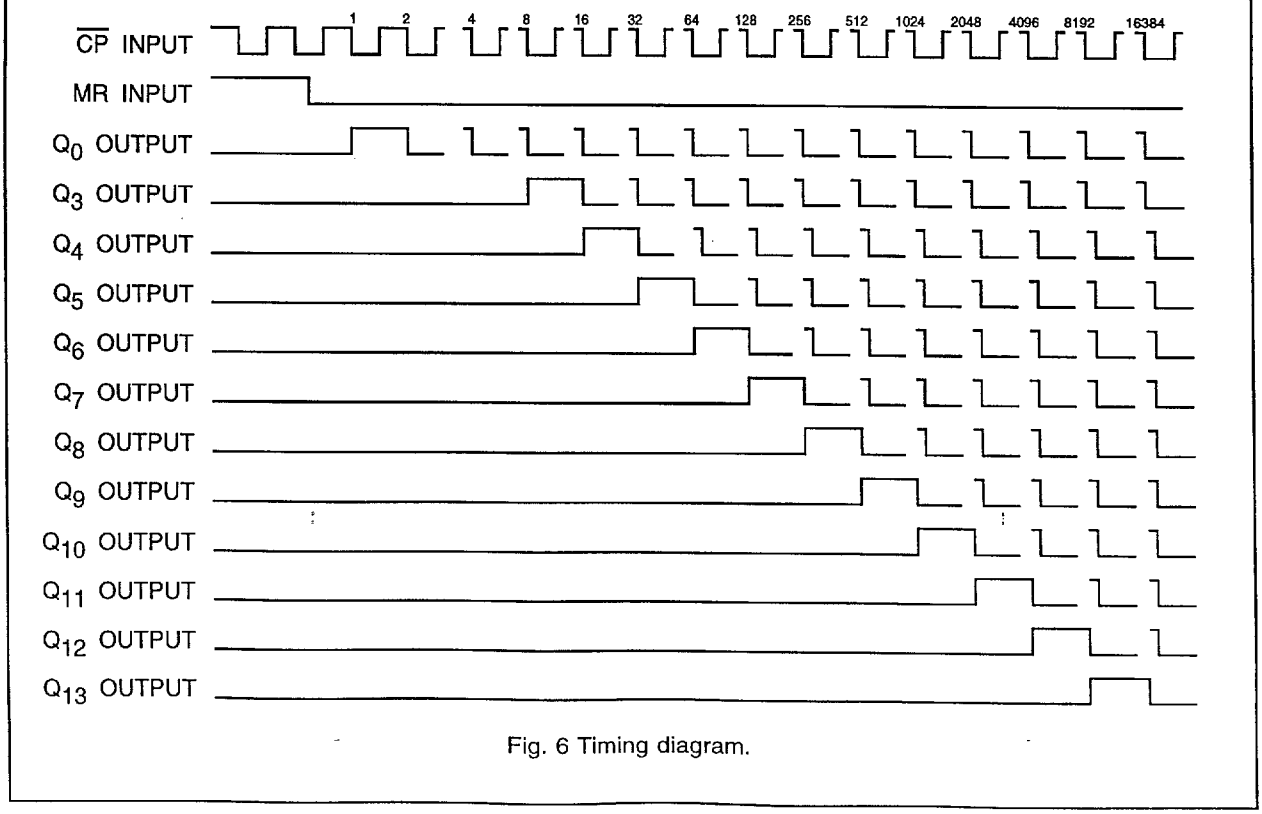


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74LV4020

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV4020

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_0	–	70	–	–	–	ns	1.2	Figs 7, 9
		–	24	44	–	54		2.0	
		–	18	33	–	40		2.7	
		–	13*	26	–	32		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay Q_n to Q_{n+1}	–	40	–	–	–	ns	1.2	Figs 7, 9
		–	14	26	–	31		2.0	
		–	10	19	–	23		2.7	
		–	8*	15	–	18		3.0 to 3.6	
t_{PHL}	propagation delay MR to Q_n	–	100	–	–	–	ns	1.2	Figs 8, 9
		–	34	65	–	77		2.0	
		–	25	48	–	56		2.7	
		–	19*	38	–	45		3.0 to 3.6	
t_W	clock pulse width HIGH to LOW	34	7	–	41	–	ns	2.0	Fig.6
		25	5	–	30	–		2.7	
		20	4*	–	24	–		3.0 to 3.6	
t_W	master reset pulse width HIGH	34	10	–	41	–	ns	2.0	Fig.7
		25	8	–	30	–		2.7	
		20	6*	–	24	–		3.0 to 3.6	
t_{rem}	removal time MR to $\overline{CP}$	–	10	–	–	–	ns	1.2	Fig.7
		22	4	–	26	–		2.0	
		16	3	–	19	–		2.7	
		13	2*	–	15	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	14	52	–	12	–	MHz	2.0	Fig.7
		19	76	–	16	–		2.7	
		24	92*	–	20	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

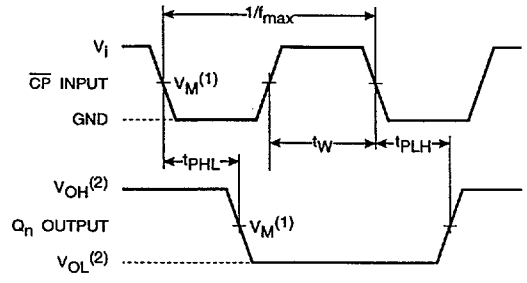


Fig.7 Waveforms showing the clock ($\overline{CP}$) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

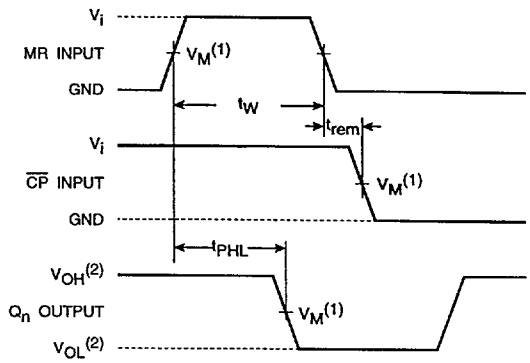
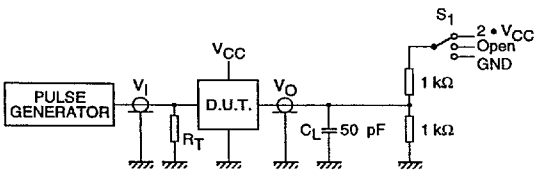


Fig.8 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}$) removal time.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.9 Load circuitry for switching times.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.