

12-stage binary ripple counter

74LV4040

FEATURES

- Optimized for Low Voltage applications: 1.0 to 5.5V
- Accepts TTL input levels between $V_{CC} = 2.7V$ and $V_{CC} = 3.6V$
- Typical V_{OLP} (output ground bounce) $< 0.8V$ @ $V_{CC} = 3.3V$, $T_{amb} = 25^{\circ}C$
- Typical V_{OHV} (output V_{OH} undershoot) $> 2V$ @ $V_{CC} = 3.3V$, $T_{amb} = 25^{\circ}C$
- Frequency dividing circuits
- Time delay circuits
- Control counters
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4040 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT4040.

The 74LV4040 is a 12-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs (Q_0 to Q_{11}). The counter is advanced on the HIGH-to-LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^{\circ}C$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $\overline{CP}$ to Q_0 Q_n to Q_{n+1} MR to Q_n	$C_L = 15pF$ $V_{CC} = 3.3V$	12 7 16	ns
f_{max}	Maximum clock frequency		100	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	30	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_I = GND$ to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	-40°C to +125°C	74LV4040 N	74LV4040 N	SOT38-4
16-Pin Plastic SO	-40°C to +125°C	74LV4040 D	74LV4040 D	SOT109-1
16-Pin Plastic SSOP Type II	-40°C to +125°C	74LV4040 DB	74LV4040 DB	SOT338-1
16-Pin Plastic TSSOP Type I	-40°C to +125°C	74LV4040 PW	74LV4040PW DH	SOT403-1

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PIN CONFIGURATION

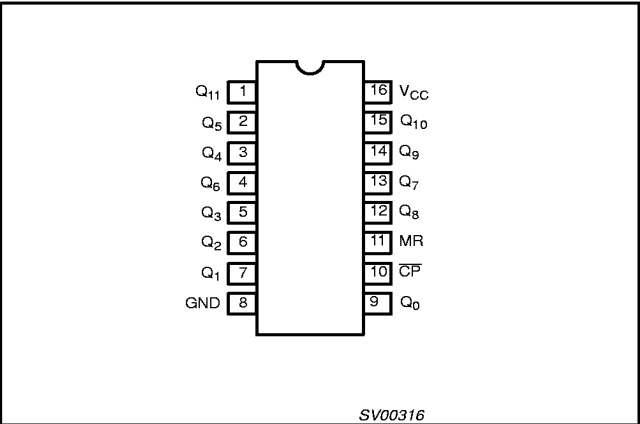


Figure 1. Pin configuration

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q ₀ to Q ₁₁	Parallel outputs
8	GND	Ground (0V)
10	$\overline{CP}$	Clock input (HIGH-to-LOW, edge-triggered)
11	MR	Master reset input (active HIGH)
16	V _{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)

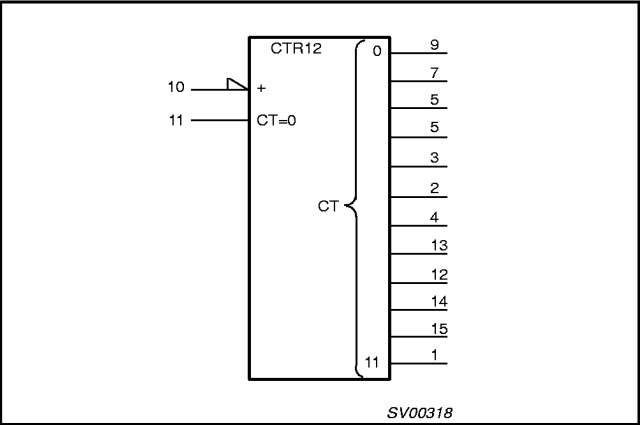


Figure 2. IEC Logic symbol

LOGIC SYMBOL

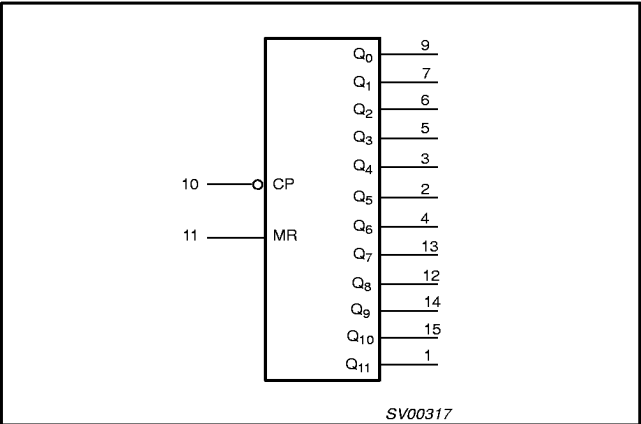


Figure 3. Logic symbol

FUNCTIONAL DIAGRAM

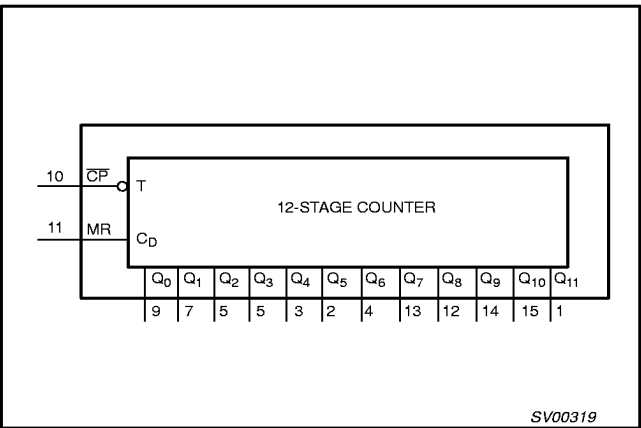


Figure 4. Functional diagram

LOGIC DIAGRAM

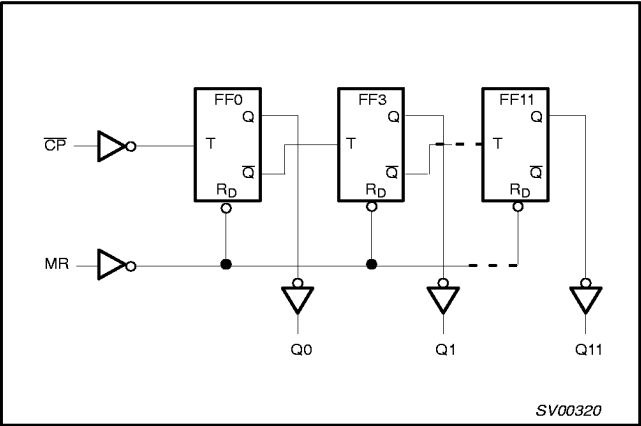


Figure 5. Logic diagram

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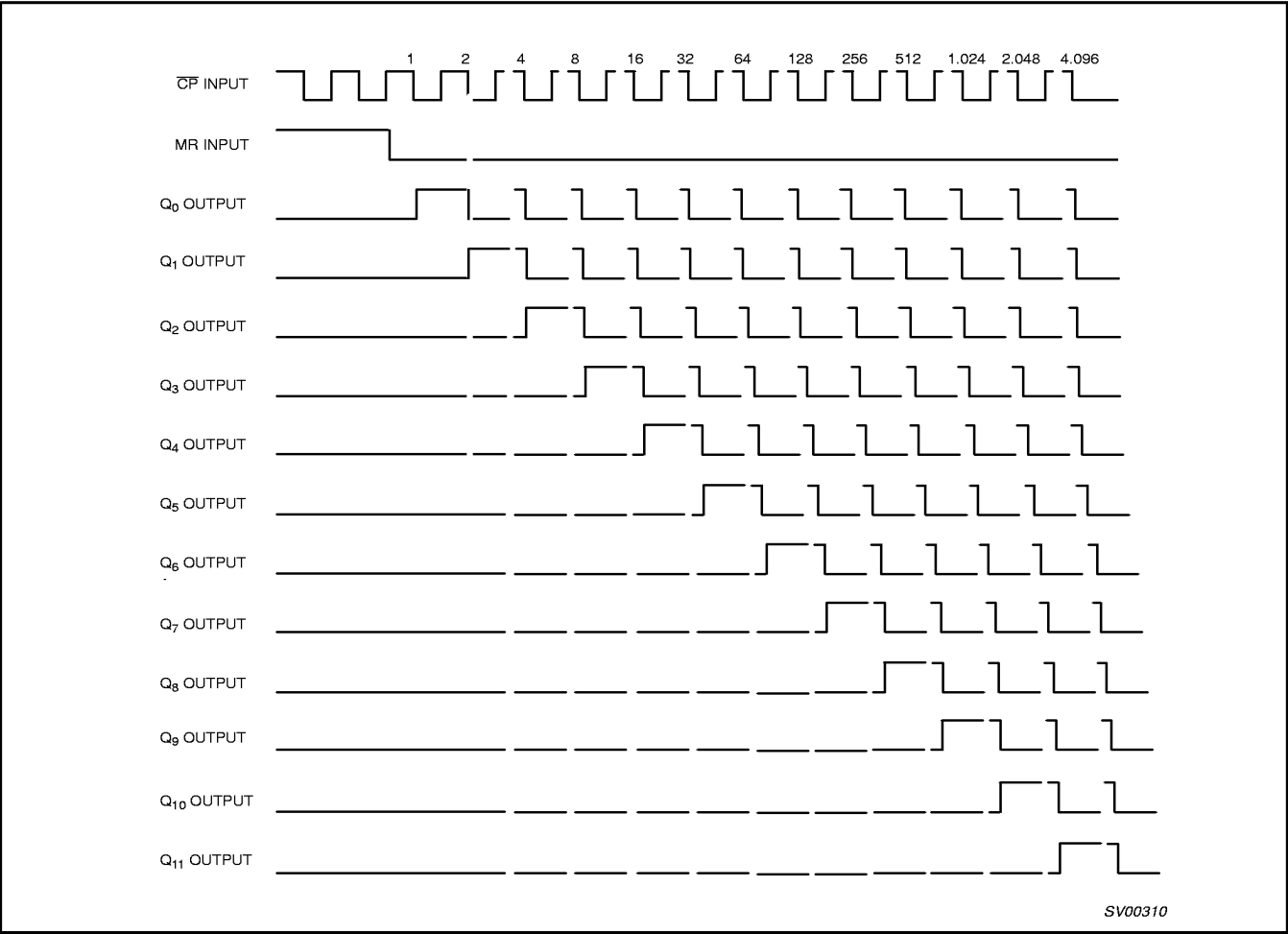


Figure 6. Timing diagram

FUNCTION TABLE

INPUTS		OUTPUTS
CP	MR	Q ₀ , Q ₃ to Q ₁₃
↑	L	no change
↓	L	count
X	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW -to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND},$ $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note ¹	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	−40 −40		+85 +125	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.0V$ to 2.0V $V_{CC} = 2.0V$ to 2.7V $V_{CC} = 2.7V$ to 3.6V $V_{CC} = 3.6V$ to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:

- The LV is guaranteed to function down to $V_{CC} = 1.0V$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2V$ to $V_{CC} = 5.5V$.

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DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP ¹	MAX	MIN	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	0.9			0.9		V
		V _{CC} = 2.0V	1.4			1.4		
		V _{CC} = 2.7 to 3.6V	2.0			2.0		
		V _{CC} = 4.5 to 5.5V	0.7*V _{CC}			0.7*V _{CC}		
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			0.3		0.3	V
		V _{CC} = 2.0V			0.6		0.6	
		V _{CC} = 2.7 to 3.6V			0.8		0.8	
		V _{CC} = 4.5 to 5.5			0.3*V _{CC}		0.3*V _{CC}	
V _{OH}	HIGH level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; -I _O = 100μA		1.2				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100μA	1.8	2.0		1.8		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; -I _O = 100μA	2.5	2.7		2.5		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100μA	2.8	3.0		2.8		
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; -I _O = 100μA	4.3	4.5		4.3		
V _{OH}	HIGH level output voltage; STANDARD outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 6mA	2.40	2.82		2.20		V
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; -I _O = 12mA	3.60	4.20		3.50		
V _{OL}	LOW level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		0				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		0	0.2		0.2	
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		0	0.2		0.2	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		0	0.2		0.2	
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		0	0.2		0.2	
V _{OL}	LOW level output voltage; STANDARD outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.25	0.40		0.50	V
		V _{CC} = 4.5V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.35	0.55		0.65	
I _I	Input leakage current	V _{CC} = 5.5V; V _I = V _{CC} or GND			1.0		1.0	μA
I _{CC}	Quiescent supply current; MSI	V _{CC} = 5.5V; V _I = V _{CC} or GND; I _O = 0			20.0		160	μA
ΔI _{CC}	Additional quiescent supply current per input	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} -0.6V			500		850	μA

NOTE:1. All typical values are measured at $T_{amb} = 25^\circ C$.

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AC CHARACTERISTICSGND = 0V; $t_r = t_f \leq 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
				$V_{CC}(\text{V})$	MIN	TYP ¹	MAX	MIN MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Q_0	Figure 7, 9	1.2	–	–	60	–	–	ns
			2.0	–	–	27	43	– 54	
			2.7	–	–	19	31	– 38	
			3.0 to 3.6	–	–	16 ²	26	– 32	
			4.5 to 5.5	–	–	1 ³	17	– 22	
t_{PHL}/t_{PLH}	Propagation delay Q_n to Q_{n+1}	Figure 7, 9	1.2	–	–	40	–	–	ns
			2.0	–	–	18	29	– 54	
			2.7	–	–	13	21	– 38	
			3.0 to 3.6	–	–	11 ²	18	– 32	
			4.5 to 5.5	–	–	7 ³	12	– 22	
t_{PHL}	Propagation delay MR to Q_n	Figure 8, 9	1.2	–	–	55	–	–	ns
			2.0	–	–	27	44	– 54	
			2.7	–	–	19	31	– 38	
			3.0 to 3.6	–	–	16 ²	26	– 32	
			4.5 to 5.5	–	–	11 ³	17	– 22	
t_W	Clock pulse width HIGH to LOW	Figure 7	2.0	35	7	–	41	54	ns
			2.7	25	5	–	30	–	
			3.0 to 3.6	20	4 ²	–	24	–	
			4.5 to 5.5	15	3 ³	–	18	–	
t_W	Master reset pulse width HIGH	Figure 8	2.0	35	11	–	41	–	ns
			2.7	25	9	–	30	–	
			3.0 to 3.6	20	8 ²	–	24	–	
			4.5 to 5.5	15	7 ³	–	18	–	
t_{rem}	Removal time MR to CP	Figure 8	1.2	–	–	10	–	–	ns
			2.0	22	5	–	26	–	
			2.7	16	4	–	19	–	
			3.0 to 3.6	13	3 ²	–	15	–	
			4.5 to 5.5	10	2 ³	–	12	–	
f_{max}	Maximum clock pulse frequency	Figure 7	2.0	14	60	–	12	–	MHz
			2.7	19	76	–	16	–	
			3.0 to 3.6	24	94 ²	–	20	–	
			4.5 to 5.5	36	112 ³	–	30	–	

NOTES:

1. Unless otherwise stated, all typical values are at $T_{amb} = 25^\circ\text{C}$.
2. Typical value measured at $V_{CC} = 3.3\text{V}$.
3. Typical value measured at $V_{CC} = 5.0\text{V}$.

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AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V \leq 3.6V$
 $V_M = 0.5V * V_{CC}$ at $V_{CC} < 2.7V$ and $\geq 4.5V$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

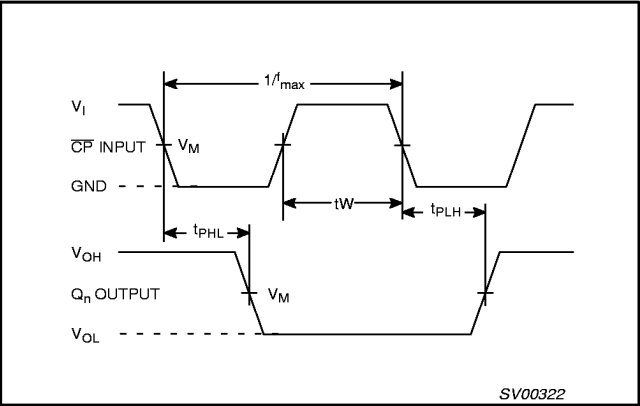


Figure 7. Clock ($\overline{CP}$) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency

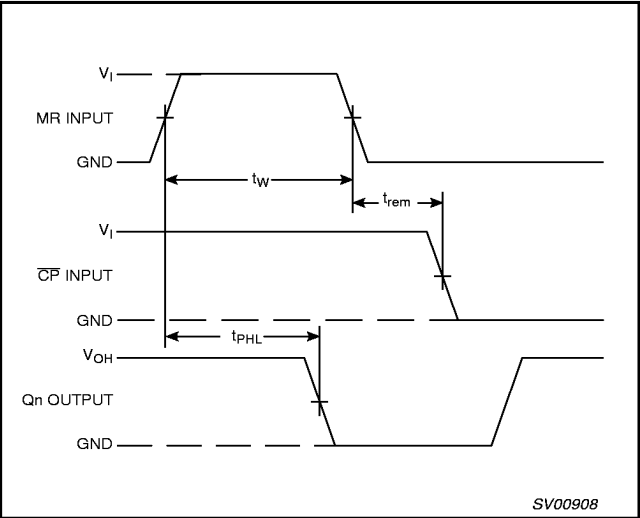


Figure 8. Master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}$) removal time

TEST CIRCUIT

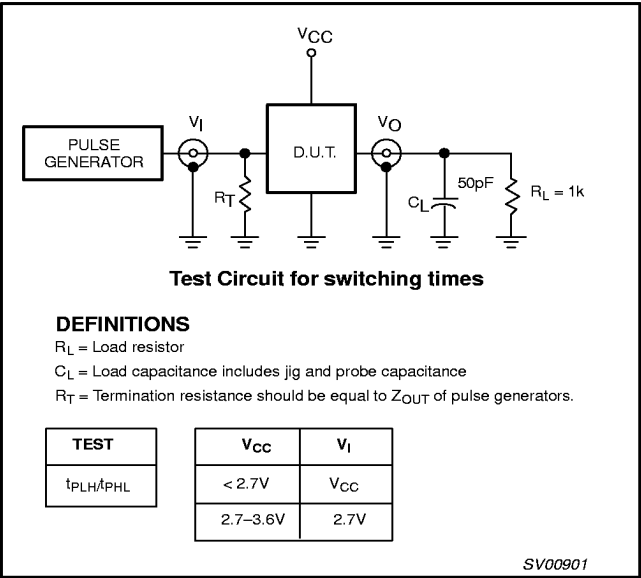


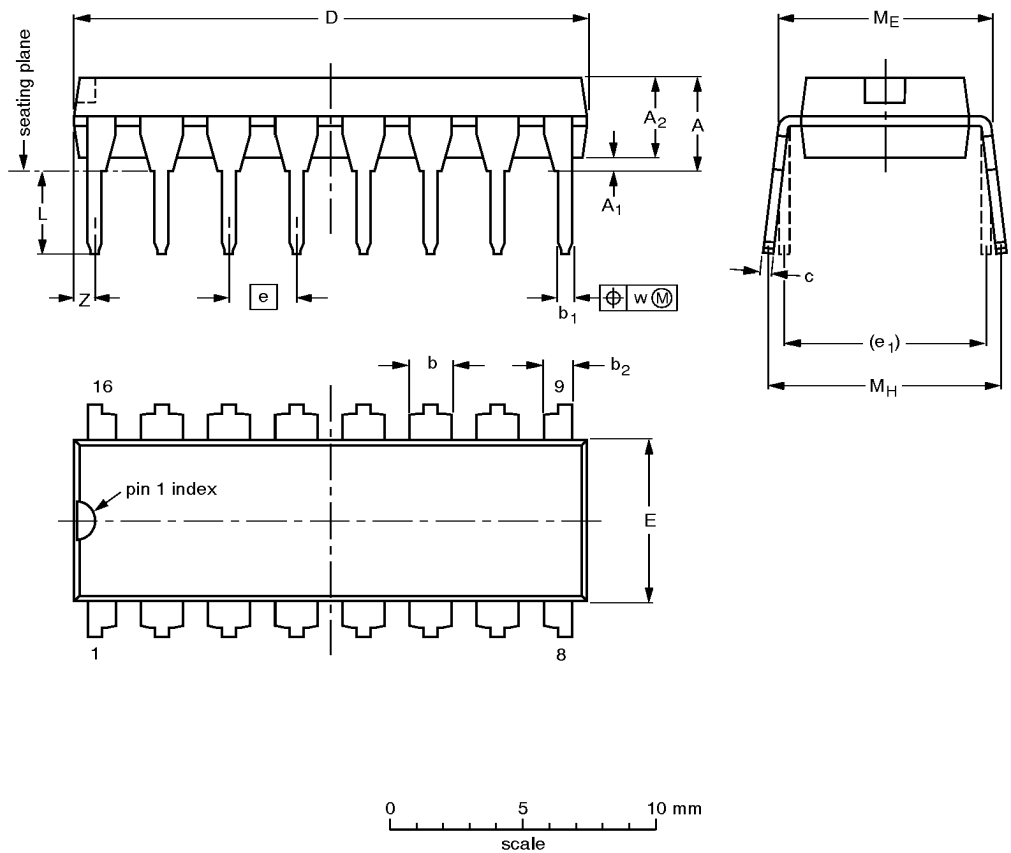
Figure 9. Load circuitry for switching times

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

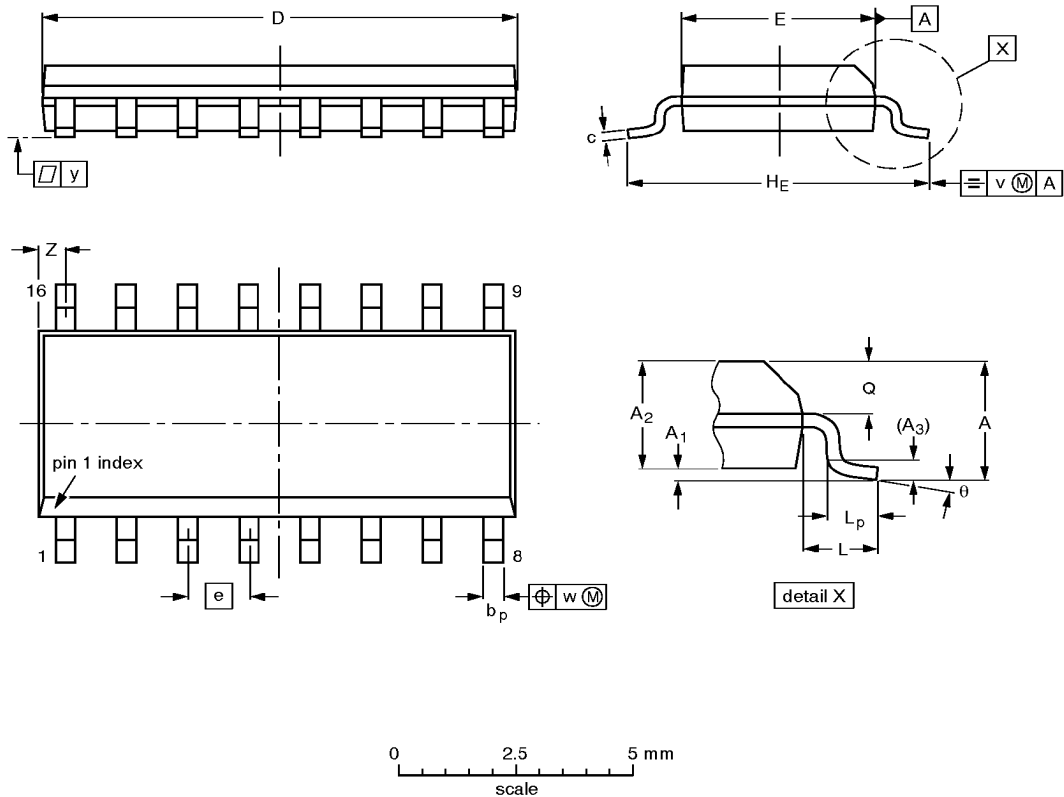
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

12-stage binary ripple counter

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

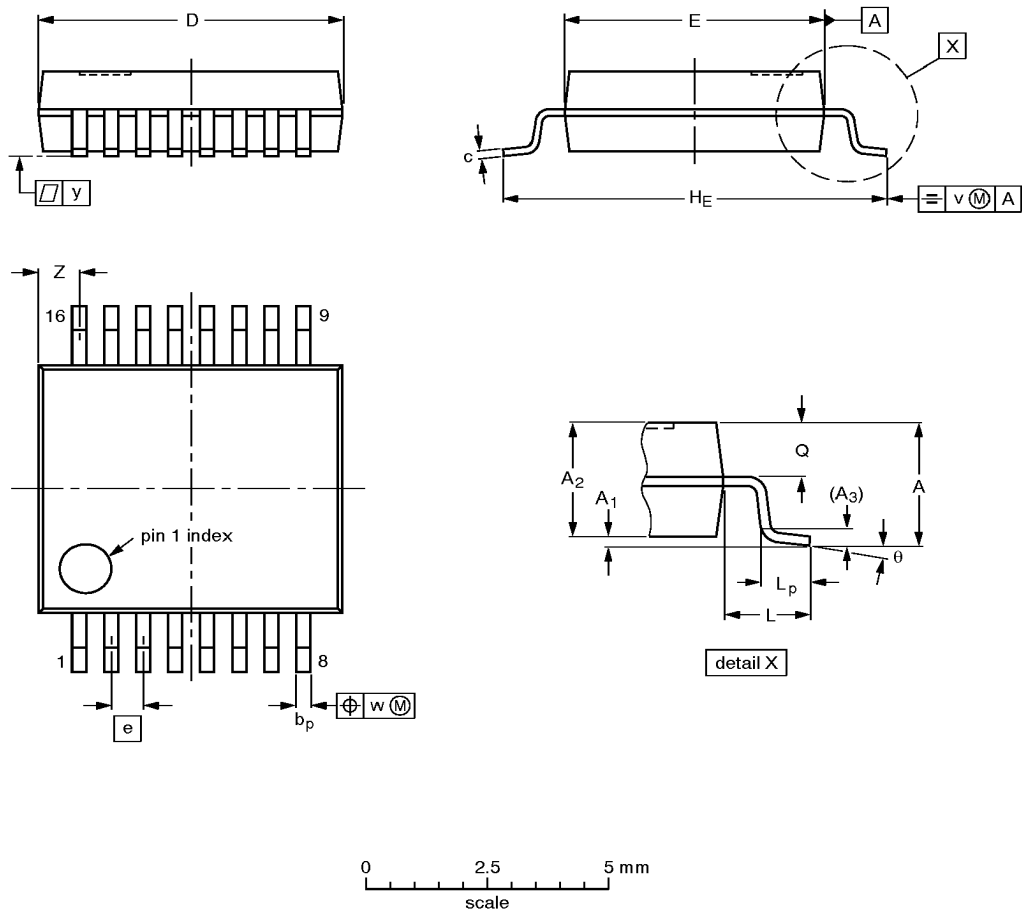
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	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				91-08-13 95-01-23

12-stage binary ripple counter

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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

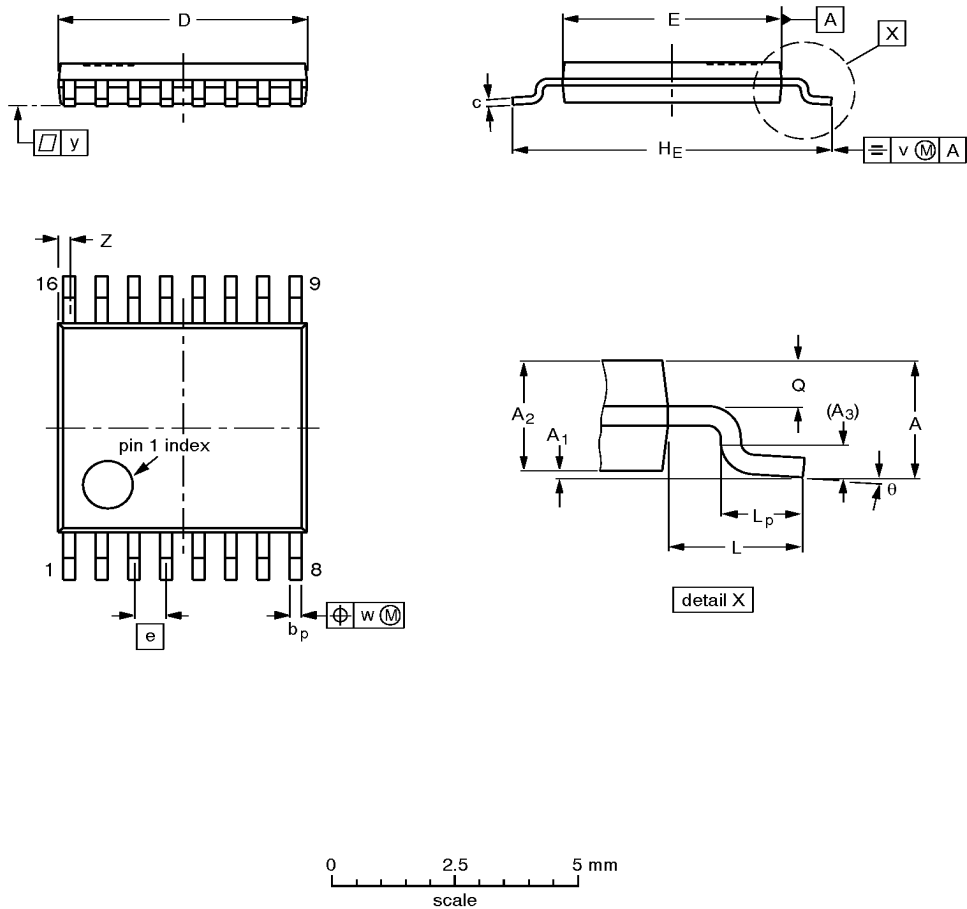
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14- 95-02-04

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

- Notes**
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04