

Quad bilateral switches

74LV4066

FEATURES

- Optimized for Low Voltage applications: 1.0V to 6.0V
- Accepts TTL input levels between $V_{CC} = 2.7\text{ V}$ and $V_{CC} = 3.6\text{ V}$
- Typical V_{OLP} (output ground bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$.
- Very low typ "ON" resistance:
 25Ω at $V_{CC} - V_{EE} = 4.5\text{ V}$
 35Ω at $V_{CC} - V_{EE} = 3.0\text{ V}$
 60Ω at $V_{CC} - V_{EE} = 2.0\text{ V}$
- Output capability: non-standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV4066 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT4066.

The 74LV4066 has four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH enable input (nE). When nE is LOW the corresponding analog switch is turned off.

The 74LV4066 has an on resistance which is dramatically reduced in comparison with 74HCT4066.

FUNCTION TABLE

INPUTS	SWITCH
nE	
L	off
H	on

NOTES:

H = HIGH voltage level

L = LOW voltage level

QUICK REFERENCE DATA

$GND = 0\text{ V}$; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{pZH}/t_{pZL}	Turn "ON" time: nE to V_{OS}	$C_L = 15\text{ pF}$ $R_L = 1\text{ k}\Omega$ $V_{CC} = 3.3\text{ V}$	10	ns
t_{pHZ}/t_{pLZ}	Turn "OFF" time: nE to V_{OS}		13	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per switch	Notes 1, 2	11	pF
C_S	Maximum switch capacitances		8	pF

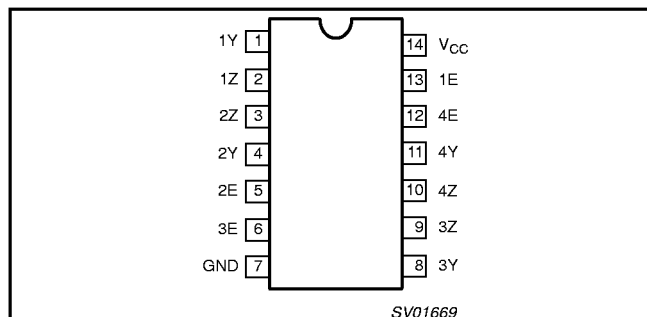
NOTES:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; C_S = maximum switch capacitance in pF;
 $\sum \{(C_L + C_S) \times V_{CC}^2 \times F_o\}$ = sum of the outputs.
 V_{CC} = supply voltage in V.
- The condition is $V_I = GND$ to V_{CC} .

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4066N	16	DIL	Plastic	SOT27-1
74LV4066D	16	SO	Plastic	SOT108-1
74LV4066DB	16	SSOP	Plastic	SOT337-1
74LV4066PW	16	TSSOP	Plastic	SOT402-1

PIN CONFIGURATION



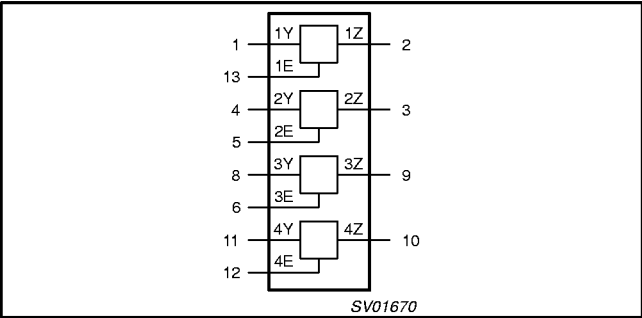
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 8, 11	1Y – 4Y	Independent inputs/outputs
2, 3, 9, 10	1Z – 4Z	Independent inputs/outputs
13, 5, 6, 12	1E to 4E	Enable input (active HIGH)
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

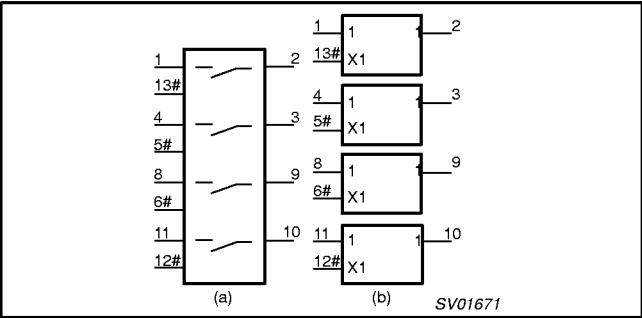
Quad bilateral switches

74LV4066

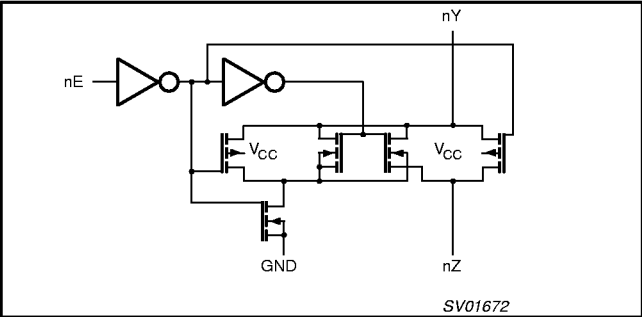
FUNCTIONAL DIAGRAM



IEC LOGIC SYMBOL



SCHEMATIC DIAGRAM (ONE SWITCH)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	6	V
V_I	Input voltage		0	—	V_{CC}	V
V_O	Output voltage		0	—	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	−40 −40		+85 +125	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$ $V_{CC} = 3.6V$ to $5.5V$	— — — —	— — — —	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to $V_{CC} = 1.0V$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2V$ to $V_{CC} = 5.5V$.

ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC switch current	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package — plastic DIL — plastic mini-pack (SO) — plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Quad bilateral switches

74LV4066

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP ¹	MAX	MIN	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2 V	0.90			0.90		V
		V _{CC} = 2.0 V	1.40			1.4		
		V _{CC} = 2.7 to 3.6 V	2.00			2.0		
		V _{CC} = 4.5 V	3.15			3.15		
		V _{CC} = 6.0 V	4.20			4.20		
V _{IL}	LOW level Input voltage	V _{CC} = 1.2 V			0.30		0.30	V
		V _{CC} = 2.0 V			0.60		0.60	
		V _{CC} = 2.7 to 3.6 V			0.80		0.80	
		V _{CC} = 4.5 V			1.35		1.35	
		V _{CC} = 6.0 V			1.80		1.80	
±I _I	Input leakage current	V _{CC} = 3.6 V; V _I = V _{CC} or GND V _{CC} = 6.0 V; V _I = V _{CC} or GND			1.0 2.0		1.0 2.0	μA
±I _S	Analog switch OFF-state current per channel	V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL} V _{CC} = 6.0 V; V _I = V _{IH} or V _{IL}			1.0 2.0		1.0 2.0	μA
±I _S	Analog switch ON-state current per channel	V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL} V _{CC} = 6.0 V; V _I = V _{IH} or V _{IL}			1.0 2.0		1.0 2.0	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0 V _{CC} = 6.0V; V _I = V _{CC} or GND; I _O = 0			20 40		40 80	μA
ΔI _{CC}	Additional quiescent supply current per input	V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} – 0.6 V			500		850	μA
R _{ON}	ON-resistance (peak)	V _{CC} = 1.2 V; V _I = V _{IH} or V _{IL}		300	—		—	Ω
		V _{CC} = 2.0 V; V _I = V _{IH} or V _{IL}		60	130		150	
		V _{CC} = 2.7 V; V _I = V _{IH} or V _{IL}		41	60		90	
		V _{CC} = 3.0 to 3.6 V; V _I = V _{IH} or V _{IL}		37	72		83	
		V _{CC} = 4.5 V; V _I = V _{IH} or V _{IL}		25	52		60	
		V _{CC} = 6.0 V; V _I = V _{IH} or V _{IL}		23	47		54	
R _{ON}	ON-resistance (rail)	V _{CC} = 1.2 V; V _I = V _{IH} or V _{IL}		75	—		—	Ω
		V _{CC} = 2.0 V; V _I = V _{IH} or V _{IL}		35	98		115	
		V _{CC} = 2.7 V; V _I = V _{IH} or V _{IL}		26	60		68	
		V _{CC} = 3.0 to 3.6 V; V _I = V _{IH} or V _{IL}		24	52		60	
		V _{CC} = 4.5 V; V _I = V _{IH} or V _{IL}		15	40		45	
		V _{CC} = 6.0 V; V _I = V _{IH} or V _{IL}		13	35		40	
R _{ON}	ON-resistance (rail)	V _{CC} = 1.2 V; V _I = V _{IH} or V _{IL}		75	—		—	Ω
		V _{CC} = 2.0 V; V _I = V _{IH} or V _{IL}		40	110		130	
		V _{CC} = 2.7 V; V _I = V _{IH} or V _{IL}		35	72		85	
		V _{CC} = 3.0 to 3.6 V; V _I = V _{IH} or V _{IL}		30	65		75	
		V _{CC} = 4.5 V; V _I = V _{IH} or V _{IL}		22	47		55	
		V _{CC} = 6.0 V; V _I = V _{IH} or V _{IL}		20	40		47	
ΔR _{ON}	Maximum variation of ON-resistance between any two channels	V _{CC} = 1.2 V; V _I = V _{IH} or V _{IL}		—				Ω
		V _{CC} = 2.0 V; V _I = V _{IH} or V _{IL}		5				
		V _{CC} = 2.7 V; V _I = V _{IH} or V _{IL}		4				
		V _{CC} = 3.0 to 3.6 V; V _I = V _{IH} or V _{IL}		4				
		V _{CC} = 4.5 V; V _I = V _{IH} or V _{IL}		3				
		V _{CC} = 6.0 V; V _I = V _{IH} or V _{IL}		2				

NOTE:

1. All typical values are measured at $T_{amb} = 25^\circ\text{C}$.
2. At supply voltage approaching 1.2V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

Quad bilateral switches

74LV4066

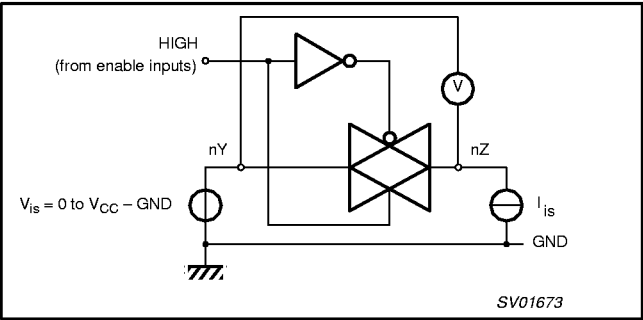


Figure 1. Test circuit for measuring ON-resistance (R_{ON}).

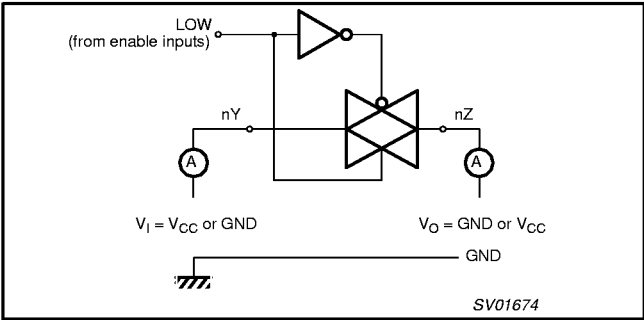


Figure 2. Test circuit for measuring OFF-state current.

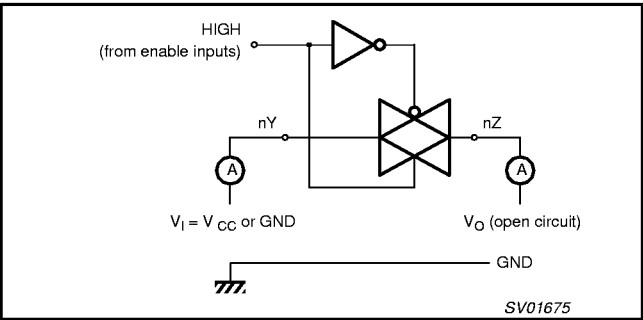


Figure 3. Test circuit for measuring ON-state current.

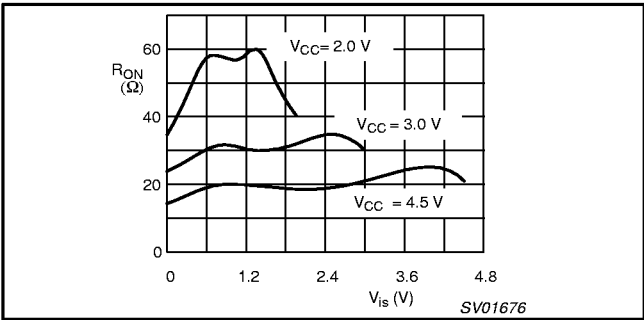


Figure 4. Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}) for $V_{is} = 0$ to $V_{CC} - V_{EE}$.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5\text{ ns}$; $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	LIMITS					UNIT	CONDITION	
		−40 to +85 °C			−40 to +125 °C			V _{CC} (V)	OTHER
		MIN	TYP ¹	MAX	MIN	MAX			
t _{PHL} /t _{PLH}	Propagation delay V _{is} to V _{os}		8				ns	1.2	R _L = ∞; C _L = 50 pF Figure 12
			5	26		31		2.0	
			3 ²	15		18		2.7 to 3.6	
			2	13		15		4.5	
			2	10		12		6.0	
t _{PZH} /t _{PZL}	Turn-on time nE to V _{os}		40				ns	1.2	R _L = 1 kΩ; C _L = 50 pF Figures 13 and 14
			22	43		51		2.0	
			12 ²	25		30		2.7 to 3.6	
			10	21		26		4.5	
			8	16		20		6.0	
t _{PHZ} /t _{PLZ}	Turn-off time nE to V _{os}		50				ns	1.2	R _L = 1 kΩ; C _L = 50 pF Figures 13 and 14
			27	65		81		2.0	
			15 ²	38		47		2.7 to 3.6	
			13	32		40		4.5	
			12	28		34		6.0	

NOTES:

1. All typical values are measured at $T_{amb} = 25^\circ\text{C}$.
2. All typical values are measured at $V_{CC} = 3.3\text{V}$.

Quad bilateral switches

74LV4066

ADDITIONAL AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5\text{ ns}$; $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	TYP	UNIT	V_{CC} (V)	$V_{IS(P-P)}$ (V)	CONDITIONS
	Sine-wave distortion $f = 1\text{ kHz}$	0.04	%	3.0	2.75	$R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ Figure 15
		0.02		6.0	5.50	
	Sine-wave distortion $f = 10\text{ kHz}$	0.12	%	3.0	2.75	$R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ Figure 15
		0.06		6.0	5.50	
	Switch "OFF" signal feed through	-50	dB	3.0	Note 1	$R_L = 600\text{ k}\Omega$; $C_L = 50\text{ pF}$; $f = 1\text{ MHz}$ Figures 10 and 16
		-50		6.0		
	Crosstalk between any two switches	-60	dB	3.0	Note 1	$R_L = 600\text{ k}\Omega$; $C_L = 50\text{ pF}$; $f = 1\text{ MHz}$ Figure 12
		-60		6.0		
$V_{(p-p)}$	Crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110	mV	3.0		$R_L = 600\text{ k}\Omega$; $C_L = 50\text{ pF}$; $f = 1\text{ MHz}$ (nE, square wave between V_{CC} and GND, $T_r = t_f = 6\text{ ns}$) Figure 13
		220		6.0		
f_{max}	Minimum frequency response (-3 dB)	180	mHz	3.0	Note 2	$R_L = 50\text{ k}\Omega$; $C_L = 50\text{ pF}$ Figures 11 and 14
		200		6.0		
C_S	Maximum switch capacitance	8	pF			

GENERAL NOTES:
 V_{IS} is the input voltage at nY or nZ terminal, whichever is assigned as an input.
 V_{OS} is the output voltage at nY or nZ terminal, whichever is assigned as an output.

- NOTES:**
- Adjust input voltage V_{IS} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
 - Adjust input voltage V_{IS} is 0 dBm level at V_{OS} for 1 MHz (0 dBm = 1 mW into 50 Ω).

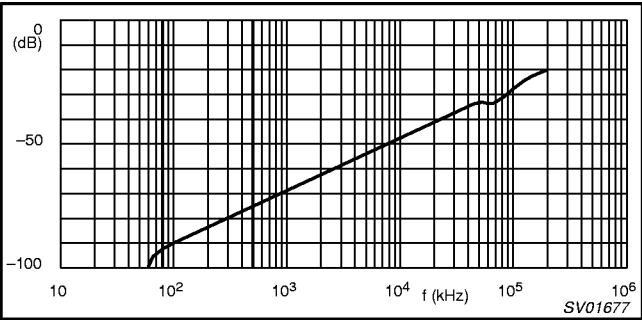


Figure 5. Typical switch "OFF" signal feed-through as a function of frequency.

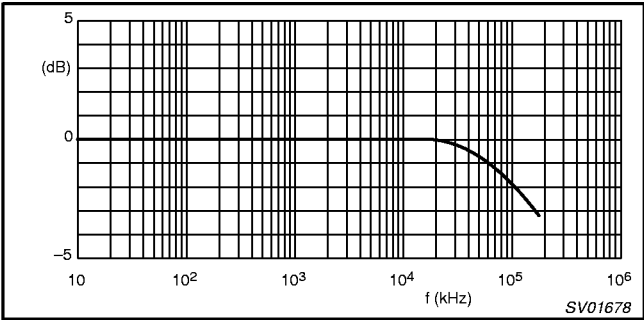


Figure 6. Typical frequency response.

NOTES TO FIGURES 5 AND 6:
Test conditions: $V_{CC} = 3.0\text{ V}$; GND = 0 V; $R_L = 50\text{ }\Omega$; $R_{SOURCE} = 1\text{ k}\Omega$.

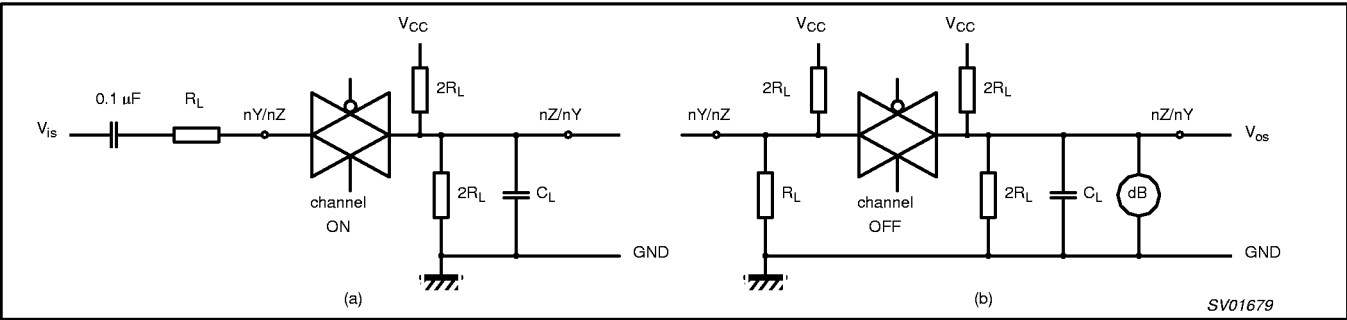


Figure 7. Test circuit for measuring crosstalk between any two switches.
(a) channel ON condition; (b) channel OFF condition.

Quad bilateral switches

74LV4066

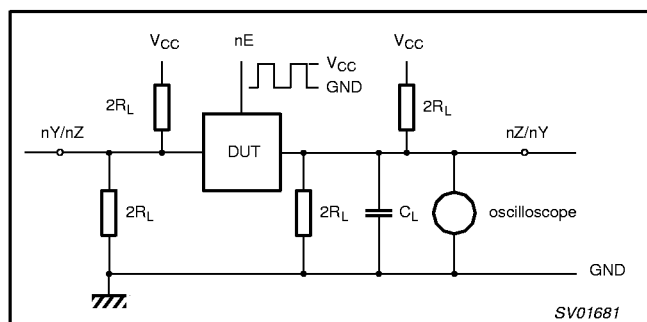


Figure 8. Test circuit for measuring crosstalk between control and any switch.

NOTE TO FIGURE 8:

The crosstalk is defined as follows (oscilloscope output):

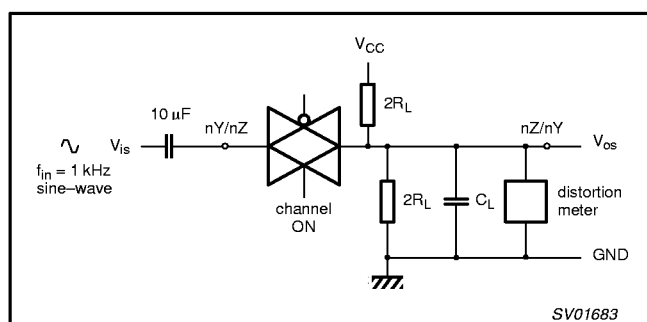
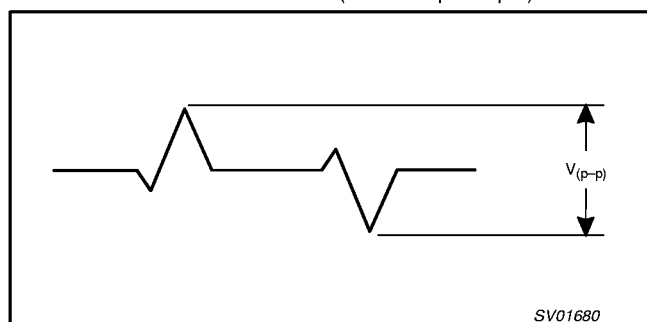


Figure 10. Test circuit for measuring sine-wave distortion.

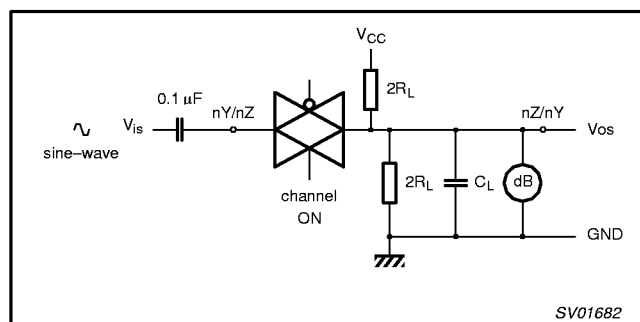


Figure 9. Test circuit for measuring minimum frequency response.

NOTE TO FIGURE 9:

Adjust input voltage to obtain 0 dBm at V_{OS} when $f_{in} = 1$ MHz. After set-up frequency of f_{in} is increased to obtain a reading of -3 dB at V_{OS} .

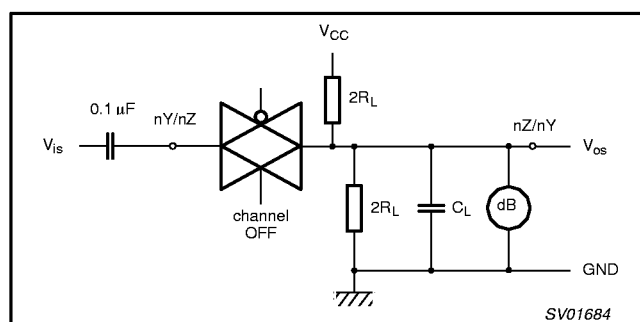


Figure 11. Test circuit for measuring switch "OFF" signal feed-through.

Quad bilateral switches

74LV4066

WAVEFORMS

$V_M = 1.5\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$
 $V_M = 0.5 \times V_{CC}$ at $V_{CC} \leq 2.7\text{ V}$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
 $V_X = V_{OL} + 0.3\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$
 $V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} < 2.7\text{ V}$
 $V_Y = V_{OH} - 0.3\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$
 $V_Y = V_{OH} - 0.1 \times V_{CC}$ $V_{CC} < 2.7\text{ V}$

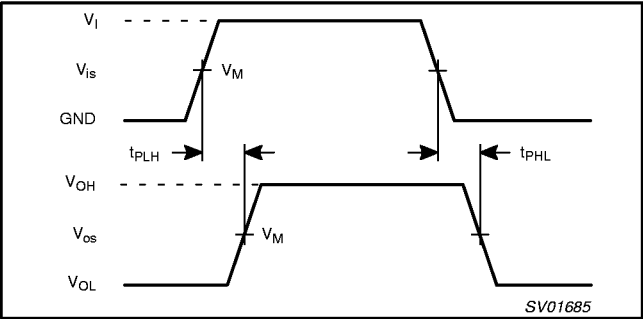


Figure 12. Input (V_{is}) to output (V_{os}) propagation delays.

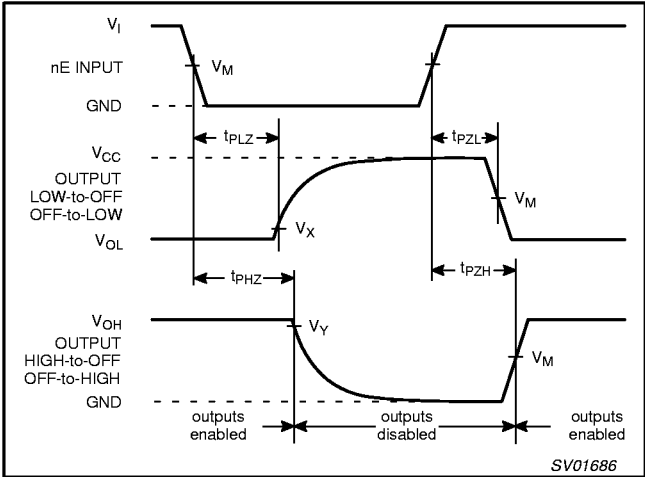


Figure 13. Turn-on and turn-off times for the inputs (nS, E) to the output (V_{os}).

TEST CIRCUIT

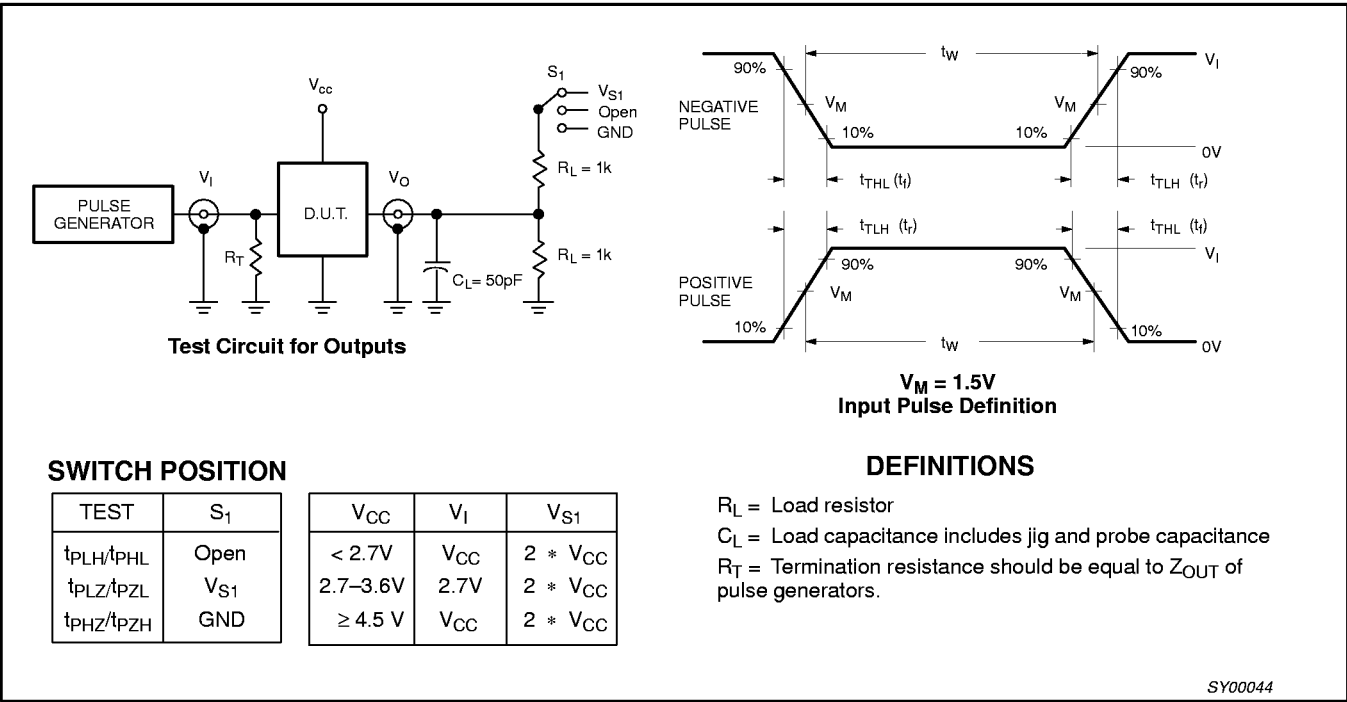


Figure 14. Load circuitry for switching times.