

**Octal D-type flip-flop with 5-volt tolerant inputs/outputs; positive edge-trigger; damping resistor; 3-state****74LVC2374A  
74LVCH2374A****FEATURES**

- 5-Volt tolerant inputs/outputs, for interfacing with 5-volt logic.
- Supply voltage range of 2.7 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when  $V_{CC} = 0$  V
- 8-bit positive edge-triggered register
- Independent register and 3-state buffer operation
- Bushold on all data inputs (LVCH2374A only).
- Integrated 30 $\Omega$  damping resistor.

**DESCRIPTION**

The 74LVC(H)2374A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC(H)2374A is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable ( $\overline{OE}$ ) input are common to all flip-flops. The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When  $\overline{OE}$  is LOW, the contents of the eight flip-flops is available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops. The '2374' is functionally identical to the '2574', but the '2574' has a different pin arrangement.

**QUICK REFERENCE DATA**GND = 0 V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f \leq 2.5$  ns

| SYMBOL            | PARAMETER                                   | CONDITIONS                        | TYPICAL | UNIT |
|-------------------|---------------------------------------------|-----------------------------------|---------|------|
| $t_{PHL}/t_{PLH}$ | propagation delay CP to $Q_n$               | $C_L = 50$ pF<br>$V_{CC} = 3.3$ V | 5.0     | ns   |
| $f_{max}$         | maximum clock frequency                     |                                   | 150     | MHz  |
| $C_i$             | input capacitance                           |                                   | 5.0     | pF   |
| $C_{PD}$          | power dissipation capacitance per flip-flop | notes 1 and 2                     | 20      | pF   |

**Notes to the quick reference data**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.
2. The condition is  $V_i = \text{GND to } V_{CC}$ .

**ORDERING INFORMATION**

| TYPE NUMBER     | PACKAGES |         |          |          |
|-----------------|----------|---------|----------|----------|
|                 | PINS     | PACKAGE | MATERIAL | CODE     |
| 74LVC(H)2374AD  | 20       | SO20    | plastic  | SOT163-1 |
| 74LVC(H)2374ADB | 20       | SSOP20  | plastic  | SOT339-1 |
| 74LVC(H)2374APW | 20       | TSSOP20 | plastic  | SOT360-1 |

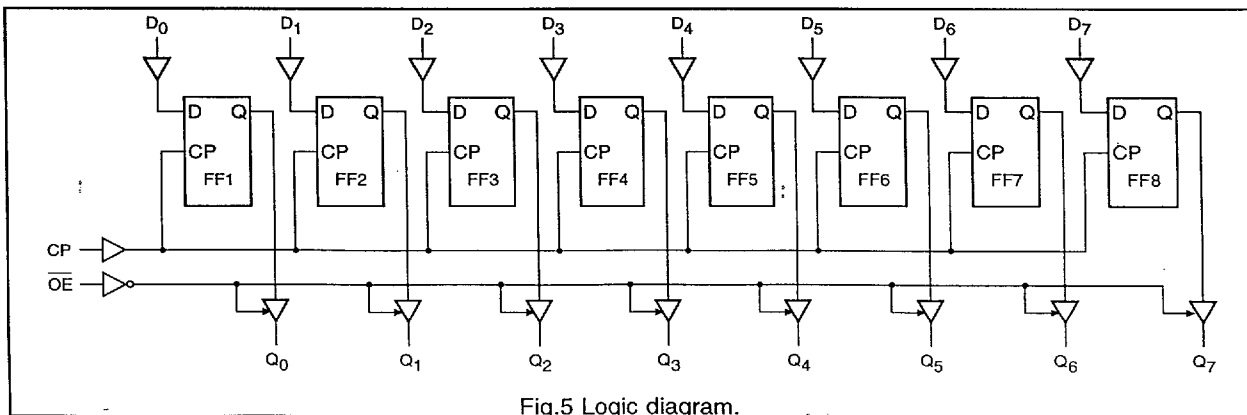
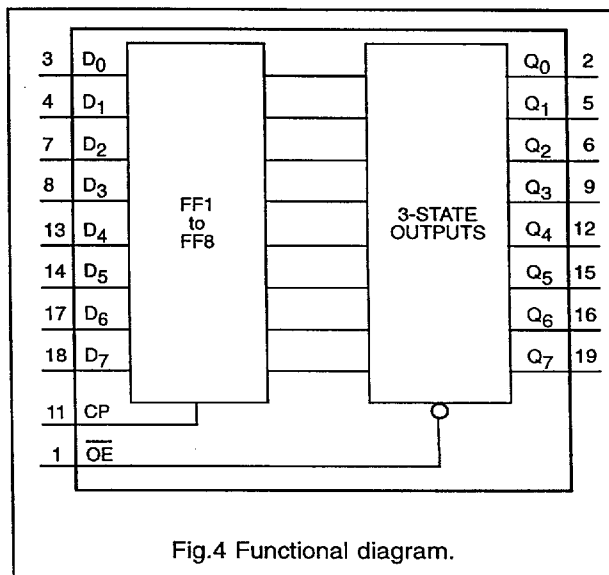
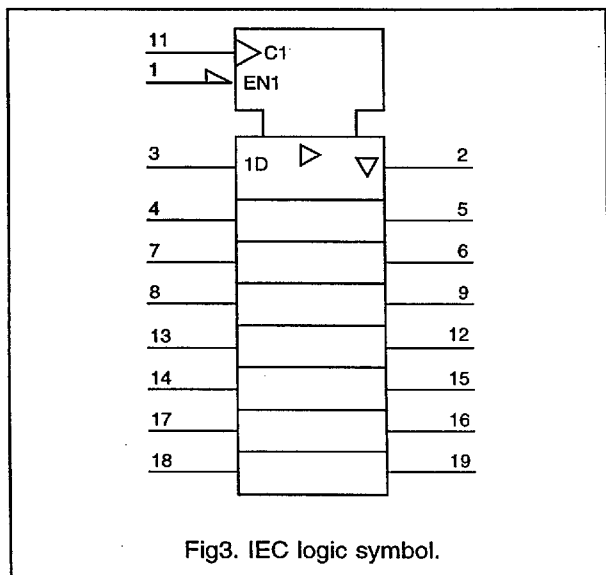
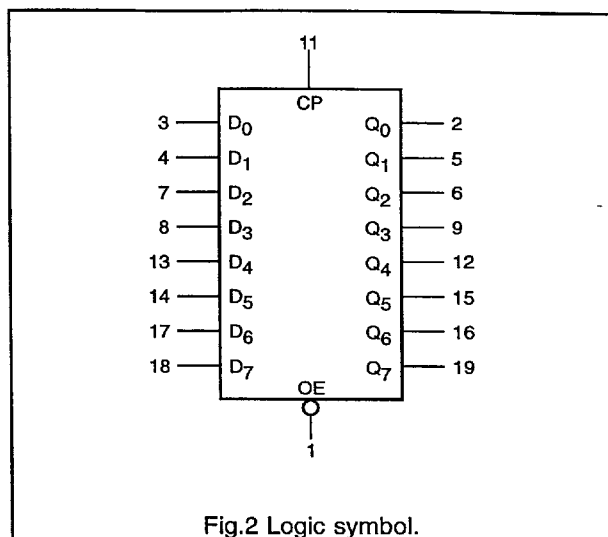
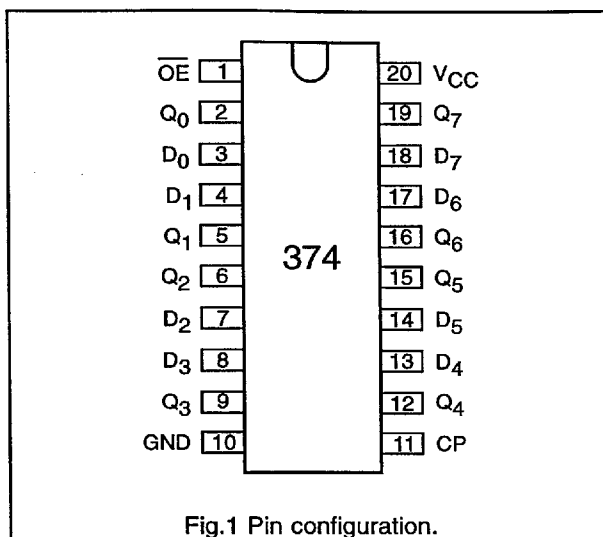
**PINNING**

| PIN                        | SYMBOL          | NAME AND FUNCTION                         |
|----------------------------|-----------------|-------------------------------------------|
| 1                          | $\overline{OE}$ | output enable input (active LOW)          |
| 2, 5, 6, 9, 12, 15, 16, 19 | $Q_0$ to $Q_7$  | 3-state flip-flop outputs                 |
| 3, 4, 7, 8, 13, 14, 17, 18 | $D_0$ to $D_7$  | data inputs                               |
| 10                         | GND             | ground (0 V)                              |
| 11                         | CP              | clock input (LOW-to-HIGH, edge-triggered) |
| 20                         | $V_{CC}$        | positive supply voltage                   |

Octal D-type flip-flop with 5-volt tolerant inputs/outputs;  
positive edge-trigger; damping resistor; 3-state

74LVC2374A

74LVCH2374A



Octal D-type flip-flop with 5-volt tolerant inputs/outputs;  
positive edge-trigger; damping resistor; 3-state

74LVC2374A  
74LVCH2374A

## FUNCTION TABLE

| OPERATING MODES                      | INPUTS          |        |                | INTERNAL<br>FLIP-FLOPS | OUTPUTS<br>Q <sub>0</sub> to Q <sub>7</sub> |
|--------------------------------------|-----------------|--------|----------------|------------------------|---------------------------------------------|
|                                      | $\overline{OE}$ | CP     | D <sub>n</sub> |                        |                                             |
| load and read register               | L<br>L          | ↑<br>↑ | l<br>h         | L<br>H                 | L<br>H                                      |
| load register and disable<br>outputs | H<br>H          | ↑<br>↑ | l<br>h         | L<br>H                 | Z<br>Z                                      |

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high impedance OFF-state

↑ = LOW-to-HIGH clock transition

## DC CHARACTERISTICS FOR 74LVC(H)2374A

For the DC characteristics see chapter "LVC(H)-A family characteristics", section "Family specifications".

## AC CHARACTERISTICS FOR 74LVC(H)2374A

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF

| SYMBOL                             | PARAMETER                                              | T <sub>amb</sub> (°C) |             |                 | UNIT | TEST CONDITIONS          |           |
|------------------------------------|--------------------------------------------------------|-----------------------|-------------|-----------------|------|--------------------------|-----------|
|                                    |                                                        | -40 to +85            |             |                 |      | V <sub>cc</sub><br>(V)   | WAVEFORMS |
|                                    |                                                        | MIN.                  | TYP.        | MAX.            |      |                          |           |
| t <sub>PHL</sub> /t <sub>PLH</sub> | propagation delay<br>CP to Q <sub>n</sub>              | —<br>1.5<br>1.5       | —<br>—<br>— | —<br>11<br>9.5  | ns   | 1.2<br>2.7<br>3.0 to 3.6 | Figs 6, 9 |
| t <sub>PZH</sub> /t <sub>PZL</sub> | 3-state output enable<br>time<br>OE to Q <sub>n</sub>  | —<br>1.5<br>1.5       | —<br>—<br>— | —<br>11<br>9.0  | ns   | 1.2<br>2.7<br>3.0 to 3.6 | Figs 7, 9 |
| t <sub>PHZ</sub> /t <sub>PLZ</sub> | 3-state output disable<br>time<br>OE to Q <sub>n</sub> | —<br>1.5<br>1.5       | —<br>—<br>— | —<br>6.5<br>6.0 | ns   | 1.2<br>2.7<br>3.0 to 3.6 | Figs 7, 9 |
| t <sub>w</sub>                     | clock pulse width HIGH<br>or LOW                       | —<br>—                | —<br>—      | —<br>—          | ns   | 2.7<br>3.0 to 3.6        | Fig.6     |
| t <sub>su</sub>                    | set-up time<br>D <sub>n</sub> to CP                    | —<br>—                | —<br>—      | —<br>—          | ns   | 2.7<br>3.0 to 3.6        | Fig.8     |
| t <sub>h</sub>                     | hold time<br>D <sub>n</sub> to CP                      | 1.0<br>1.0            | —<br>—      | —<br>—          | ns   | 2.7<br>3.0 to 3.6        | Fig.8     |
| f <sub>max</sub>                   | maximum clock pulse<br>frequency                       | —<br>75               | —<br>—      | —<br>—          | MHz  | 2.7<br>3.0 to 3.6        | Fig.6     |

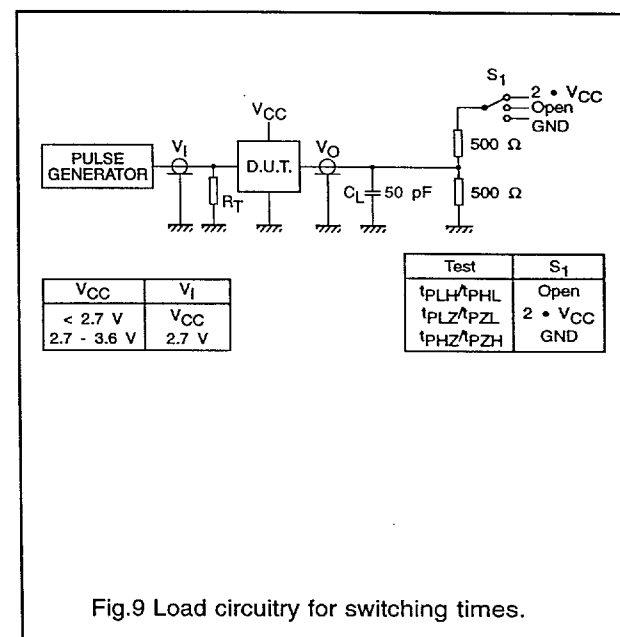
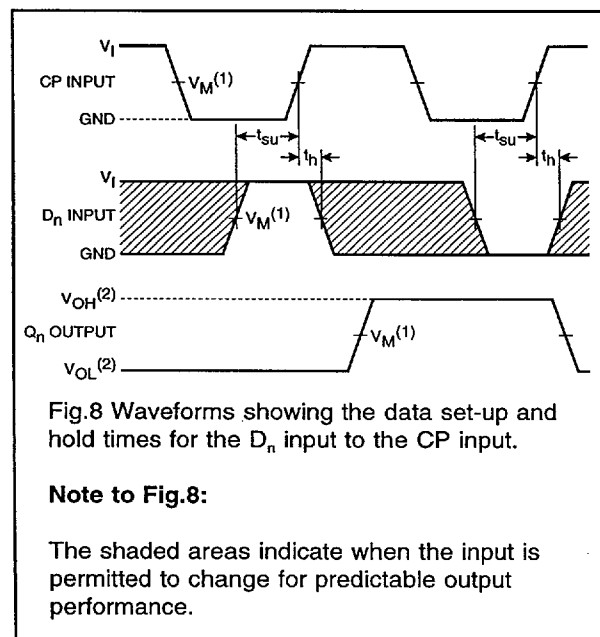
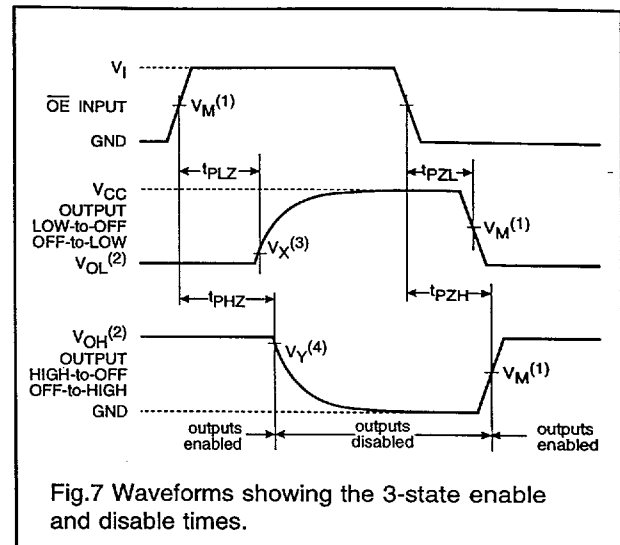
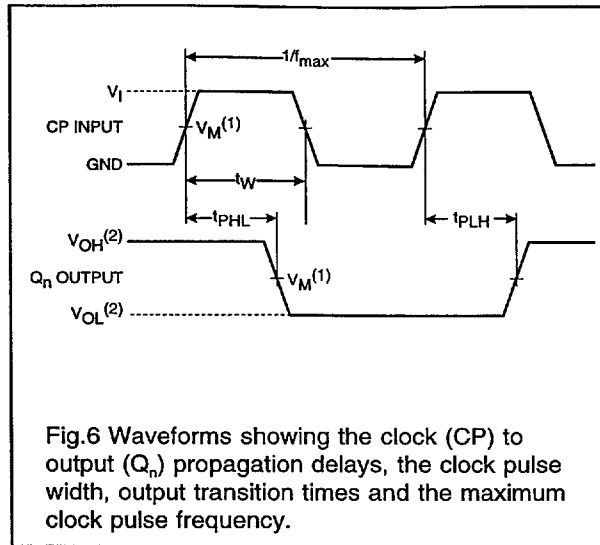
Notes: All typical values are measured at T<sub>amb</sub> = 25 °C.

\* Typical values are measured at V<sub>CC</sub> = 3.3 V.

Octal D-type flip-flop with 5-volt tolerant inputs/outputs;  
positive edge-trigger; damping resistor; 3-state

74LVC2374A  
74LVCH2374A

## AC WAVEFORMS



- Notes:**
- (1)  $V_M = 1.5$  V at  $V_{CC} \geq 2.7$  V  
 $V_M = 0.5 \cdot V_{CC}$  at  $V_{CC} < 2.7$  V
  - (2)  $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load
  - (3)  $V_X = V_{OL} + 0.3$  V at  $V_{CC} \geq 2.7$  V  
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$  at  $V_{CC} < 2.7$  V
  - (4)  $V_Y = V_{OH} - 0.3$  V at  $V_{CC} \geq 2.7$  V  
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$  at  $V_{CC} < 2.7$  V