Octal registered tranceiver with 5-volt tolerant inputs/ouputs (3-State)

74LVC2952A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with the JEDEC standard no. 8-1 A
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Flow-through pin-out architecture
- 3-State outputs
- Direct interface with TTL levels
- Integrated 30Ω damping resistor

DESCRIPTION

The 74LVC2952A is a low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. The 74LVC2952A is an octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional busses. Data applied to the inputs is entered and stored on the rising edge of the clock (CPnn) provided that the clock enable ($\overline{CE}_{nn}$) is LOW. The data is then present at the 3-State output buffers, but is only accessible when the output enable input ($\overline{OE}_{nn}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs. The 74LVC2952A is identical to the 74LVC2953A but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP_{nn} to A_n, B_n	C_L = 50 pF; V_{CC} = 3.3 V	4.3	ns
f_{max}	Maximum clock frequency		150	MHz
C_I	Input capacitance		5	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3V[1]	31	pF

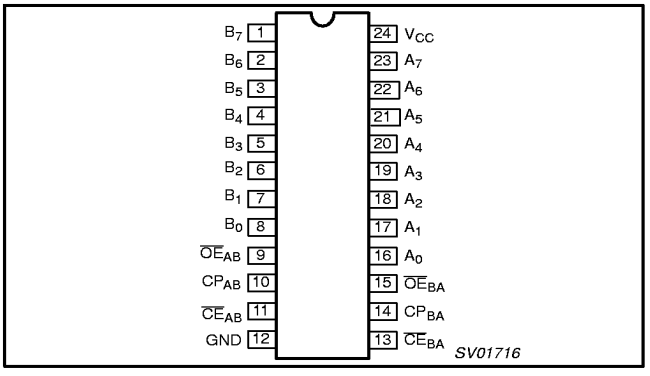
NOTE:

1 C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; C_L = output load capacity in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +125°C	74LVC2952A D	74LVC2952A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +125°C	74LVC2952A DB	74LVC2952A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +125°C	74LVC2952A PW	74LVC2952APW DH	SOT355-1

PIN CONFIGURATION

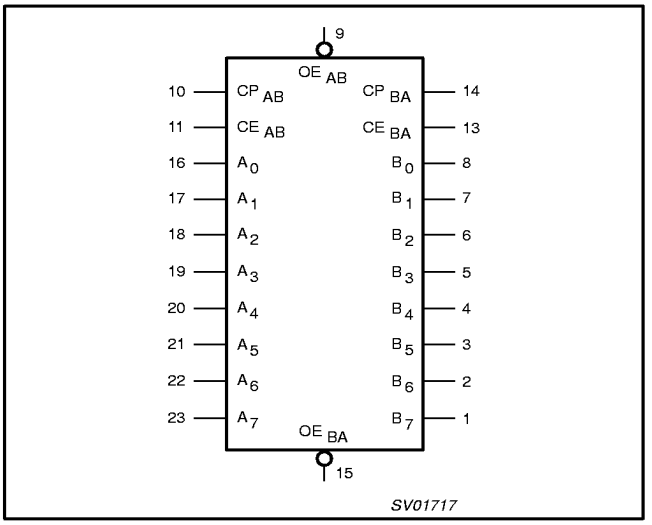


PIN DESCRIPTION

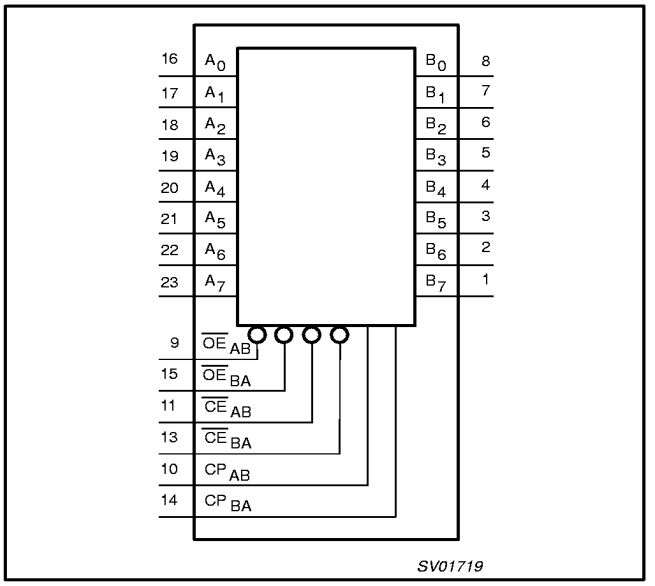
PIN NUMBER	SYMBOL	FUNCTION
8, 7, 6, 5, 4, 3, 2, 1,	B_0 to B_7	B data inputs/outputs
12	GND	Ground (0 V)
9, 15	$\overline{OE}_{AB}$,$\overline{OE}_{BA}$	Output enable inputs (active LOW)
10, 14	CP_{AB}, CP_{BA}	Clock inputs
11, 13,	$\overline{CE}_{AB}$, $\overline{CE}_{BA}$	Clock enable inputs
16, 17, 18, 19, 20, 21, 22, 23	A_0 to A_7	A data inputs/outputs
24	V_{CC}	Positive supply voltage

Octal registered tranceiver with 5-volt tolerant inputs/ouputs (3-State)

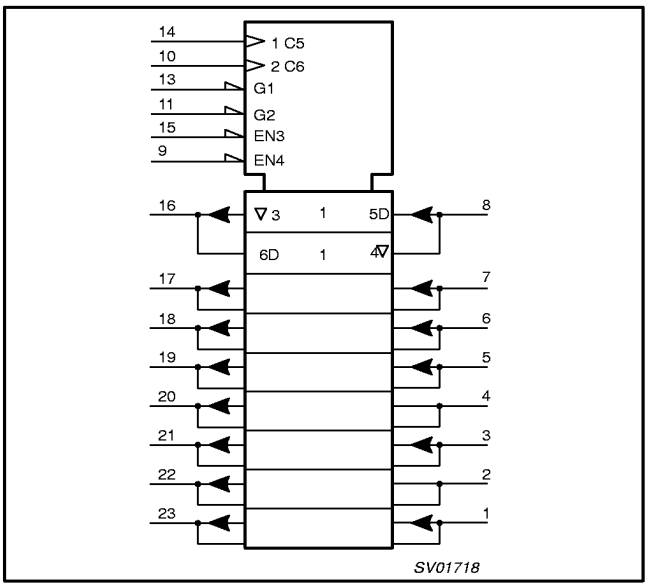
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC SYMBOL



FUNCTION TABLE for register A_n or B_n

INPUTS			INTERNAL Q	OPERATING MODE
A_n or B_n	CP_{nn}	$\overline{CE}_{nn}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

FUNCTION TABLE for output enable

INPUTS	INTERNAL Q	A_n or B_n OUTPUTS	OPERATING MODE
$\overline{OE}_{nn}$			
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	Enable outputs

Z = high impedance OFF-state
↑ = Low-to-High transition
NC = no change

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC input voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_{I/O}$	DC output voltage; output HIGH or LOW	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2 The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V		V_{CC}			V
		V_{CC} = 2.7 to 3.6V		2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V				GND	V
		V_{CC} = 2.7 to 3.6V				0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA		V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA		V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA		V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA		V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA				0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA				0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA				0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND	Not for I/O pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 3.6V; V_I = 5.5V or GND			±0.1	±15	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND			0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V				±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0			5	500	µA

NOTES:

1 All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF; R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			V_{CC} = 1.2V	
			MIN	TYP	MAX	MIN	TYP	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay CP_{BA}, CP_{AB} to A_n, B_n	Figures 1, 4	1.5	4.1	7.6	1.5	4.4	8.6	16	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$, to A_n, B_n	Figures 3, 4	1.5	3.9	7.6	1.5	4.7	8.6	16	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$, to A_n, B_n	Figures 3, 4	1.5	3.4	6.6	1.5	3.8	7.6	8	ns
t_w	CP_{AB}, CP_{BA} pulse width, HIGH or LOW	Figure 1	3.0	1.5	–	3.0	1.5	–	–	ns
t_{su}	Set-up time HIGH or LOW A_n, B_n to CP_{AB}, CP_{BA}	Figure 2	2.0	–0.5	–	2.0	–	–	–	ns
t_{su}	Set-up time, HIGH or LOW $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	Figure 2	2.0	0.5	–	2.0	–	–	–	ns
t_h	Hold time A_n, B_n to CP_{AB}, CP_{BA}	Figure 2	1.5	0.6	–	1.5	–	–	–	ns
t_h	Hold time $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	Figure 2	1.5	0	–	1.5	–	–	–	ns
f_{max}	Maximum clock pulse frequency	Figure 2	100	150	–	80	–	–	–	MHz

NOTE:

These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 0.6 V at V_{CC} = 1.2 V
V_M = 1.0 V at V_{CC} = 2.0 V
V_M = 1.5 V at V_{CC} = 3.0 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-State output load.

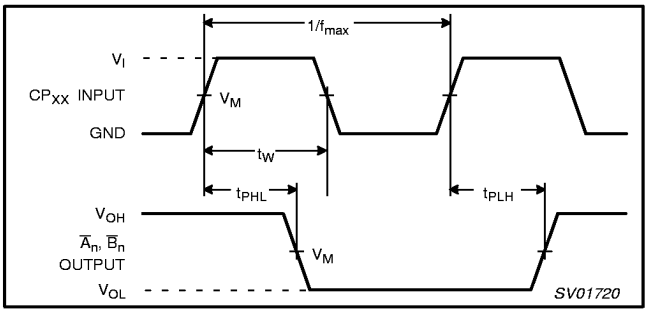


Figure 1. Clock input (CP_{BA}, CP_{AB}) to output ($\overline{B}_n$, $\overline{A}_n$) propagation delays, the clock pulse width and the maximum clock frequency.

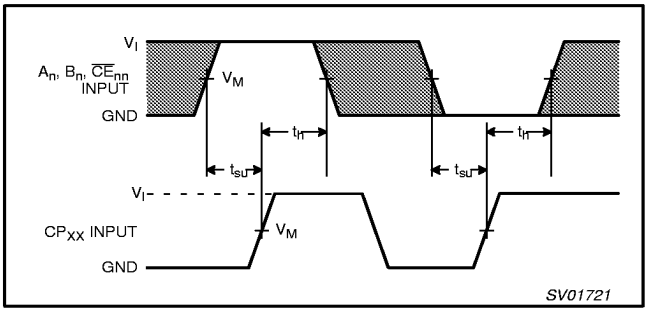


Figure 2. Set-up and hold times for the A_n, B_n and $\overline{CE}_{nn}$ inputs.

NOTE:
The shaded areas indicate when the input is permitted to change for predictable output performance

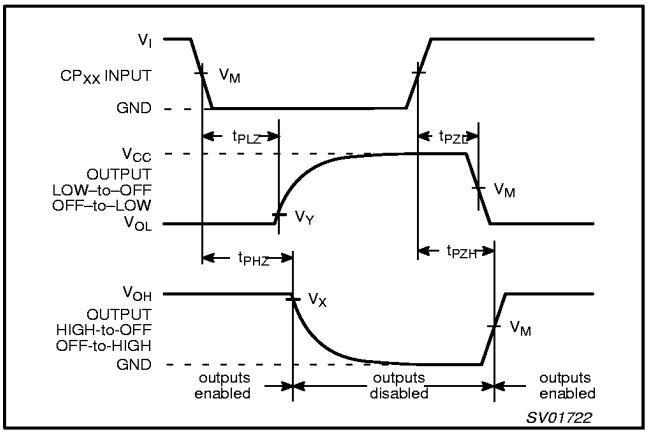


Figure 3. 3-State enable and disable times.

TEST CIRCUIT

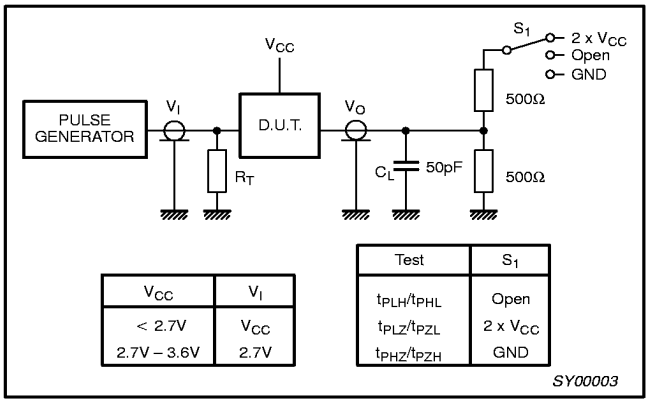
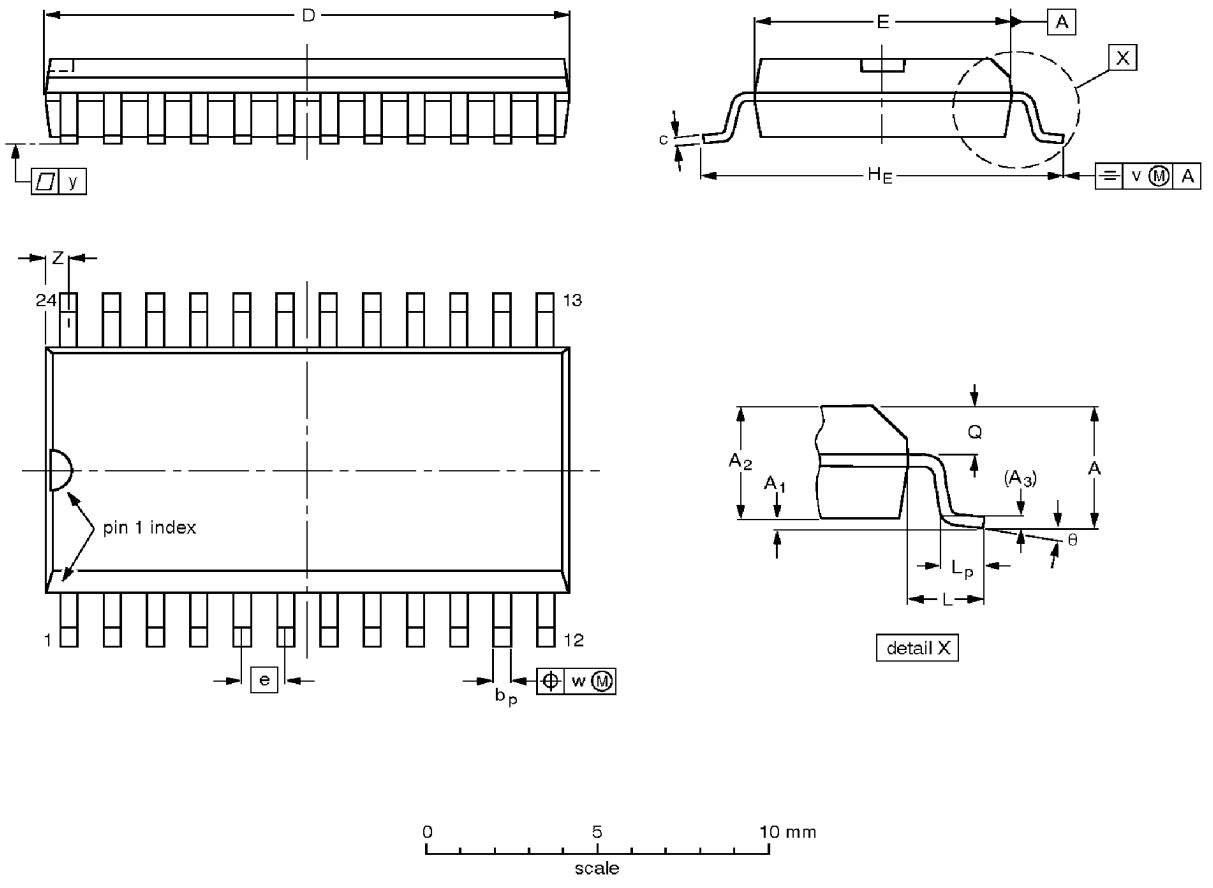


Figure 4. Load circuitry for switching times.

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

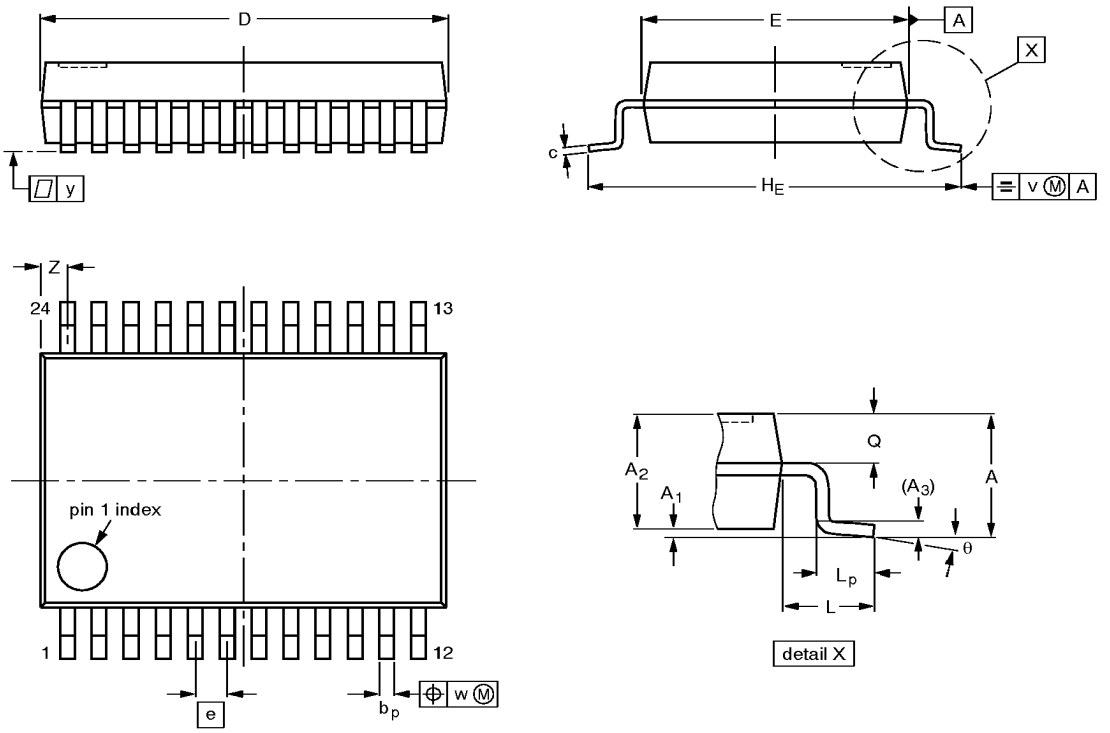
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

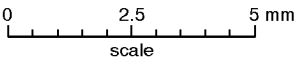
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**





DIMENSIONS (mm are the original dimensions)

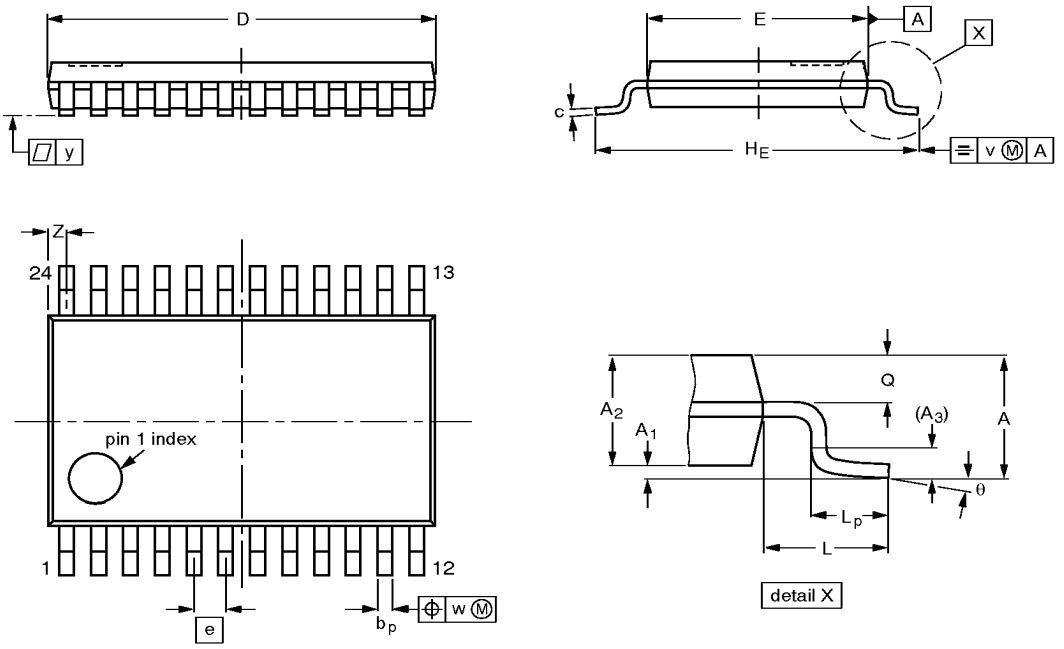
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

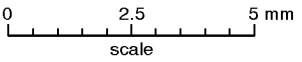
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04