

Octal registered transceiver; 3-state

74LVC2952

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels.
- Inputs accept voltages upto 5.5 V
- Flow-through pin-out architecture
- 3-state outputs
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC2952 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC2952 is an octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the clock (CP_{nn}) provided that the clock enable ($\overline{CE}_{nn}$) is LOW. The data is then present at the 3-state output buffers, but is only accessible when the output enable input ($\overline{OE}_{nn}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

The '952' is identical to the '953' but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f = 2.0\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP_{nn} to A_n, B_n	$C_L = 50\text{ pF}$ $V_{CC} = 3.3\text{ V}$	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_i	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is $V_i = \text{GND to } V_{CC}$.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC2952D	24	SO	plastic	SO24/SOT137A
74LVC2952DB	24	SSOP	plastic	SSOP24/SOT340
74LVC2952PW	24	TSSOP	plastic	TSSOP24/SOT355

PINNING

PIN	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	B_0 to B_7	B data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
9, 15	$\overline{OE}_{AB}, \overline{OE}_{BA}$	output enable inputs (active LOW)
10, 14	CP_{AB}, CP_{BA}	clock inputs
11, 13	$\overline{CE}_{AB}, \overline{CE}_{BA}$	clock enable inputs
16, 17, 18, 19, 20, 21, 22, 23	A_0 to A_7	A data inputs/outputs
24	V_{CC}	positive supply voltage

FUNCTION TABLE for register A_n or B_n

INPUTS			INTERNAL Q	OPERATING MODE
A_n or B_n	CP_{nn}	$\overline{CE}_{nn}$		
X	X	H	NC	Hold data
L	$\uparrow$	L	L	Load data
H	$\uparrow$	L	H	Load data

H = HIGH voltage level
L = LOW voltage level
 $\uparrow$ = Low-to-High transition

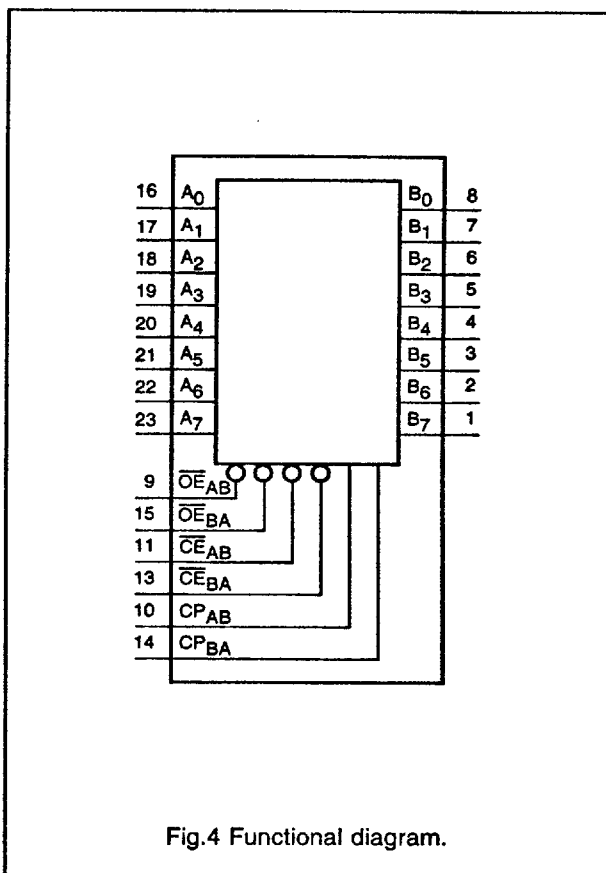
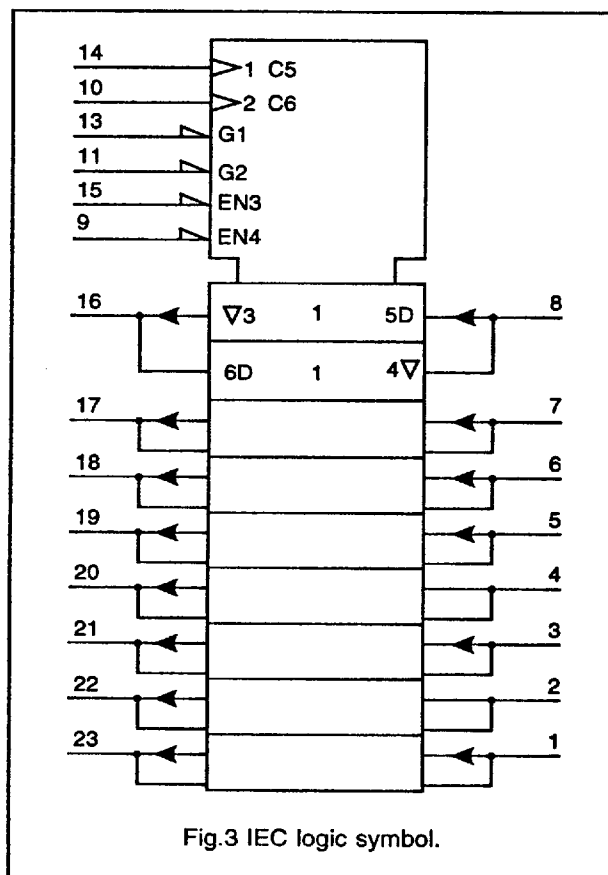
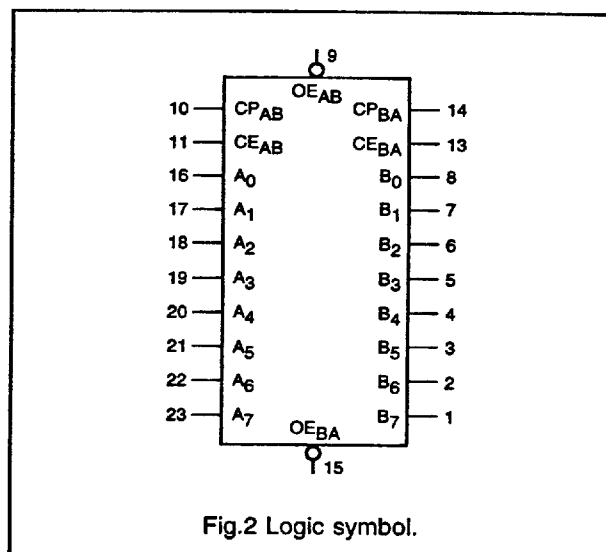
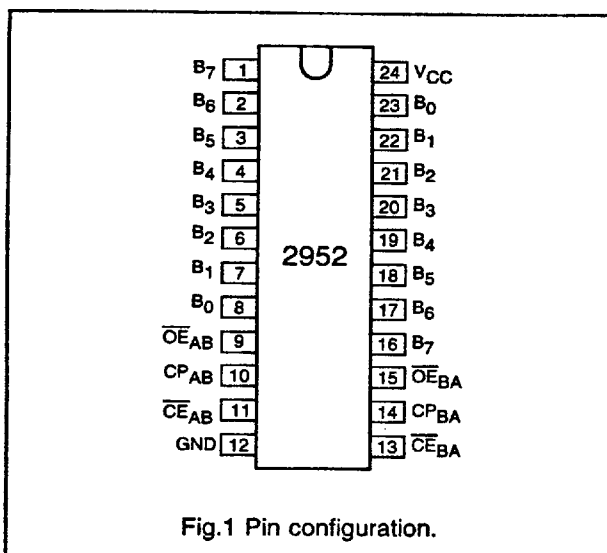
FUNCTION TABLE for output enable

INPUTS $\overline{OE}_{nn}$	INTERNAL Q	A_n or B_n OUTPUTS	OPERATING MODE
H	X	Z	disable outputs
L	L	L	enable outputs
L	H	H	enable outputs

NC = no change
X = don't care
Z = high impedance OFF-state

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DC CHARACTERISTICS FOR 74LVC2952

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC2952

GND = 0 V; $t_r = t_f = 2.5$ ns; $C_L = 50$ pF

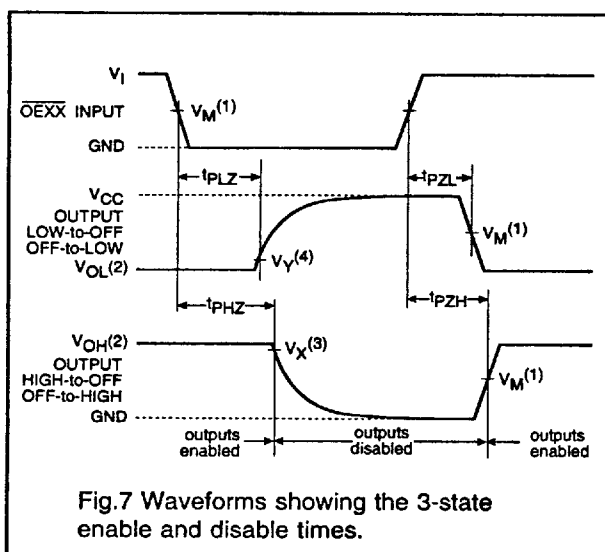
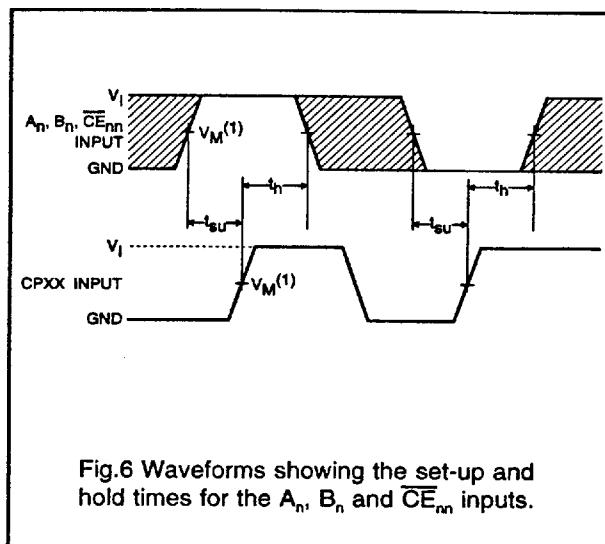
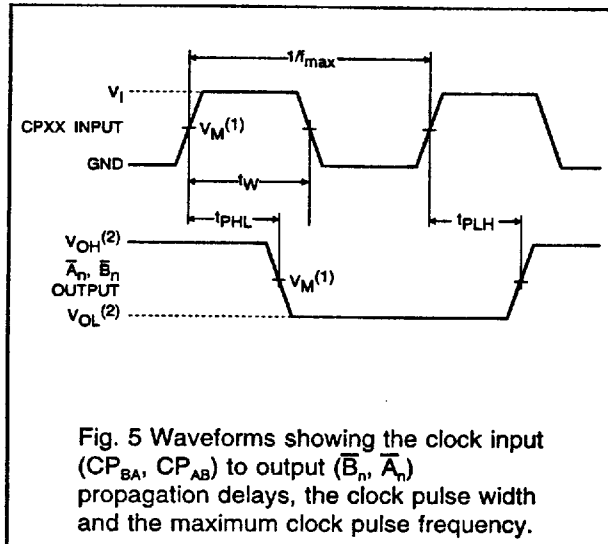
SYMBOL	PARAMETER	T _{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V _{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t _{PHL} /t _{PLH}	propagation delay CP _{BA} , CP _{AB} to A _n , B _n	-	-	-	ns	1.2	Fig.5
		-	-	10		2.7	
		-	3.2*	9.0		3.0 to 3.6	
t _{PZH} /t _{PZL}	3-state output enable time OE _{BA} , OE _{AB} to A _n , B _n	-	-	-	ns	1.2	Fig.7
		-	-	11		2.7	
		-	-	10		3.0 to 3.6	
t _{PHZ} /t _{PLZ}	3-state output disable time OE _{BA} , OE _{AB} to A _n , B _n	-	-	-	ns	1.2	Fig.7
		-	-	10		2.7	
		-	-	9.0		3.0 to 3.6	
t _W	CP _{AB} , CP _{BA} pulse width, HIGH or LOW	3.0	-	-	ns	2.7	Fig.5
		3.0	-	-		3.0 to 3.6	
t _{su}	set-up time, HIGH or LOW A _n , B _n to CP _{AB} , CP _{BA}	-5.0	-	-	ns	2.7	Fig.6
		-5.0	-	-		3.0 to 3.6	
t _{su}	set-up time, HIGH or LOW CE _{AB} , CE _{BA} to CP _{AB} , CP _{BA}	4.0	-	-	ns	2.7	Fig.6
		4.0	-	-		3.0 to 3.6	
t _h	hold time A _n , B _n to CP _{AB} , CP _{BA}	0	-	-	ns	2.7	Fig.6
		0	-	-		3.0 to 3.6	
t _h	hold time CE _{AB} , CE _{BA} to CP _{AB} , CP _{BA}	3.0	-	-	ns	2.7	Fig.6
		3.0	-	-		3.0 to 3.6	
f _{max}	maximum clock pulse frequency	145	-	-	MHz	2.0	Fig.5
		150	-	-		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.* Typical values are measured at V_{CC} = 3.3 V.

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AC WAVEFORMS



Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

- Notes:
- (1) $V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
 - (3) $V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (4) $V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$

