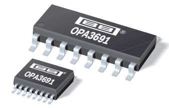


SBOS227 – DECEMBER 2001

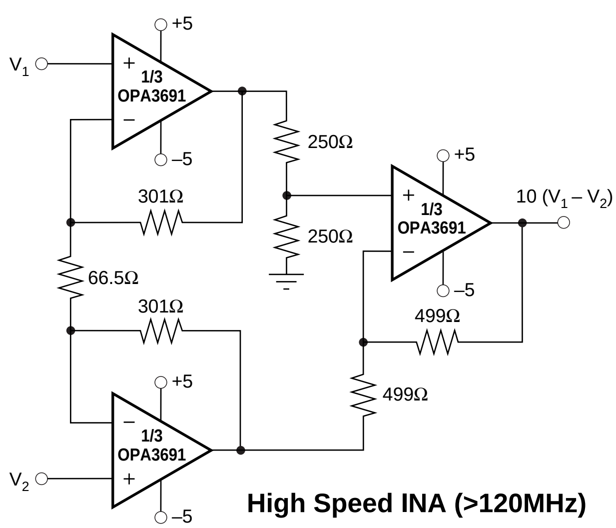
Triple Wideband, Current-Feedback OPERATIONAL AMPLIFIER With Disable

FEATURES

- FLEXIBLE SUPPLY RANGE: +5V to +12V
- UNITY-GAIN STABLE: 400MHz (G = 1)
- HIGH OUTPUT CURRENT: 190mA
- OUTPUT VOLTAGE SWING: ±4.0V
- HIGH SLEW RATE: 2100V/µs
- LOW SUPPLY CURRENT: 5.1mA/ch
- LOW DISABLED CURRENT: 150µA/ch
- IMPROVED HIGH FREQUENCY PINOUT
- WIDEBAND +5V OPERATION: 230MHz (G = +2)

APPLICATIONS

- RGB AMPLIFIERS
- WIDEBAND INA
- BROADBAND VIDEO BUFFERS
- HIGH SPEED IMAGING CHANNELS
- PORTABLE INSTRUMENTS
- ADC BUFFERS
- ACTIVE FILTERS
- CABLE DRIVERS



High Speed INA (>120MHz)

DESCRIPTION

The OPA3691 sets a new level of performance for broadband triple current-feedback op amps. Operating on a very low 5.1mA/ch supply current, the OPA3691 offers a slew rate and output power normally associated with a much higher supply current. A new output stage architecture delivers a high output current with minimal voltage headroom and crossover distortion. This gives exceptional single-supply operation. Using a single +5V supply, the OPA3691 can deliver a 1V to 4V output swing with over 120mA drive current and 150MHz bandwidth. This combination of features makes the OPA3691 an ideal RGB line driver or single-supply Analog-to-Digital Converter (ADC) input driver.

The OPA3691's low 5.1mA/ch supply current is precisely trimmed at 25°C. This trim, along with low drift over temperature, ensures lower maximum supply current than competing products. System power may be further reduced by using the optional disable control pin. Leaving this disable pin open, or holding it HIGH, gives normal operation. If pulled LOW, the OPA3691 supply current drops to less than 150µA/ch while the output goes into a high impedance state. This feature may be used for power savings.

OPA3691 RELATED PRODUCTS

	SINGLES	DUALS	TRIPLES
Voltage Feedback	OPA690	OPA2690	OPA3690
Current Feedback	OPA691	OPA2691	OPA3681
Fixed Gain	OPA692	OPA2682	OPA3692

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	±6.5VDC
Internal Power Dissipation(2)	See Thermal Information
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: ID, IDBQ	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+175°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

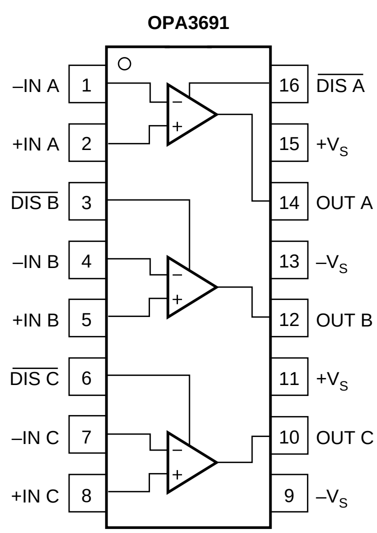
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	TEMPERATURE RANGE	SPECIFIED PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA3691IDBQ	SSOP-16 Surface-Mount	DBQ	–40°C to +85°C	OPA3691	OPA3691IDBQT	Tape and Reel, 250
"	"	"	"	"	OPA3691IDBQR	Tape and Reel, 2500
OPA3691ID(2)	SO-16 Surface-Mount	D	–40°C to +85°C	OPA3691	OPA3691ID	Rails, 48
"	"	"	"	"	OPA3691IDR	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com. (2) OPA3691ID available Q1 2002.

PIN CONFIGURATION

Top View **SSOP-16, SO-16**



ELECTRICAL CHARACTERISTICS: $V_S = \pm5V$

$R_F = 499\Omega$, $R_L = 100\Omega$, and G = +2, (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA3691ID, IDBQ TYP +25°C	MIN/MAX OVER TEMPERATURE +25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth (V_O = 0.5Vp-p)	G = +1, $R_F = 549\Omega$	400				MHz	typ	C
	G = +2, $R_F = 499\Omega$	350				MHz	typ	C
	G = +5, $R_F = 365\Omega$	320				MHz	typ	C
	G = +10, $R_F = 182\Omega$	200				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O = 0.5Vp-p	35				MHz	typ	C
Peaking at a Gain of +1	R_F = 453, V_O = 0.5Vp-p	1				dB	typ	C
Large Signal Bandwidth	G = +2, V_O = 5Vp-p	300				MHz	typ	C
Slew Rate	G = +2, 4V Step	2100				V/µs	typ	C
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	1.7				ns	typ	C
	G = +2, 5V Step	2.0				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	14				ns	typ	C
0.1%	G = +2, V_O = 2V Step	10				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2Vp-p							
2nd Harmonic	$R_L = 100\Omega$	–71				dBc	typ	C
	$R_L \geq 500\Omega$	–80				dBc	typ	C
3rd Harmonic	$R_L = 100\Omega$	–76				dBc	typ	C
	$R_L \geq 500\Omega$	–92				dBc	typ	C
Input Voltage Noise	f > 1MHz	2.2				$nV/\sqrt{Hz}$	typ	C
Noninverting Input Current Noise	f > 1MHz	12				$pA/\sqrt{Hz}$	typ	C
Inverting Input Current Noise	f > 1MHz	15				$pA/\sqrt{Hz}$	typ	C
Differential Gain	G = +2, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$	0.001				%	typ	C
	$R_L = 37.5\Omega$	0.008				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$	0.01				deg	typ	C
	$R_L = 37.5\Omega$	0.05				deg	typ	C
Crosstalk	Input Referred, f = 5MHz, All Hostile	–55				dBc	typ	C
DC PERFORMANCE[4]								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = 0V, $R_L = 100\Omega$	225	**125**	110	100	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±0.8	**±3**	±3.7	±4.3	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±12	±20	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	+15	**+35**	+43	+45	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V			–300	–300	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±5	**±25**	±30	±40	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V			±90	±200	nA°/C	max	B
INPUT								
Common-Mode Input Range[5]		±3.5	**±3.4**	±3.3	±3.2	V	min	A
Common-Mode Rejection (CMRR)	V_{CM} = 0V	56	**52**	51	50	dB	min	A
Noninverting Input Impedance		100 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open Loop	37				Ω	typ	C
OUTPUT								
Voltage Output Swing	No Load	±4.0	**±3.8**	±3.7	±3.6	V	min	A
	$R_L = 100\Omega$	±3.9	**±3.7**	±3.6	±3.3	V	min	A
Current Output, Sourcing	V_O = 0	+190	**+160**	+140	+100	mA	min	A
Current Output, Sinking	V_O = 0	–190	**–160**	–140	–100	mA	min	A
Short-Circuit Current	V_O = 0	±250				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.03				Ω	typ	C
DISABLE (Disabled LOW)								
Power-Down Supply Current ($+V_S$)	$V_{\overline{DIS}}$ = 0, All Channels	–450	**–900**	–1050	–1200	µA	max	A
Disable Time		100				ns	typ	C
Enable Time		25				ns	typ	C
Off Isolation	G = +2, 5MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn On Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±50				mV	typ	C
Turn Off Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0, Each Channel	75	**130**	150	160	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6**	±6	±6	V	max	A
Max Quiescent Current (3 Channels)	$V_S = \pm5V$	15.3	**15.9**	16.5	17.1	mA	max	A
Min Quiescent Current (3 Channels)	$V_S = \pm5V$	15.3	**14.7**	14.1	13.5	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input Referred	58	52	50	49	dB	min	A
TEMPERATURE RANGE								
Specification: D, DBQ		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
DBQ SSOP-16		100				°C/W	typ	C
D SO-16		100				°C/W	typ	C

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction temperature = ambient for 25°C specifications. (3) Junction temperature = ambient at low temperature limit: Junction temperature = ambient +15°C at high temperature limit for over temperature specifications. (4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

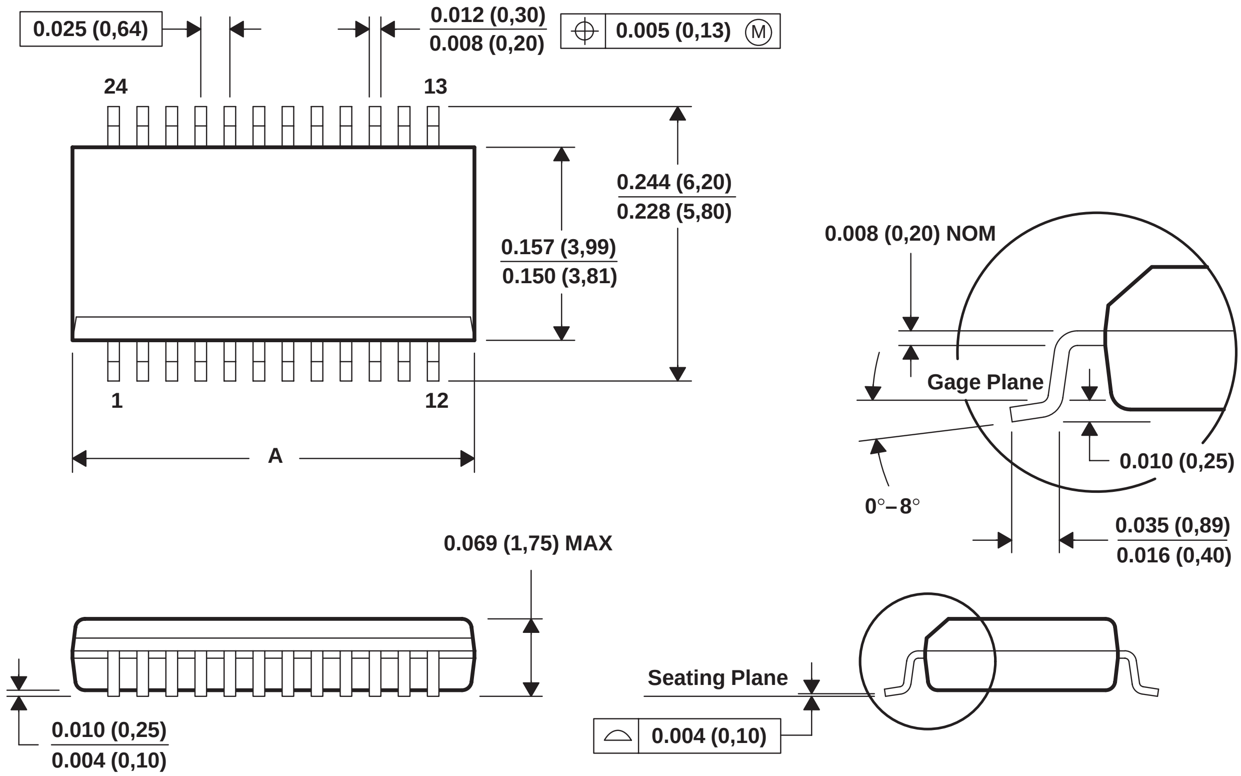
R_F = 499Ω, R_L = 100Ω to $V_S/2$, G = +2, (see Figure 2 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA3691ID, IDBQ TYP +25°C	MIN/MAX OVER TEMPERATURE +25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)	UNITS	MIN/MAX	TEST LEVEL(1)
AC PERFORMANCE (see Figure 2)								
Small-Signal Bandwidth (V_O = 0.5Vp-p)	G = +1, R_F = 549Ω	250				MHz	typ	C
	G = +2, R_F = 499Ω	230				MHz	typ	C
	G = +5, R_F = 365Ω	215				MHz	typ	C
	G = +10, R_F = 182Ω	171				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5Vp-p	35				MHz	typ	C
Peaking at a Gain of +1	R_F = 649Ω, V_O < 0.5Vp-p	0.4				dB	typ	C
Large Signal Bandwidth	G = +2, V_O = 2Vp-p	300				MHz	typ	C
Slew Rate	G = +2, 2V Step	850				V/µs	typ	C
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	1.5				ns	typ	C
	G = +2, V_O = 2V Step	2.0				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	16				ns	typ	C
0.1%	G = +2, V_O = 2V Step	12				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2Vp-p							
2nd Harmonic	R_L = 100Ω to $V_S/2$	–68				dBc	typ	C
	R_L ≥ 500Ω to $V_S/2$	–75				dBc	typ	C
3rd Harmonic	R_L = 100Ω to $V_S/2$	–71				dBc	typ	C
	R_L ≥ 500Ω to $V_S/2$	–79				dBc	typ	C
Input Voltage Noise	f > 1MHz	2.2				$nV/\sqrt{Hz}$	typ	C
Noninverting Input Current Noise	f > 1MHz	12				$pA/\sqrt{Hz}$	typ	C
Inverting Input Current Noise	f > 1MHz	15				$pA/\sqrt{Hz}$	typ	C
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = $V_S/2$, R_L = 100Ω to $V_S/2$	200	**100**	90	80	kΩ	min	A
Input Offset Voltage	V_{CM} = 2.5V	±0.8	**±3.5**	±4.1	±4.8	mV	max	A
Average Offset Voltage Drift	V_{CM} = 2.5V			±12	±20	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 2.5V	+20	**+40**	+46	+56	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 2.5V			–250	–250	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 2.5V	±5	**±20**	±25	±35	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 2.5V			±112	±200	nA/°C	max	B
INPUT								
Least Positive Input Voltage(5)		1.5	**1.6**	1.7	1.8	V	max	A
Most Positive Input Voltage(5)		3.5	**3.4**	3.3	3.2	V	min	A
Common-Mode Rejection (CMRR)	V_{CM} = $V_S/2$	54	**50**	49	48	dB	min	A
Noninverting Input Impedance		100 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open Loop	40				Ω	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	4	**3.8**	3.7	3.5	V	min	A
	R_L = 100Ω, 2.5V	3.9	**3.7**	3.6	3.4	V	min	A
Least Positive Output Voltage	No Load	1	**1.2**	1.3	1.5	V	max	A
	R_L = 100Ω, 2.5V	1.1	**1.3**	1.4	1.6	V	max	A
Current Output, Sourcing	V_O = $V_S/2$	+160	**+120**	+100	+80	mA	min	A
Current Output, Sinking	V_O = $V_S/2$	–160	**–120**	–100	–80	mA	min	A
Short-Circuit Current	V_O = $V_S/2$	250				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.03				Ω	typ	C
DISABLE (Disabled LOW)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, All Channels	–450	**–900**	–1050	–1200	µA	max	A
Disable Time		100				ns	typ	C
Enable Time		25				ns	typ	C
Off Isolation	G = +2, 5MHz	65				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn On Glitch	G = +2, R_L = 150Ω, V_{IN} = $V_S/2$	±50				mV	typ	C
Turn Off Glitch	G = +2, R_L = 150Ω, V_{IN} = $V_S/2$	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0, Each Channel	75	130	150	160	µA	typ	C
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Maximum Single-Supply Operating Voltage			**12**	12	12	V	max	A
Max Quiescent Current (3 Channels)	V_S = +5V	13.5	**14.4**	15.0	15.6	mA	max	A
Min Quiescent Current (3 Channels)	V_S = +5V	13.5	**12.3**	12	11.4	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input Referred	55				dB	typ	C
TEMPERATURE RANGE								
Specification: D, DBQ		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
DBQ SSOP-16		100				°C/W	typ	C
D SO-16		100				°C/W	typ	C

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction temperature = ambient for 25°C specifications. (3) Junction temperature = ambient at low temperature limit: Junction temperature = ambient +15°C at high temperature limit for over temperature specifications. (4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

DBQ (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



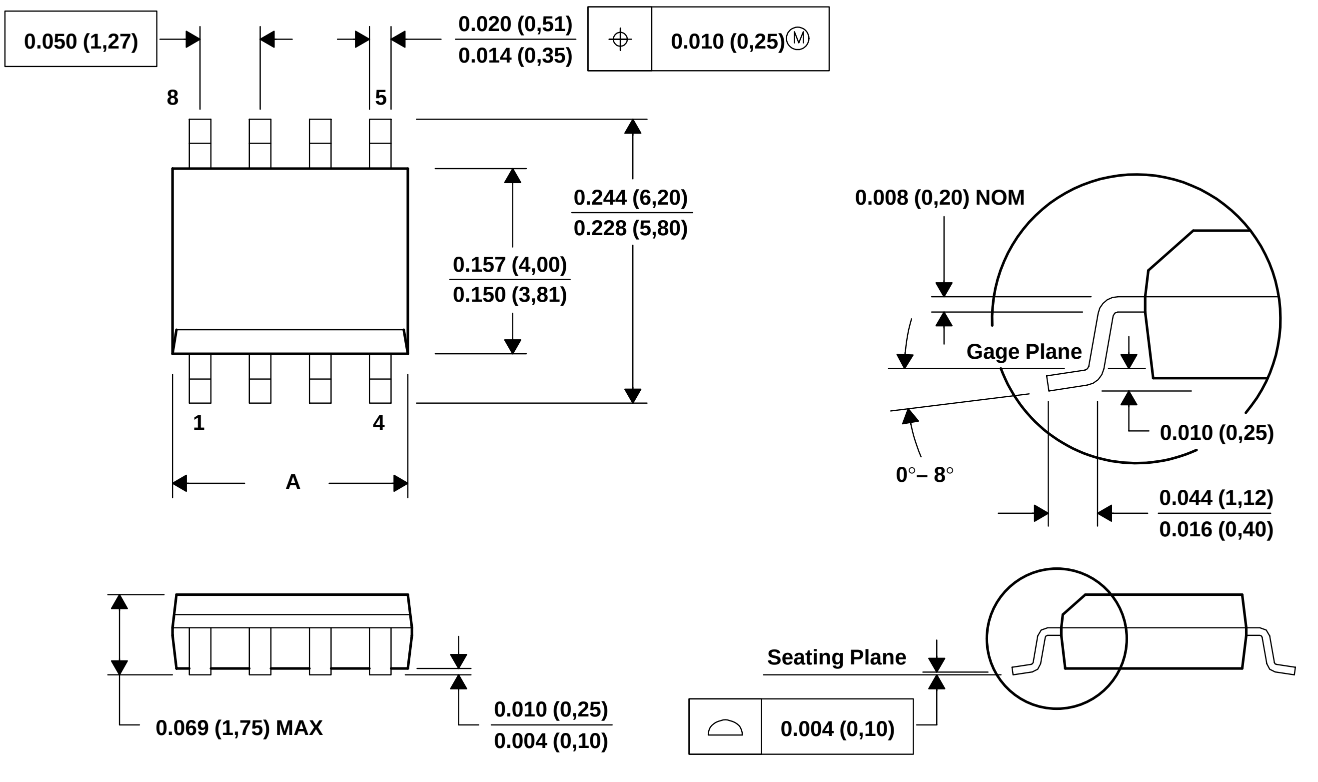
PINS ** / DIM	16	20	24	28
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.188 (4,78)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)

4073301/E 10/00

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-137

D (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

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