Octal bus transceiver/register; 3-state; inverting — 74LVC648

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Flow-through pin-out architecture**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**

DESCRIPTION

The 74LVC648 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC648 consist of 8 inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropiate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both.The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

The '648' is functionally identical to the '646', but has inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $\overline{B}_n$, $\overline{A}_n$	C_L = 50 pF V_{CC} = 3.3 V	5.0	ns
f_{max}	maximum clock frequency		150	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PACKAGE	MATERIAL	CODE
74LVC648D	24	SO	plastic	SO24/SOT137A
74LVC648DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	CP_{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)
2	S_{AB}	select 'A' to 'B' source input
3	DIR	direction control input
4, 5, 6, 7, 8, 9, 10, 11	$\overline{A}_0$ to $\overline{A}_7$	'A' data inputs/outputs
12	GND	ground (0 V)
20, 19, 18, 17, 16,15, 14, 13	$\overline{B}_0$ to $\overline{B}_7$	'B' data inputs/outputs
21	$\overline{OE}$	output enable input (active LOW)
22	S_{BA}	select 'B' to 'A' source input
23	CP_{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
24	V_{CC}	positive supply voltage

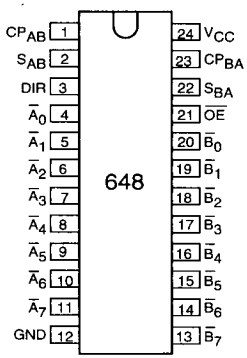


Fig.1 Pin configuration.

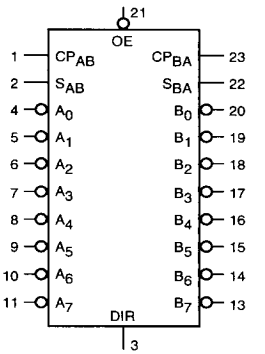


Fig.2 Logic symbol.

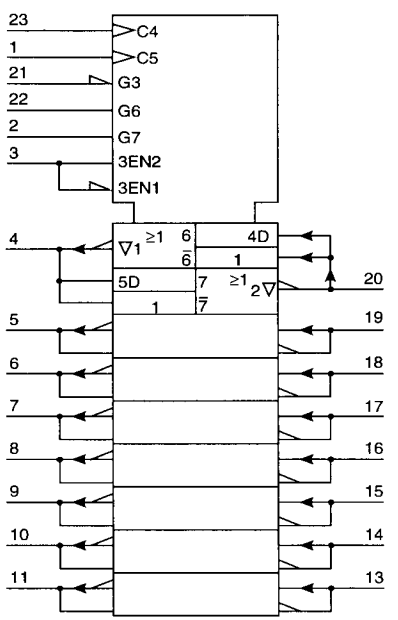


Fig3. IEC logic symbol.

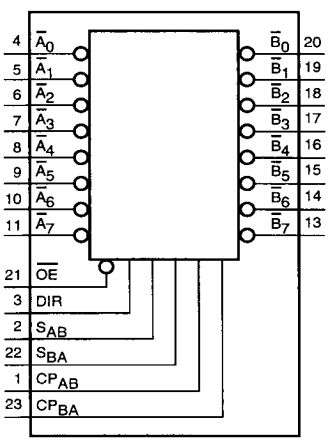


Fig.4 Functional diagram.

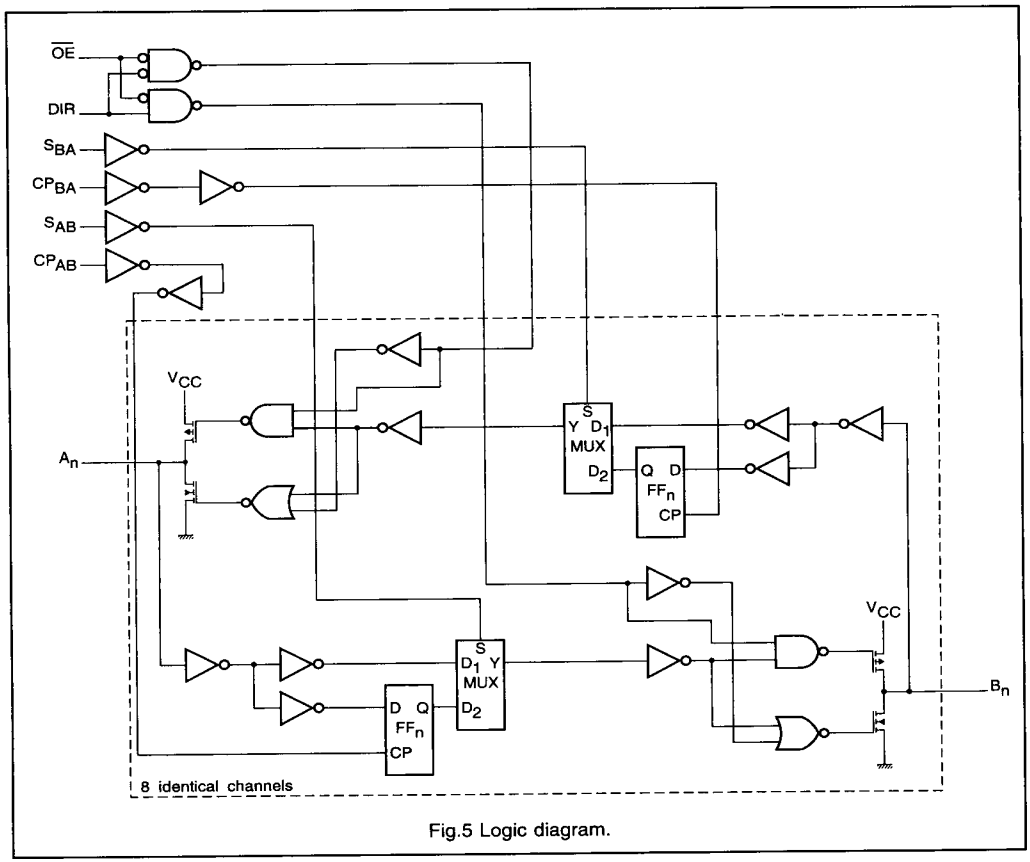


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ to $\overline{A}_7$	$\overline{B}_0$ to $\overline{B}_7$	
X X	X X	↑ X	X ↑	X X	X X	input un*	un* input	store A, B unspecified* store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	store A and B data, isolation hold storage
L L	L L	X X	X H or L	X X	L H	output	input	real-time $\overline{B}$ data to A bus stored $\overline{B}$ data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time $\overline{A}$ data to B bus stored $\overline{A}$ data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

DC CHARACTERISTICS FOR 74LVC648

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC648

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $\overline{B}_n$, $\overline{A}_n$	1.5 1.5 1.5	25 6.0 4.9*	– 10 8.3	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to $\overline{B}_n$, $\overline{A}_n$	1.5 1.5 1.5	26 6.0 5.2*	– 11 8.9	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to $\overline{B}_n$, $\overline{A}_n$	1.5 1.5 1.5	27 6.4 5.2*	– 11 8.8	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{A}_n$, $\overline{B}_n$	1.5 1.5 1.5	21 5.3 4.3*	– 9.5 8.5	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{A}_n$, $\overline{B}_n$	1.5 1.5 1.5	16 4.3 3.8*	– 8.5 8.0	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PZH}/t_{PZL}	3-state output enable time DIR to $\overline{A}_n$, $\overline{B}_n$	1.5 1.5 1.5	21 5.3 4.3	– 9.6 6.8	ns	1.2 2.7 3.0 to 3.6	Fig.10
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to $\overline{A}_n$, $\overline{B}_n$	1.5 1.5 1.5	16 4.3 4.0	– 7.9 5.7	ns	1.2 2.7 3.0 to 3.6	Fig.10
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	– –	3.0 3.0*	– –	ns	2.7 3.0 to 3.6	Figs 6 and 8
t_{su}	set-up time A_n, B_n to CP_{AB}, CP_{BA}	1.0 1.0	– –	– –	ns	2.7 3.0 to 3.6	Fig.7
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	0.0 0.0	– –	– –	ns	2.7 3.0 to 3.6	Fig.7
f_{max}	maximum clock pulse frequency	– 75	– 150*	– –	ns	2.7 3.0 to 3.6	Fig.7

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

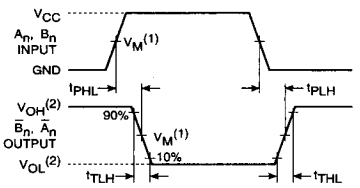


Fig.6 Waveforms showing the input A_n, B_n to output $\overline{B}_n$, $\overline{A}_n$ propagation delays and the output transition times.

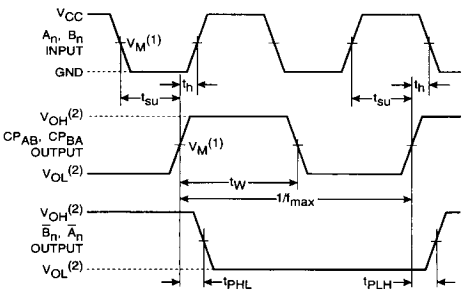


Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output $\overline{B}_n$, $\overline{A}_n$ propagation delays.

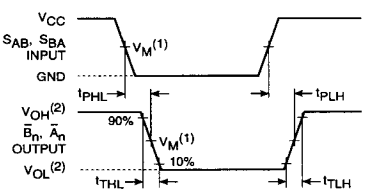


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output $\overline{B}_n$, $\overline{A}_n$ propagation delay times and output transition times.

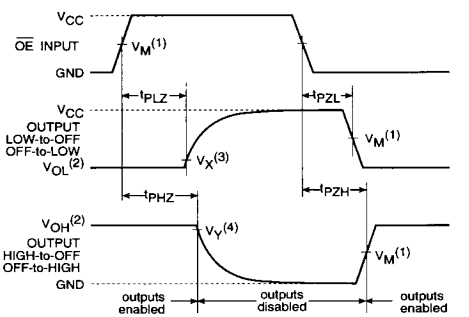


Fig.9 Waveforms showing the input $\overline{OE}$ to output $\overline{A}_n$, $\overline{B}_n$ 3-state enable and disable times.

Notes:
(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

AC WAVEFORMS *(Continued)*

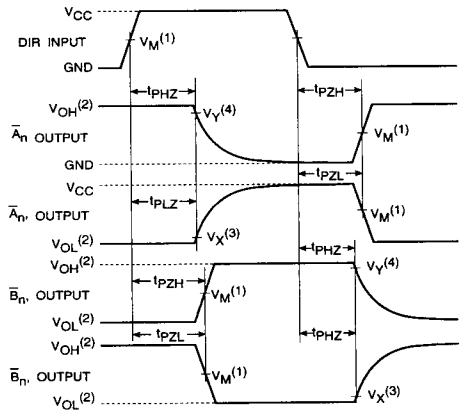
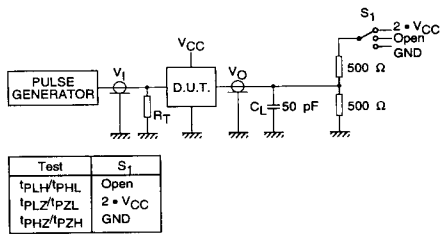


Fig.10 Waveforms showing the input DIR to output $\overline{A}_n$, $\overline{B}_n$ 3-state enable and disable times.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

Fig.11 Load cicuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

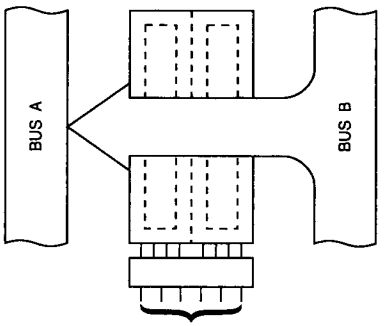
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

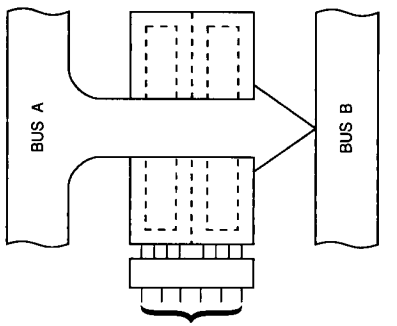
APPLICATION INFORMATION

Real-time transfer; bus B to bus $\overline{A}$



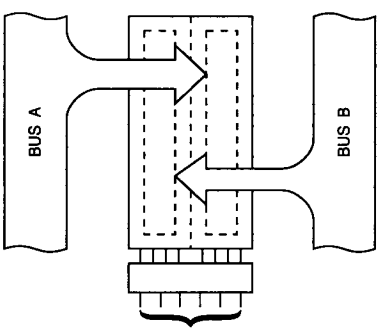
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus $\overline{B}$



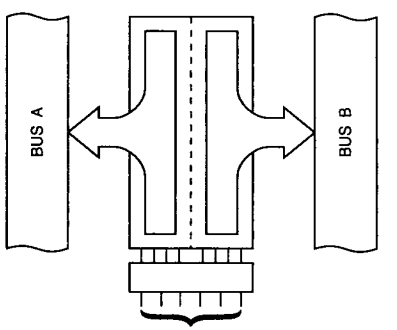
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	H	X	X	L	X

Storage from A, B or A and B



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Transfer storage data to $\overline{A}$ or $\overline{B}$



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	H or L	X	H
L	H	H or L	X	H	X