

Octal transceiver/register with dual enable; 3-state; inverting

74LVC651

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Flow-through pin-out architecture
- Inputs accept voltages upto 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC651 is a high-performance, low-power, high-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC651 consist of 8 inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the "A" or "B" or both buses, will be stored in the internal registers, at the appropriate clock inputs (CP_{AB} or CP_{BA}) regardless of the select inputs (S_{AB} and S_{BA}) or output enable (OE_{AB} and OE_{BA}) control inputs. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OE_n inputs this operating mode permits. The output enable inputs OE_{AB} and OE_{BA} determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from A_n to B_n is possible and when OE_{BA} is HIGH, there is no data transmission from B_n to A_n possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and OE_{BA}. In this configuration each output reinforces its input.

The '651' is functionally identical to the '652', but has inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f ≤ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PHL} /t _{PLH}	propagation delay A _n , B _n to B _n , A _n	C _L = 50 pF V _{CC} = 3.3 V	5.0	ns
f _{max}	maximum clock frequency		150	MHz
C _I	input capacitance		3.0	pF
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_i = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC651D	24	SO	plastic	SO24/SOT137A
74LVC651DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	CP _{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)
2	S _{AB}	select 'A' to 'B' source input
3	OE _{AB}	output enable B to A input (active LOW)
4, 5, 6, 7, 8, 9, 10, 11	A ₀ to A ₇	'A' data inputs/outputs
12	GND	ground (0 V)
20, 19, 18, 17, 16, 15, 14, 13	B ₀ to B ₇	'B' data inputs/outputs
21	OE _{BA}	output enable A to B input
22	S _{BA}	select 'B' to 'A' source input
23	CP _{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
24	V _{CC}	positive supply voltage

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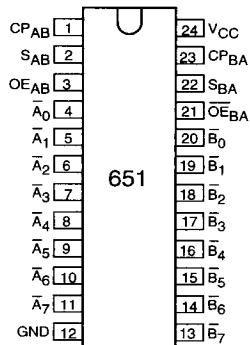


Fig.1 Pin configuration.

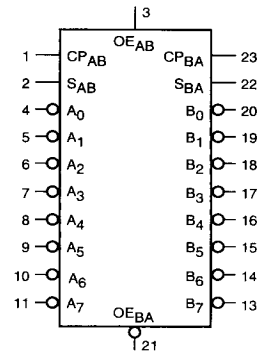


Fig.2 Logic symbol.

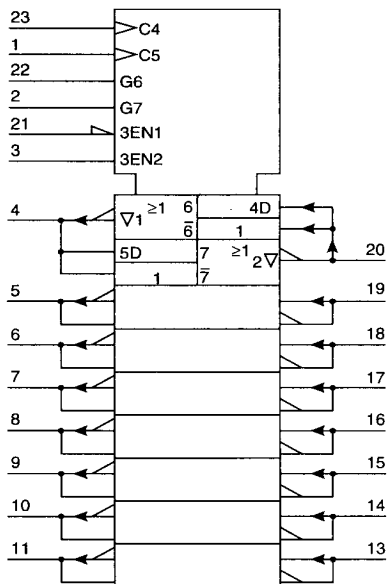


Fig.3. IEC logic symbol.

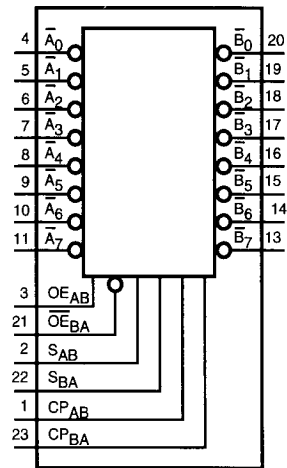
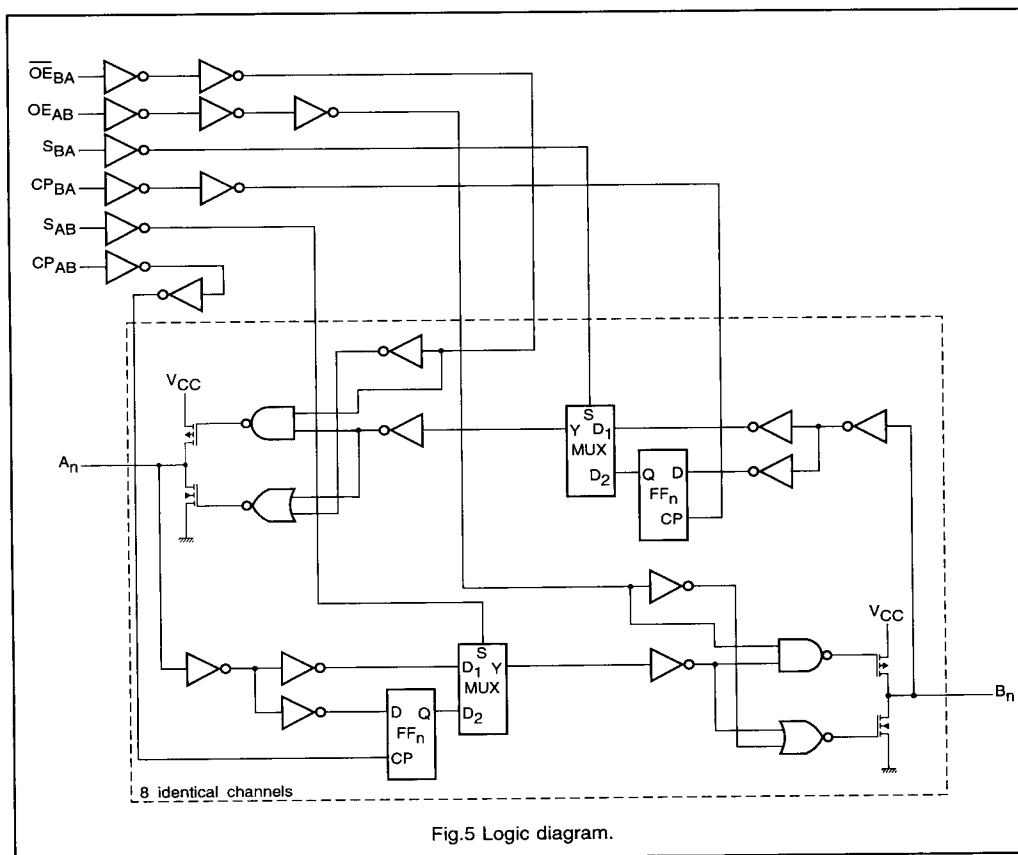


Fig.4 Functional diagram.

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FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE _{AB}	OE _{BA}	CP _{AB}	CP _{BA}	S _{AB}	S _{BA}	A ₀ to A ₇	B ₀ to B ₇	
L L	H H	H or L ↑	H or L ↑	X X	X X	input	input	isolation store A and B data
X H	H H	↑ ↑	H or L ↑	X L	X X	input input	un* output	store A, hold B store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X L	un* output	input input	hold A, store B store B in both registers
L L	L L	X X	X H or L	X X	L H	output	input	real time B data to A bus stored B data to A bus
H H	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and OE_{BA} inputs. Data input functions are always enabled,

i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

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DC CHARACTERISTICS FOR 74LVC651

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC651GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

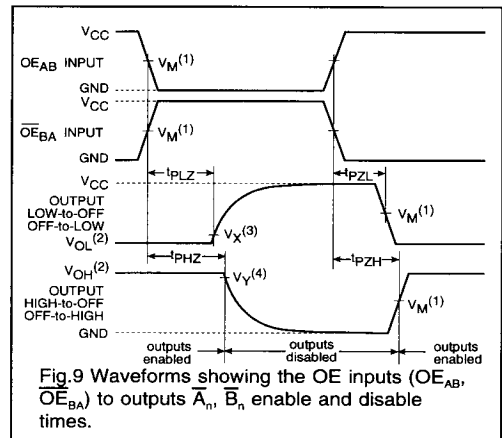
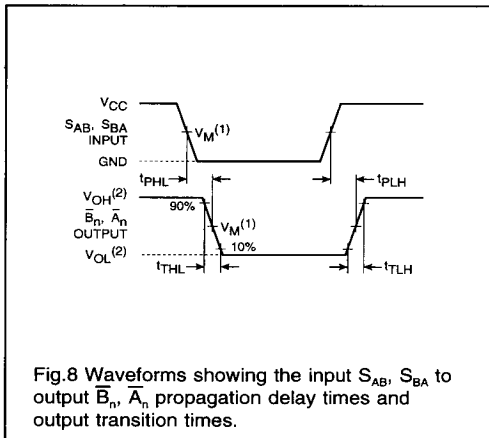
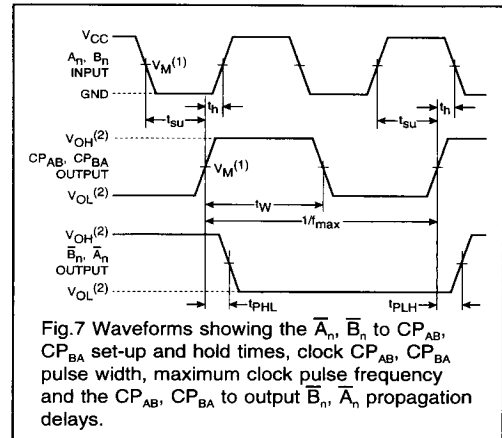
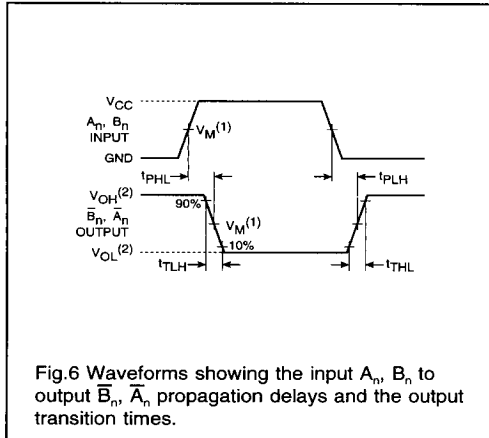
SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $\overline{B}_n, \overline{A}_n$	1.5 1.5 1.5	25 6.0 4.9*	— 10 8.3	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to $\overline{B}_n, \overline{A}_n$	1.5 1.5 1.5	26 6.0 5.2*	— 11 8.9	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to $\overline{B}_n, \overline{A}_n$	1.5 1.5 1.5	27 6.4 5.2*	— 11 8.8	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB} to $\overline{B}_n$	1.5 1.5 1.5	20 6.0 4.8*	— 10 8.0	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB} to $\overline{B}_n$	1.5 1.5 1.5	20 5.3 4.4*	— 10 8.0	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$	1.5 1.5 1.5	20 6.0 4.8*	— 10 8.0	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$	1.5 1.5 1.5	10 5.3 4.4*	— 10 8.0	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	— —	3.0 3.0*	— —	ns	2.7 3.0 to 3.6	Figs 6 and 8
t_{SU}	set-up time $\overline{A}_n, \overline{B}_n$ to CP_{AB}, CP_{BA}	1.0 1.0	— —	— —	ns	2.7 3.0 to 3.6	Fig.7
t_H	hold time $\overline{A}_n, \overline{B}_n$ to CP_{AB}, CP_{BA}	1.0 1.0	— —	— —	ns	2.7 3.0 to 3.6	Fig.7
f_{max}	maximum clock pulse frequency	— 75	— 150*	— —	MHz	2.7 3.0 to 3.6	Fig.7

Notes: All typical values are measured at $T_{amb} = 25$ °C.* Typical values are measured at $V_{CC} = 3.3$ V.

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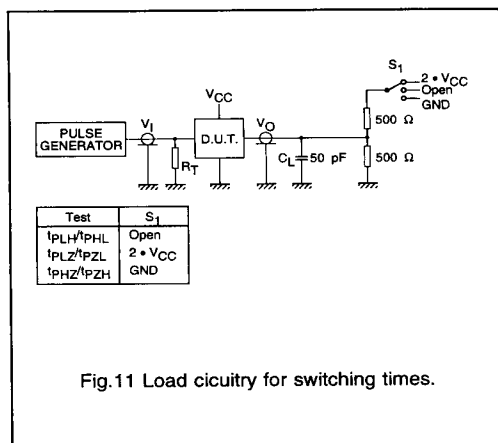
AC WAVEFORMS



- Notes:**
- (1) $V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
 - (3) $V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (4) $V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$

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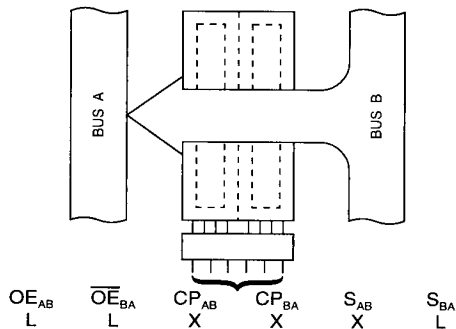


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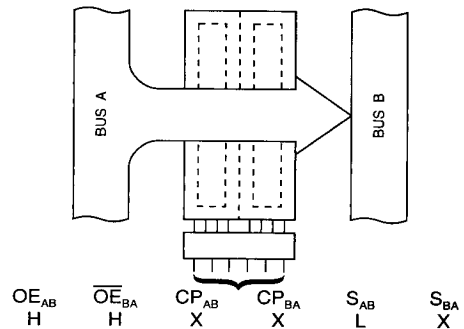
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APPLICATION INFORMATION

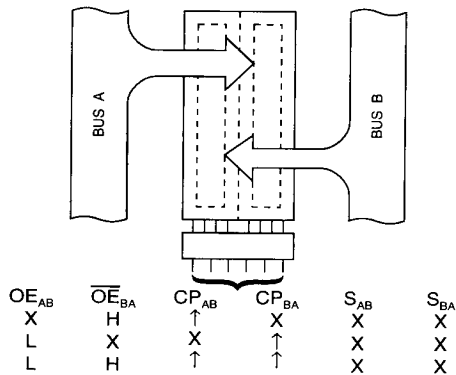
Real-time transfer; bus B to bus A



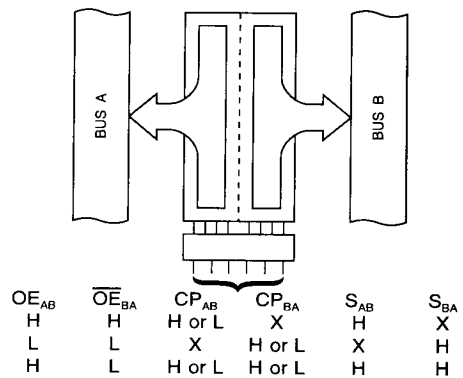
Real-time transfer; bus A to bus B



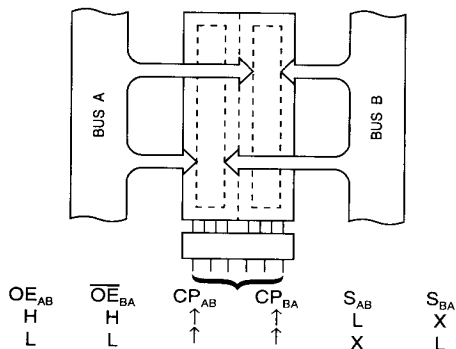
Store A, B or A and B in one register



Transfer A stored data to B bus or B stored data to A bus or both at the same time



Store bus A in both registers or store bus B in both registers



Isolation

