

Dual D-type flip-flop with set and reset;
positive-edge trigger

74LVC74A

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC74A is a high-performance, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC74A is a dual positive edge triggered, D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt-trigger action in all data inputs makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; t_r = t_f ≤ 2.5 ns

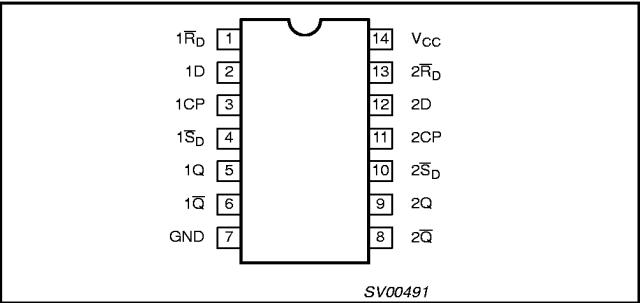
SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PHL} /t _{PLH}	Propagation delay	C _L = 50 pF; V _{CC} = 3.3 V	3.6 3.5 3.5	ns
	nCP to nQ, n $\overline{Q}$			
	n $\overline{S}_D$ to nQ, n $\overline{Q}$			
	n $\overline{R}_D$ to nQ, n $\overline{Q}$			
f _{max}	Maximum clock frequency		250	MHz
C _I	Input capacitance		5.0	pF
C _{PD}	Power dissipation capacitance per flip-flop	Notes NO TAG and NO TAG	30	pF

- NOTES:
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) + \sum (V_O^2/R_L) \times \text{duty factor LOW}$, where:
f_i = input frequency in MHz; C_L = output load capacity in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
 2. The condition is V_I = GND to V_{CC}.

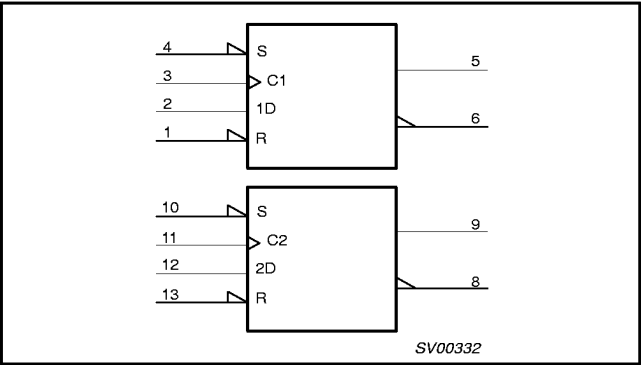
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	−40°C to +85°C	74LVC74A D	74LVC74A D	SOT108-1
14-Pin Plastic SSOP Type II	−40°C to +85°C	74LVC74A DB	74LVC74A DB	SOT337-1
14-Pin Plastic TSSOP Type I	−40°C to +85°C	74LVC74A PW	74LVC74APW DH	SOT402-1

PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



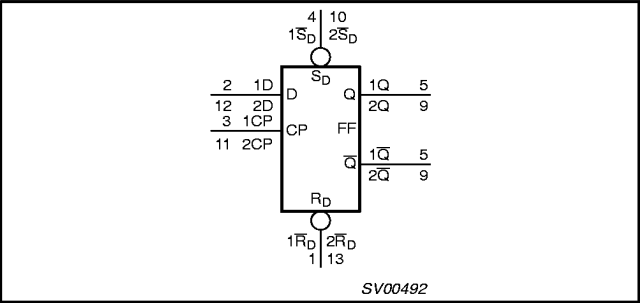
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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 13	1R _D , 2R _D	Asynchronous reset-direct input (active LOW)
2, 12	1D, 2D	Data inputs
3, 11	1CP, 2CP	Clock input (LOW-to-HIGH, edge triggered)
4, 10	1S _D , 2S _D	Asynchronous set-direct input (active LOW)
5, 9	1Q, 2Q	True flip-flop outputs
6, 8	1Q̄, 2Q̄	Complement flip-flop outputs
7	GND	Ground (0 V)
14	V _{CC}	Positive supply voltage

LOGIC SYMBOL



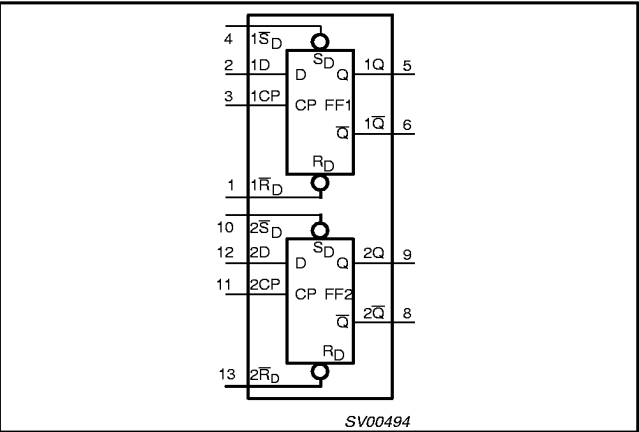
FUNCTION TABLE

INPUTS				OUTPUTS	
S _D	R _D	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

INPUTS				OUTPUTS	
S _D	R _D	CP	D	Q _{n+1}	Q̄ _{n+1}
H	H	↑	L	L	H
H	H	↑	H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition

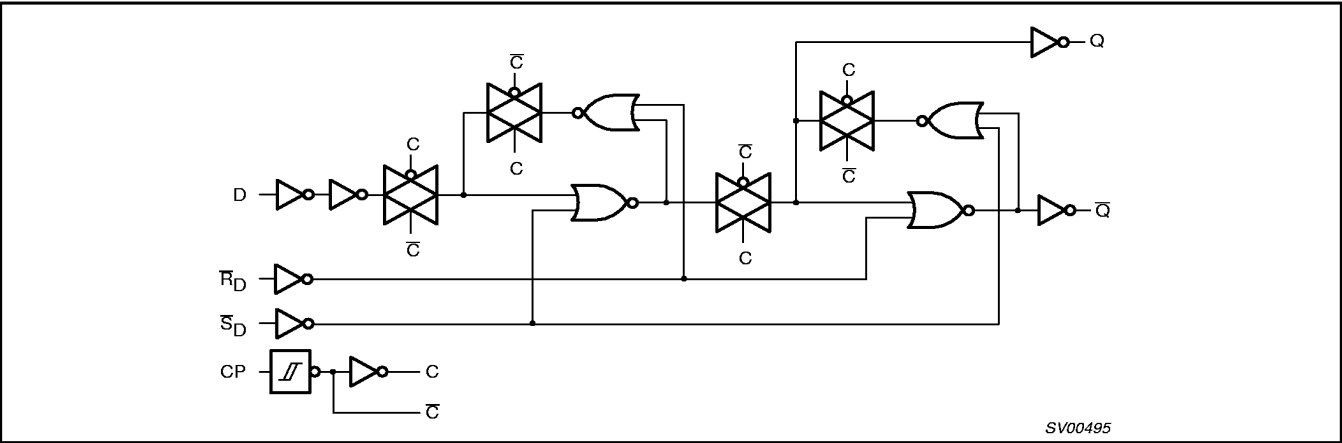
FUNCTIONAL DIAGRAM



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LOGIC DIAGRAM (ONE FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V _{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V _I	DC input voltage range		0	5.5	V
V _O	DC output voltage range		0	V _{CC}	V
T _{amb}	Operating free-air temperature range		−40	+85	°C
t _r , t _f	Input rise and fall times	V _{CC} = 1.2 to 2.7V	0	20	ns/V
		V _{CC} = 2.7 to 3.6V	0	10	

ABSOLUTE MAXIMUM RATINGSNO TAG

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		−0.5 to +6.5	V
I _{IK}	DC input diode current	V _I < 0	−50	mA
V _I	DC input voltage	Note NO TAG	−0.5 to +5.5	V
I _{OK}	DC output diode current	V _O > V _{CC} or V _O < 0	± 50	mA
V _O	DC output voltage	Note NO TAG	−0.5 to V _{CC} + 0.5	V
I _O	DC output source or sink current	V _O = 0 to V _{CC}	± 50	mA
I _{GND} , I _{CC}	DC V _{CC} or GND current		± 100	mA
T _{stg}	Storage temperature range		−65 to +150	°C
P _{TOT}	Power dissipation per package			mW
	– plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP1	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}			V
		V _{CC} = 2.7 to 3.6V	2.0			
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			GND	V
		V _{CC} = 2.7 to 3.6V			0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.5			V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} - 0.2	V _{CC}		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -18mA	V _{CC} - 0.6			
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} - 1.0			
V _{OL}	LOW level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA			0.40	V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		GND	0.20	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA			0.55	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = 5.5V or GND		± 0.1	± 5	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0		0.1	10	μA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		5	500	μA

NOTES:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\Omega$; $T_{amb} = -40^\circ C$ to $+85^\circ C$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V _{CC} = 3.3V ±0.3V			V _{CC} = 2.7V		
			MIN	TYP ¹	MAX	MIN	MAX	
t _{PHL} / t _{PLH}	Propagation delay nCP to nQ, nQ̄	Figures 1, 3	1.5	3.6	5.2	—	6.0	ns
	Propagation delay nSD to nQ, nQ̄	Figures 2, 3	1.5	3.5	5.4	—	6.4	ns
	Propagation delay nRD to nQ, nQ̄	Figures 2, 3	1.5	3.5	5.4	—	6.4	ns
t _W	Clock pulse width HIGH or LOW	Figure 1	3.3	1.3	—	—	—	ns
	Set or reset pulse width LOW	Figure 2	3.3	1.7	—	—	—	
t _{rem}	Removal time set or reset	Figure 2	1	–3	—	—	—	ns
t _{su}	Set-up time nD to nCP	Figure 1	2.0	0.8	—	—	—	ns
t _h	Hold time nD to nCP	Figure 1	1	–0.7	—	—	—	ns
f _{max}	Maximum clock pulse frequency	Figure 1	150	250	—	—	—	MHz

NOTE:

1. These typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.

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AC WAVEFORMS

$V_M = 1.5\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7\text{ V}$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

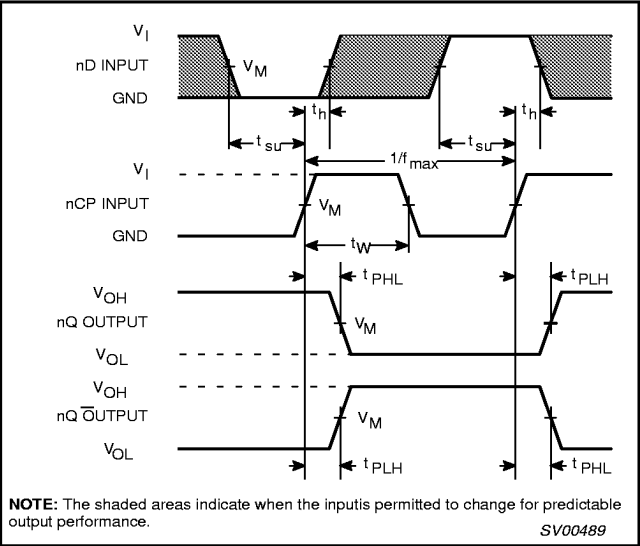


Figure 1. Clock (nCP) to output (nQ, nQ̄) propagation delays, clock pulse width, nD to nCP set-up times, the nCP to nD hold times, output transition times and maximum clock pulse frequency.

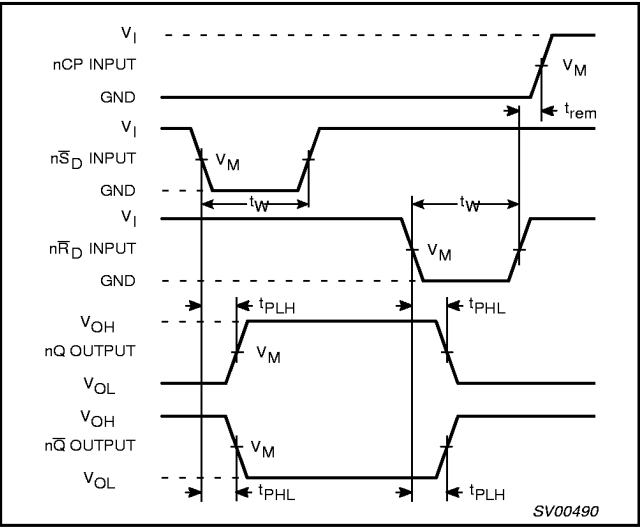


Figure 2. Set (nSD) and reset (nRD) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the nRD to nCP removal time.

TEST CIRCUIT

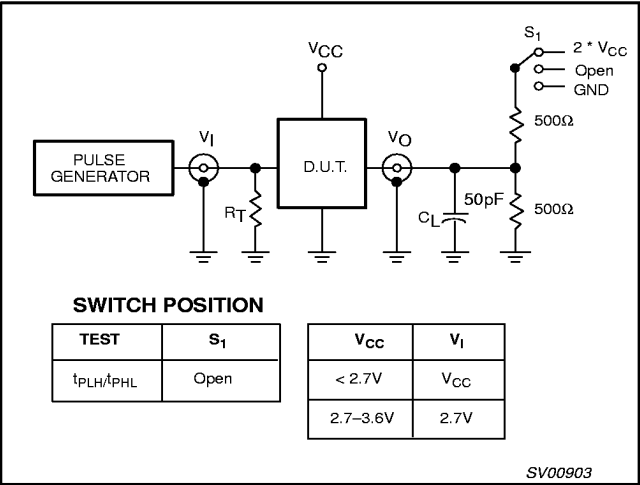


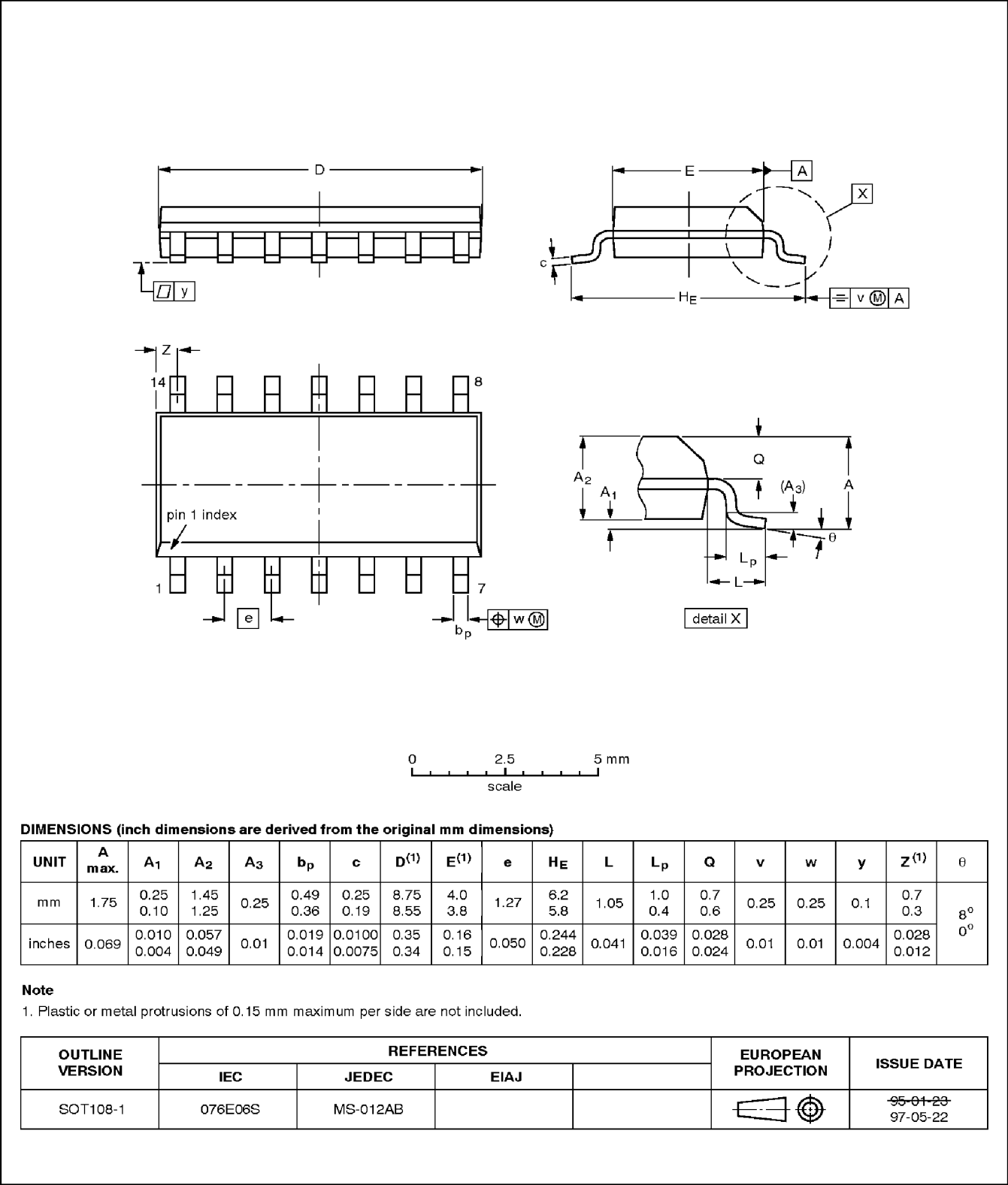
Figure 3. Load circuitry for switching times.

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

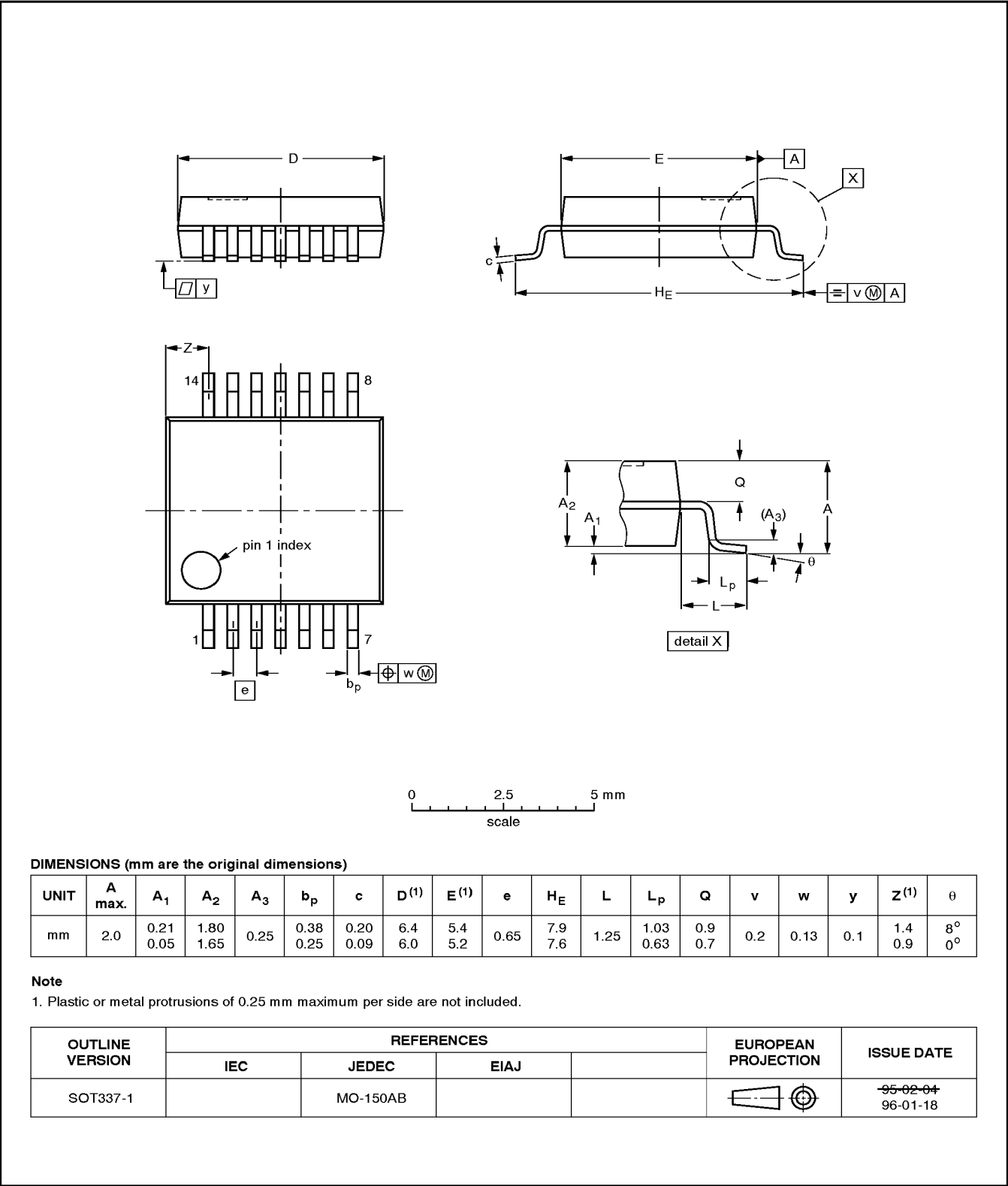


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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

