

9-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

74LVC823A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 9-bit positive edge-triggered register
- Independent register and 3-State buffer operation
- Flow-through pin-out architecture

DESCRIPTION

The 74LVC823A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-state operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC823A is a 9-bit D-type flip-flop with common clock (CP), Clock Enable ($\overline{CE}$), Master Reset ($\overline{MR}$) and 3-State outputs for bus-oriented applications.

The nine flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition provided $\overline{CE}$ is LOW. When $\overline{CE}$ is HIGH the flip-flops hold their data.

A LOW on $\overline{MR}$ resets all flip-flops.

When $\overline{OE}$ is LOW, the contents of the nine flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	$C_L = 50 \text{ pF}$; $V_{CC} = 3.3 \text{ V}$	4.8	ns
f_{max}	Maximum clock frequency	$C_L = 50 \text{ pF}$; $V_{CC} = 3.3 \text{ V}$	150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	27	pF

NOTES:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
- The condition is $V_I = \text{GND to } V_{CC}$

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDERING CODE	PKG. DWG. #
24-Pin Plastic SO	-40°C to $+85^{\circ}\text{C}$	74LVC823A D	SOT137-1
24-Pin Plastic SSOP Type II	-40°C to $+85^{\circ}\text{C}$	74LVC823A DB	SOT340-1
24-Pin Plastic TSSOP Type I	-40°C to $+85^{\circ}\text{C}$	74LVC823A PW	SOT355-1

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PIN DESCRIPTION

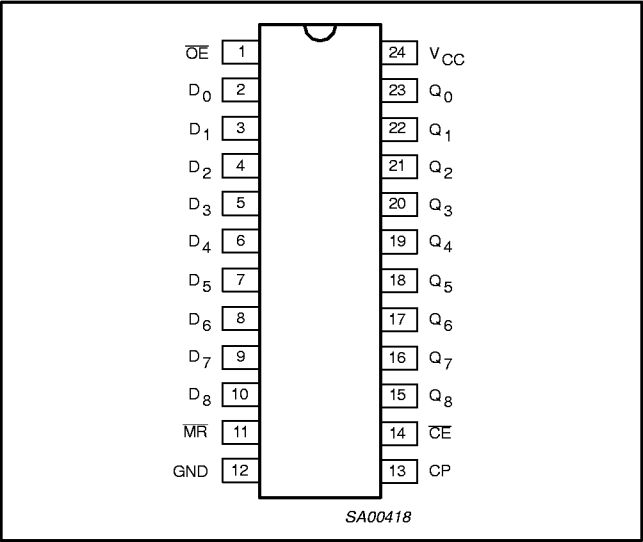
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10	D_0 to D_8	Data inputs
11	MR	Master reset (active LOW)
12	GND	Ground (0 V)
13	CP	Clock pulse (active rising)
14	$\overline{CE}$	Clock enable (active LOW)
23, 22, 21, 20, 19, 18, 17, 16, 15	Q_0 to Q_8	3-State flip-flop outputs
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

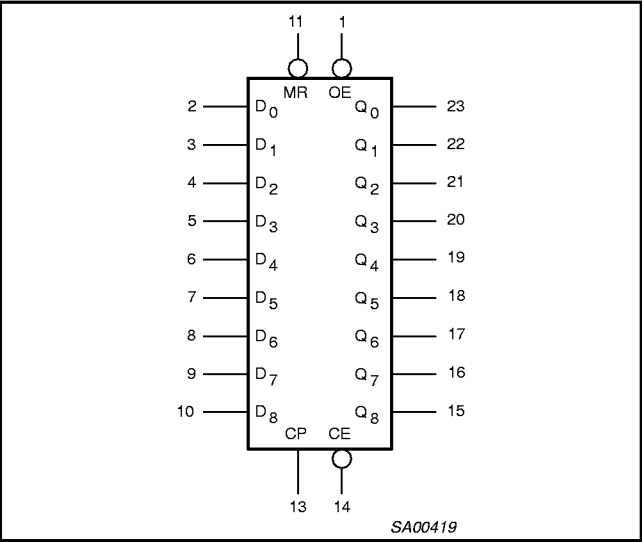
OPERATING MODES	INPUTS					INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	MR	$\overline{CE}$	CP	D_n		Q_0 to Q_8
Clear	L	L	X	X	X	L	L
Load and read register	L	H	L	$\uparrow$	L	L	L
	L	H	L	$\uparrow$	h	H	H
Load register and disable outputs	H	H	L	X	L	L	Z
	H	H	L	X	h	H	Z
Hold	L	H	H	NC	X	NC	NC

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
 $\uparrow$ = LOW-to-HIGH clock transition
NC= no change

PIN CONFIGURATION



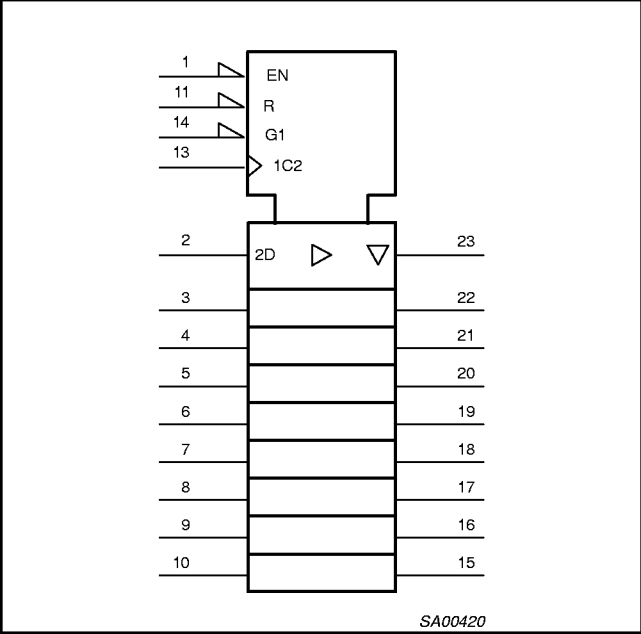
LOGIC SYMBOL



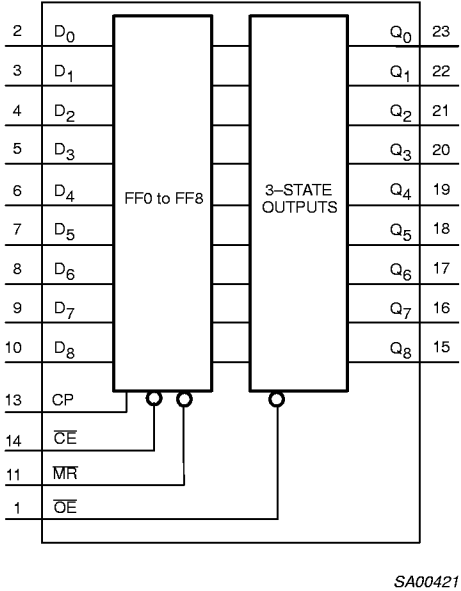
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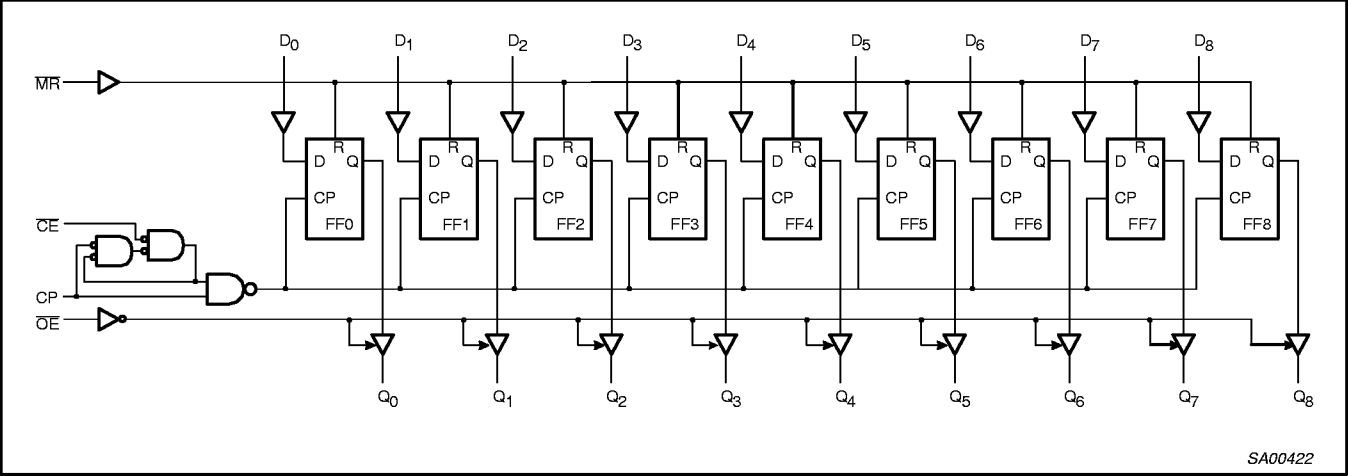
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$	0	20	ns/V
		$V_{CC} = 2.7$ to $3.6V$	0	10	

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	Note 2	-0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	-0.5 to $V_{CC} + 0.5$	V
	DC output voltage; output 3-State	Note 2	-0.5 to 6.5	
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package			mW
	– plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}			V
		V _{CC} = 2.7 to 3.6V	2.0			
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			GND	V
		V _{CC} = 2.7 to 3.6V			0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.5			V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} - 0.2	V _{CC}		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -18mA	V _{CC} - 0.6			
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} - 0.8			
V _{OL}	LOW level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA			0.40	V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA			0.20	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA			0.55	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = 5.5V or GND		± 0.1	± 5	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = 5.5V or GND		0.1	± 5	μA
I _{off}	Power off leakage supply	V _{CC} = 0.0V; V _I or V _O = 5.5V		0.1	± 10	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0		0.1	10	μA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		5	500	μA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

GND = 0V; t_r = t_f ≤ 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V _{CC} = 3.3V ± 0.3V			V _{CC} = 2.7V		V _{CC} = 1.2V	
			MIN	TYP ¹	MAX	MIN	MAX	TYP	
t _{PHL} t _{PLH}	Propagation delay CP to Q _n	Figures 1, 4			8.5		9.5		ns
t _{PHL}	Propagation delay MR to Q _n	Figures 1, 4			8.0		8.5		ns
t _{PZH} t _{PZL}	3-State output enable time OE to Q _n	Figures 2, 4			7.0		7.5		ns
t _W	Clock pulse width HIGH or LOW	Figure 1		3.0					ns
t _{SU}	Setup time D _n to CP	Figure 3	1.0	0.3		1.0			ns
t _H	Hold time HIGH or LOW D _n after CP	Figure 3	1.0	-0.2		1.0			ns
f _{max}	Maximum clock pulse frequency	Figure 1	75	150					MHz

NOTE:

1. Unless otherwise stated, all typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

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AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7V$.
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7V$
 $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7V$

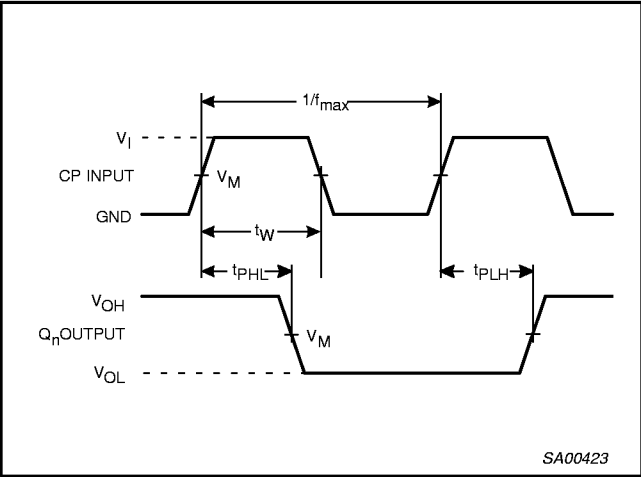


Figure 1. Clock (CP) to output (Qn) propagation delays, the clock pulse width and the maximum clock pulse frequency.

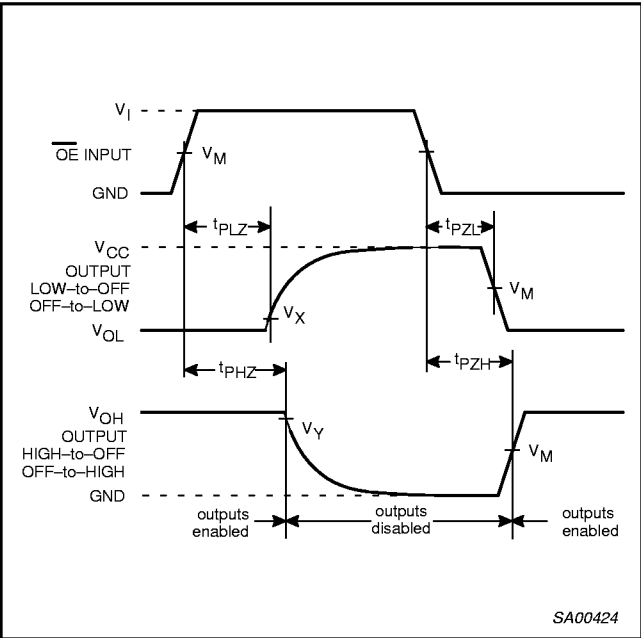


Figure 2. 3-State enable and disable times.

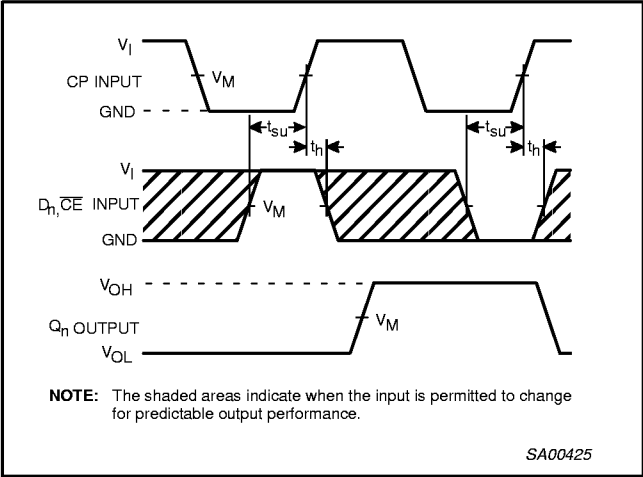


Figure 3. Data setup and hold times for the Dn input and CE input to the CP input.

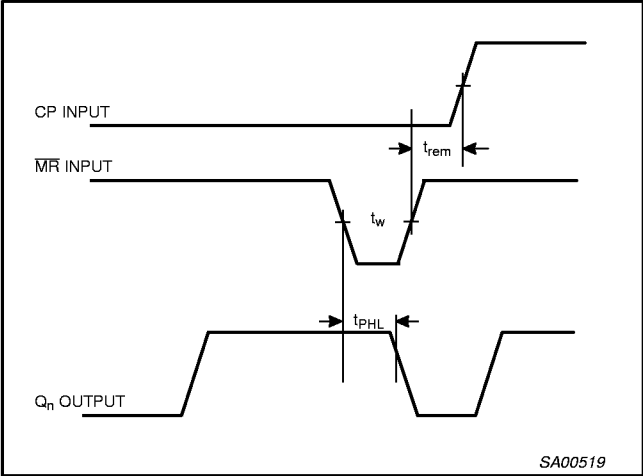


Figure 4. Master reset pulse width, master reset to clock removal time, master reset to output propagation delay.

TEST CIRCUIT

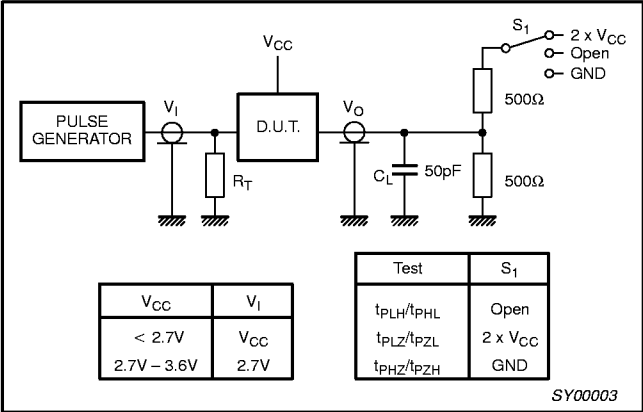


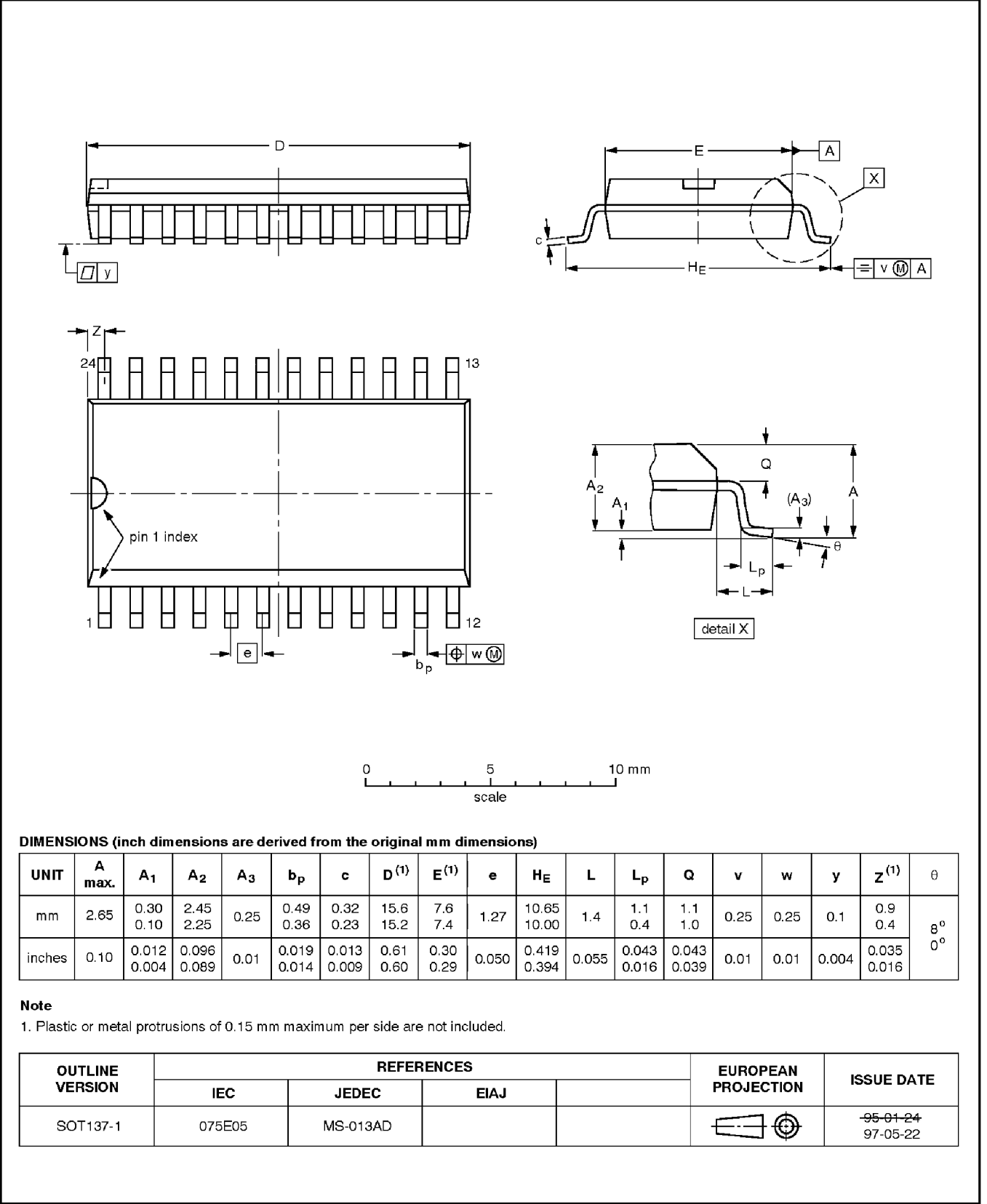
Figure 5. Load circuitry for switching times.

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

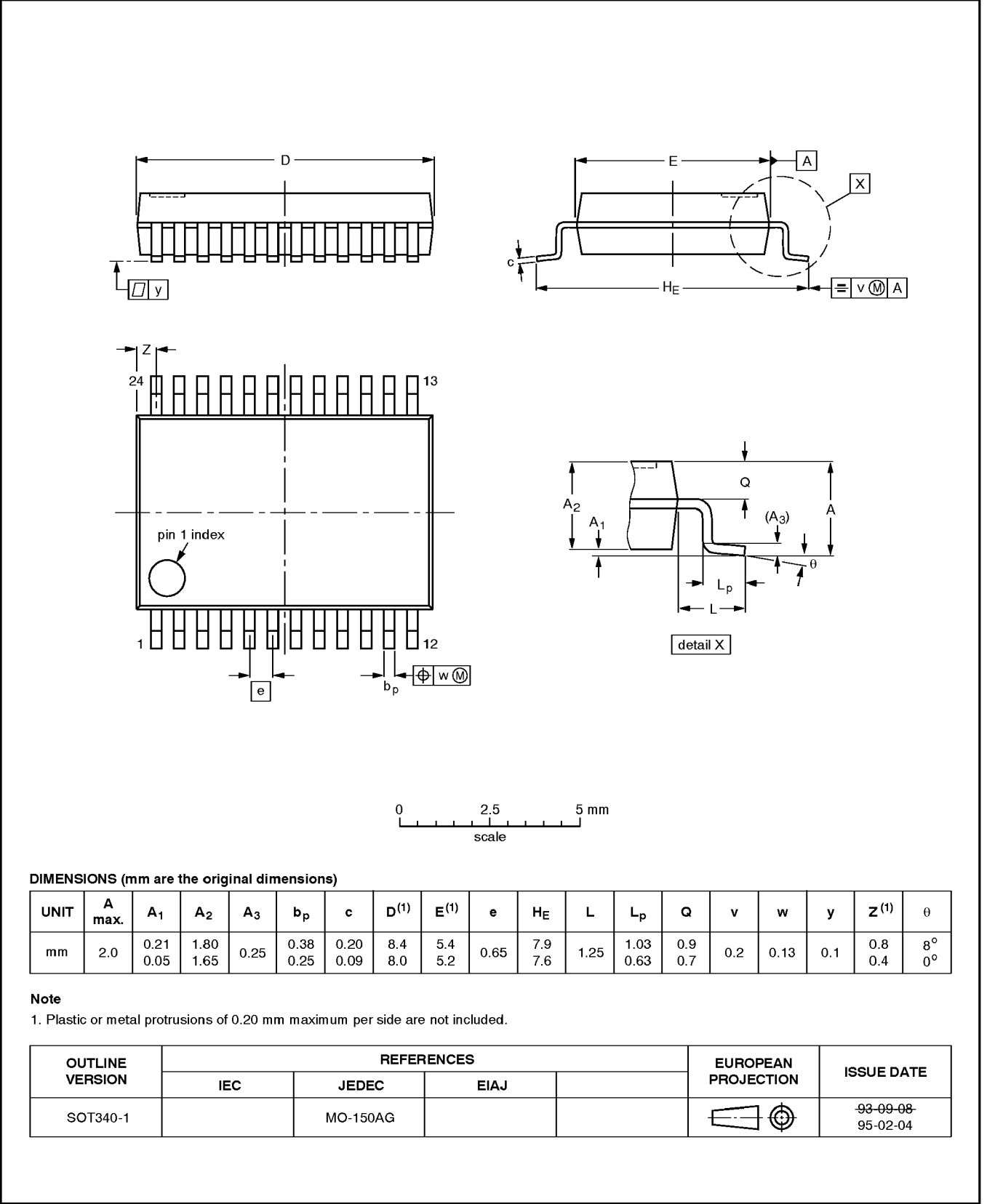


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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

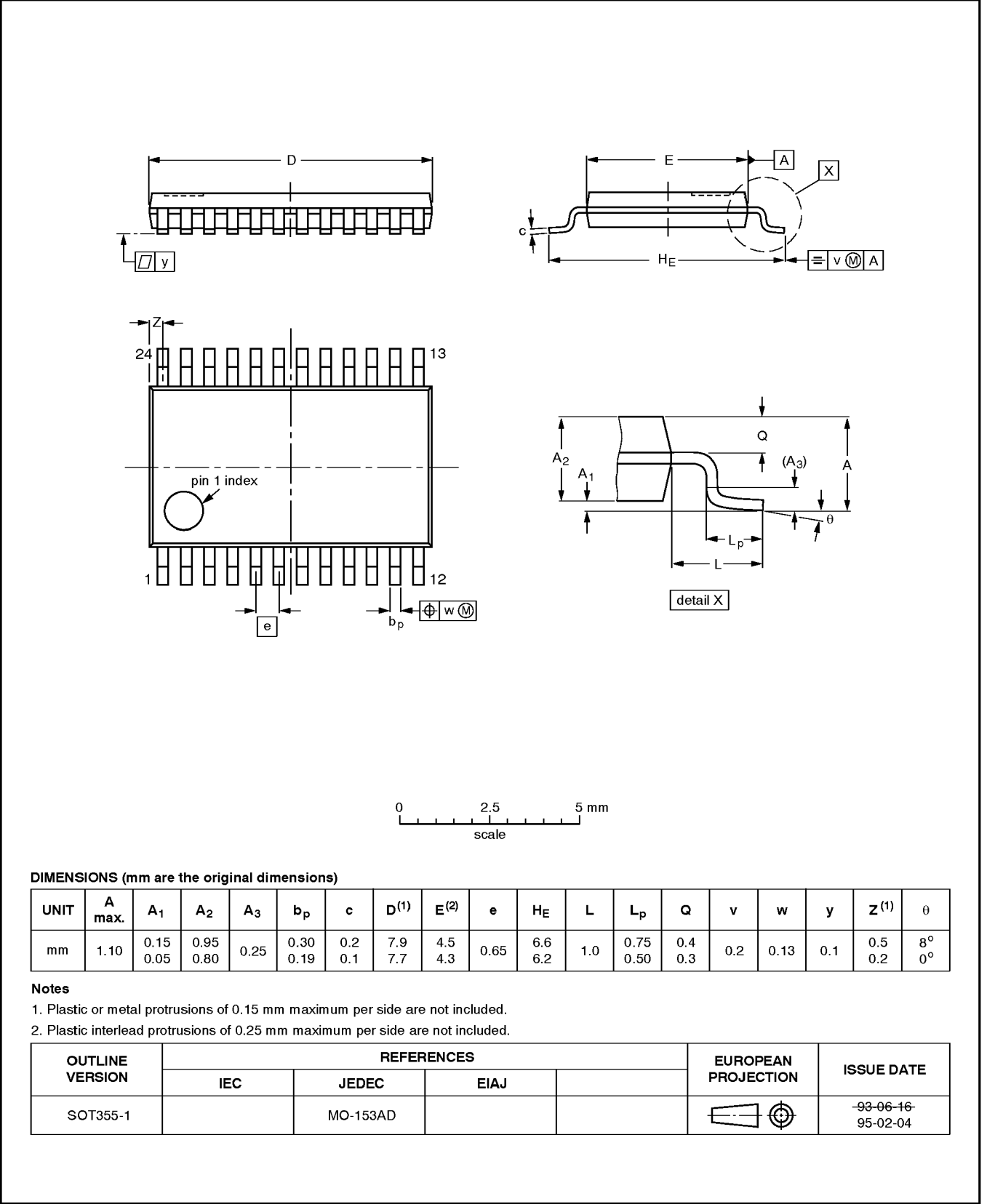


9-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

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TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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