9-Bit D-type flip-flop; positive-edge trigger; 3-state 74LVC823

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **8-bit positive edge-triggered register**
- **Independent register and 3-state buffer operation**
- **Flow-through pin-out architecture**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC823 is a low-power, low-voltage, high-performance, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.
The 74LVC823 is a 9-bit D-type flip-flop with common clock (CP), Clock Enable ($\overline{CE}$), Master Reset ($\overline{MR}$) and 3-state outputs for bus oriented applications.
The nine flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition, provided $\overline{CE}$ is LOW. When $\overline{CE}$ is HIGH the flip-flops hold their data.
A low on $\overline{MR}$ resets all flip-flops.

When $\overline{OE}$ is LOW, the contents of the nine flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 50 pF; V_{CC} = 3.3 V	4.8	ns
f_{max}	maximum clock frequency		150	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	28	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC823D	24	SO	plastic	SO24/SOT137
74LVC823DB	24	SSOP	plastic	SSOP24/SOT340
74LVC823PW	24	TSSOP	plastic	TSSOP24/SOT355

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10	D_0 to D_8	data inputs
11	$\overline{MR}$	mater reset (active Low)
12	GND	ground (0 V)
13	CP	clock pulse (active rising)
14	$\overline{CE}$	clock enable (active Low)
23, 22, 21, 20, 19, 18, 17, 16, 15	Q_0 to Q_8	3-state flip-flop outputs
24	V_{CC}	positive supply voltage

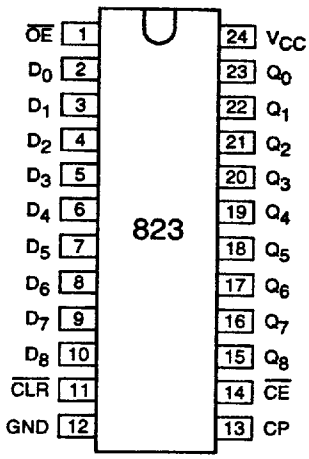


Fig.1 Pin configuration.

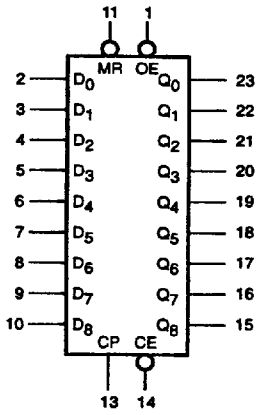


Fig.2 Logic symbol.

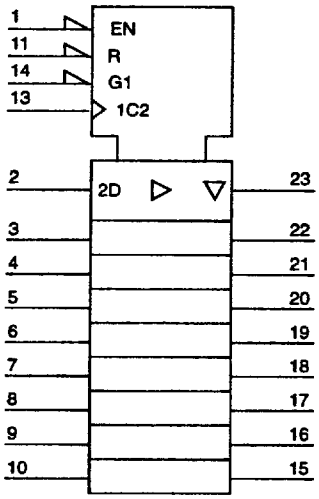


Fig3. IEC logic symbol.

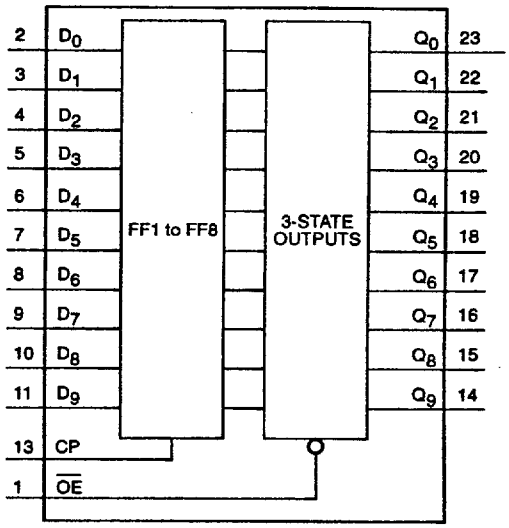


Fig.4 Functional diagram.

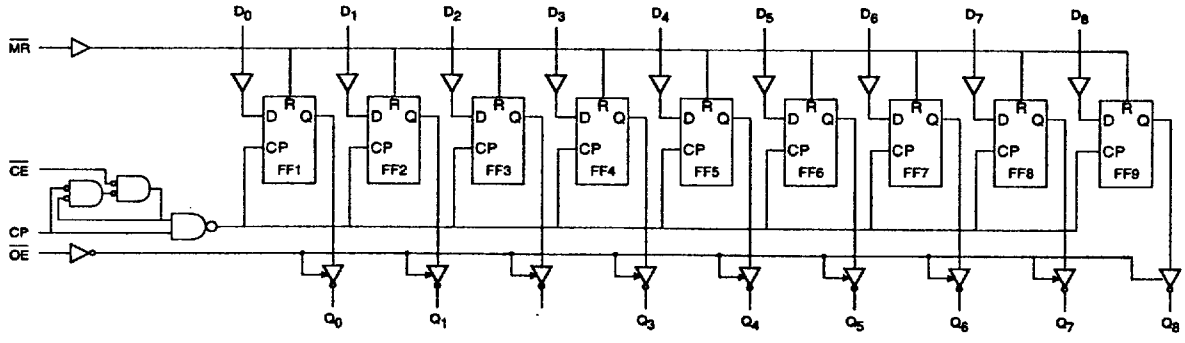


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS					INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	D_n		Q_0 to Q_8
clear	L	L	X	X	X	L	L
load and read register	L L	H H	L L	↑ ↑	l h	L H	L H
load register and disable outputs	H H	H H	L L	X X	l h	L H	Z Z
hold	L	H	H	NC	X	NC	NC

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition
NC = no change

DC CHARACTERISTICS FOR 74LVC823

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC823

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	– – –	– – –	– 9.5 8.5	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– – –	– – –	– 8.5 8.0	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– – –	– – –	– 7.5 7.0	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_W	clock pulse width HIGH or LOW	– –	3.0 3.0*	– –	ns	2.7 3.0 to 3.6	Fig.6
t_{su}	set-up time D_n to CP	1.0 1.0	0.3 0.3*	– –	ns	2.7 3.0 to 3.6	Fig.8
t_h	hold time D_n to CP	1.0 1.0	−0.2 −0.2*	– –	ns	2.7 3.0 to 3.6	Fig.8
f_{max}	maximum clock pulse frequency	– 75	– 150*	– –	MHz	2.7 3.0 to 3.6	Fig.6

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

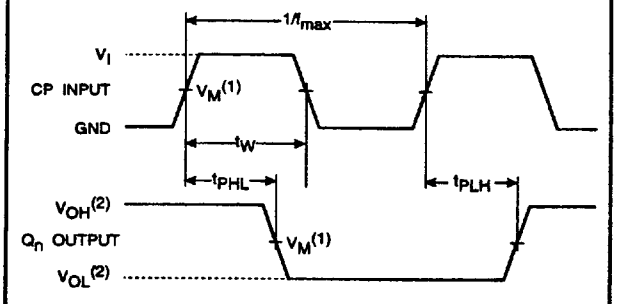


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

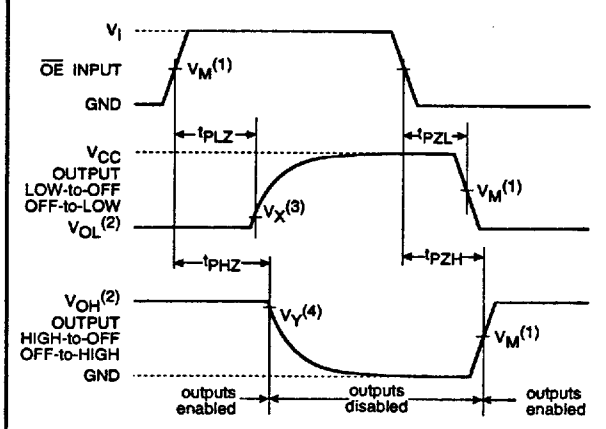


Fig.7 Waveforms showing the 3-state enable and disable times.

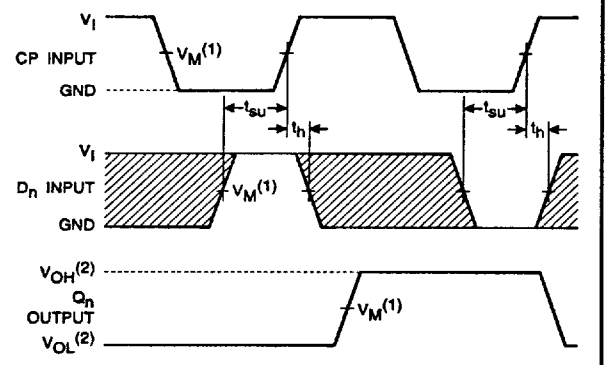
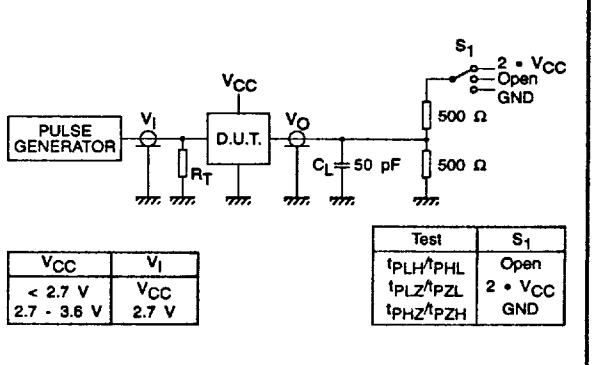


Fig.8 Waveforms showing the data set-up and hold times for the D_n input to the CP input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} < 2.7 V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

(4) $V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V