Quad buffer/line driver with 5-volt tolerant inputs/outputs; 3-state

74LVC125A
74LVCH125A

FEATURES

- **5-Volt tolerant inputs/outputs, for interfacing with 5-volt logic.**
- **Supply voltage range of 2.7 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **High impedance when V_{CC}=0 V**
- **Bushold on all data inputs (LVCH125A only).**

DESCRIPTION

The 74LVC(H)125A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 V or 5.0 V devices. In 3-state operation, outputs can handle 5 V. The 74LVC(H)125A consists of four non-inverting buffers/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 50 pF V_{CC} = 3.3 V	3.5	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC(H)125AD	14	SO	plastic	SOT108-1
74LVC(H)125ADB	14	SSOP	plastic	SOT337-1
74LVC(H)125APW	14	TSSOP	plastic	SOT402-1

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$1\overline{OE}$ to $4\overline{OE}$	output enable inputs (active LOW)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

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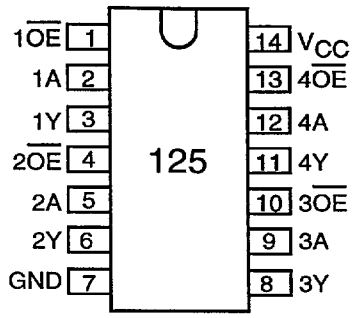


Fig.1 Pin configuration.

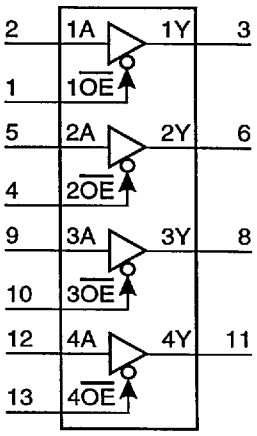


Fig.2 Logic symbol.

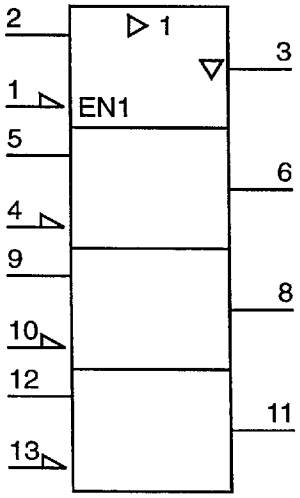


Fig.3 IEC Logic symbol.

DC CHARACTERISTICS FOR 74LVC(H)125A

For the DC characteristics see chapter "LVC(H)-A family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC(H)125A

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA to nY	–	–	–	ns	1.2	Figs 4, 6
		–	–	6.0		2.7	
		–	–	5.0		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY	–	–	–	ns	1.2	Figs 5, 6
		–	–	7.0		2.7	
		–	–	6.0		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY	–	–	–	ns	1.2	Figs 5, 6
		–	–	6.0		2.7	
		–	–	5.0		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

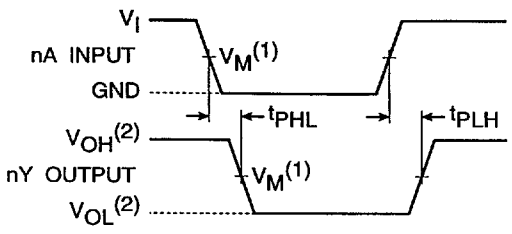


Fig.4 Waveforms showing the input (nA) to output (nY) propagation delays.

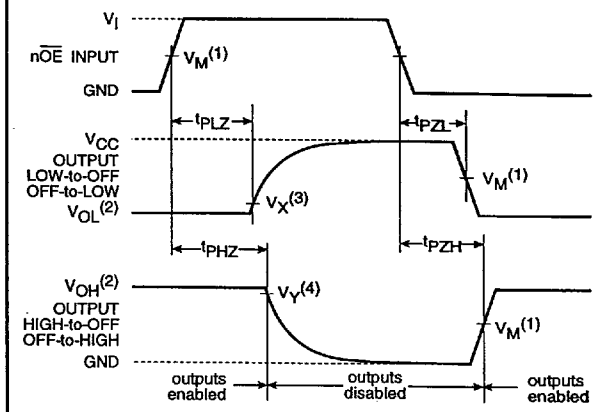
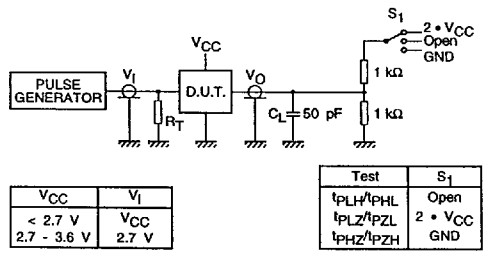


Fig.5 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.6 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V