

Octal buffer/line driver with 5-volt tolerant inputs/outputs; damping resistor; 3-state

74LVC2241A 74LVCH2241A

FEATURES

- 5-Volt tolerant inputs/outputs, for interfacing with 5-volt logic.
- Supply voltage range of 2.7 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when $V_{CC} = 0$ V
- Bushold on all data inputs (LVCH241A only).
- integrated 30Ω damping resistor.

DESCRIPTION

The 74LVC(H)2241A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment

The 74LVC(H)2241A is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs 1OE and 2OE. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n	$C_L = 50$ pF $V_{CC} = 3.3$ V	4.0	ns
C_i	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_i = \text{GND to } V_{CC}$

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC(H)2241AD	20	SO20	plastic	SOT163-1
74LVC(H)2241ADB	20	SSOP20	plastic	SOT339-1
74LVC(H)2241APW	20	TSSOP20	plastic	SOT360-1

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	1OE	output enable input (active LOW)
2, 4, 6, 8	1A ₀ to 1A ₃	data inputs
3, 5, 7, 9	2Y ₀ to 2Y ₃	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	2A ₀ to 2A ₃	data inputs
18, 16, 14, 12	1Y ₀ to 1Y ₃	bus outputs
19	2OE	output enable input (active HIGH)
20	V _{CC}	positive power supply

FUNCTION TABLES

INPUTS		OUTPUT
1OE	1A _n	1Y _n
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUT
2OE	2A _n	2Y _n
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high impedance OFF-state

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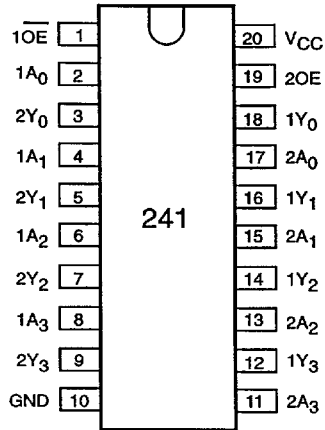


Fig.1 Pin configuration.

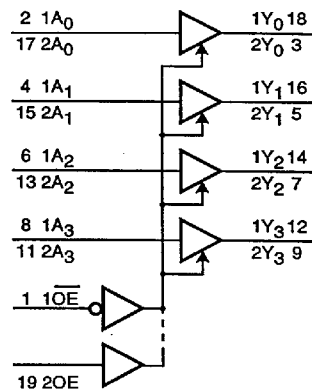


Fig.2 Logic symbol.

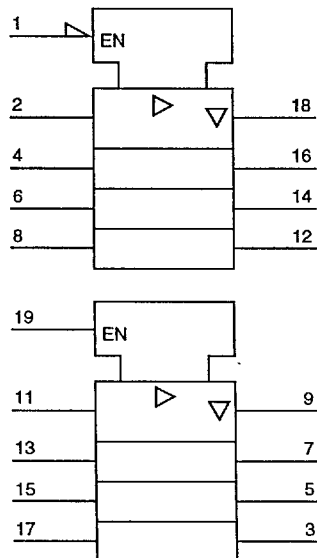


Fig.3 IEC logic symbol.

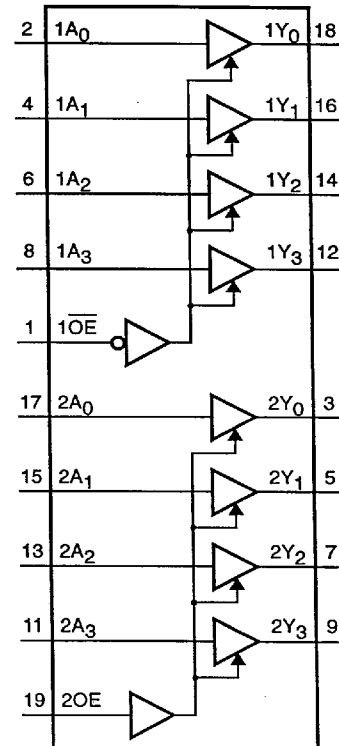


Fig.4 Functional diagram.

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74LVCH2241A

DC CHARACTERISTICS FOR 74LVC(H)2241A

For the DC characteristics see chapter "LVC(H)-A family characteristics", section "Family specifications".

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC(H)2241A

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay 1A _n to 1Y _n ; 2A _n to 2Y _n	—	—	—	ns	1.2	Figs 5, 8
		1.5	—	9.0		2.7	
		1.5	—	8.0		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time 1OE to 1Y _n	—	—	—	ns	1.2	Figs 6, 8
		1.5	—	10		2.7	
		1.5	—	9.0		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time 1OE to 1Y _n	—	—	—	ns	1.2	Figs 6, 8
		1.5	—	7.0		2.7	
		1.5	—	6.0		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time 2OE to 2Y _n	—	—	—	ns	1.2	Figs 7, 8
		1.5	—	10		2.7	
		1.5	—	9.0		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time 2OE to 2Y _n	—	—	—	ns	1.2	Figs 7, 8
		1.5	—	7.0		2.7	
		1.5	—	6.0		3.0 to 3.6	

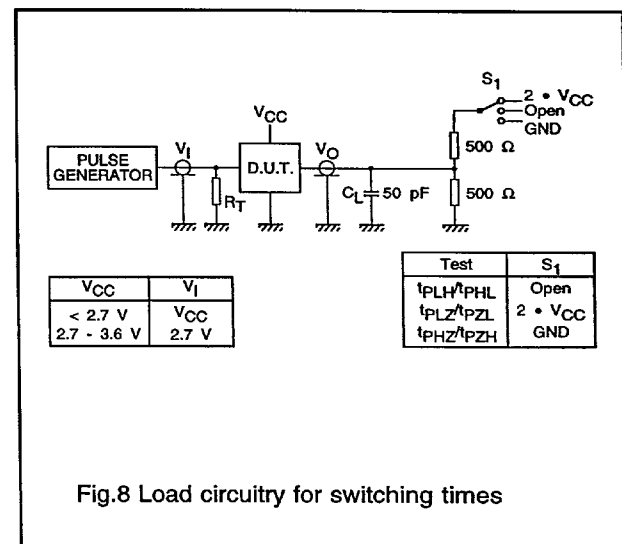
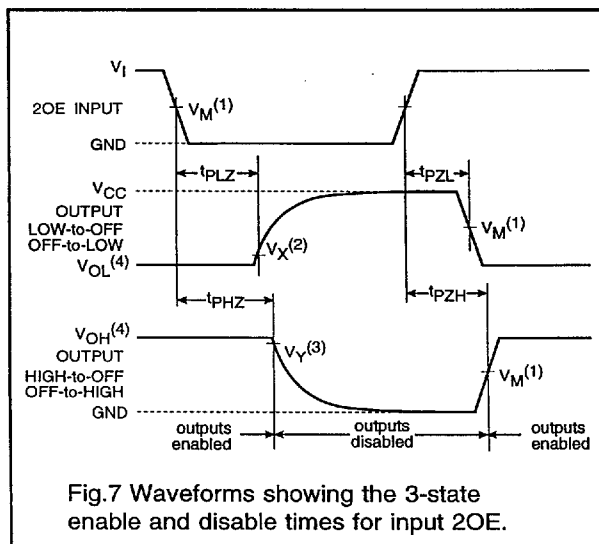
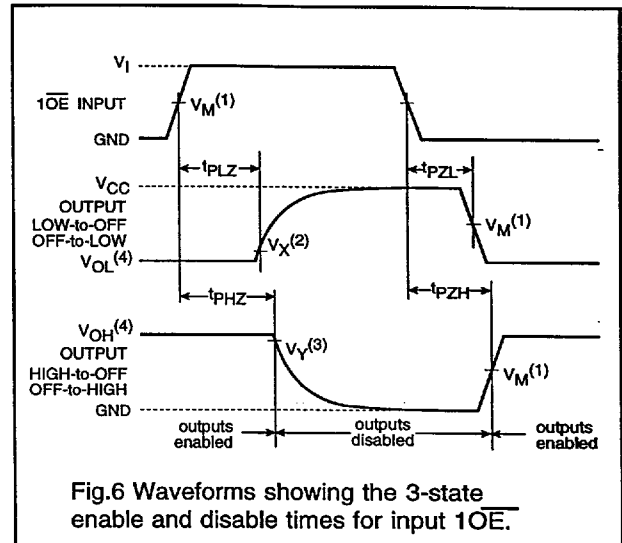
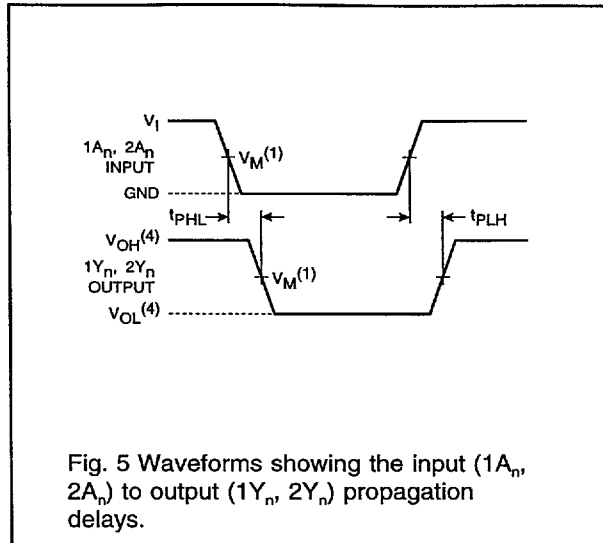
Notes: All typical values are measured at $T_{amb} = 25$ °C.

* Typical values are measured at $V_{CC} = 3.3$ V.

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AC WAVEFORMS



- Notes:**
- (1) $V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (2) $V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (3) $V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.