10-bit buffer/line driver with 5-volt tolerant inputs/outputs; damping resistor; 3-state

74LVC2827A
74LVCH2827A

FEATURES

- **5-volt tolerant inputs/outputs, for interfacing with 5-volt logic.**
- **Supply voltage range of 2.7 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **High impedance when V_{CC}= 0 V**
- **Bushold on all data inputs (LVCH2827A only).**
- **Integrated 30Ω damping resistor.**

GENERAL DESCRIPTION

The 74LVC(H)2827A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V enviroment.
The 74LVC(H)2827A is an 10-bit buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}_1$ and $\overline{OE}_2$.
A HIGH on $\overline{OE}$n causes the outputs to assume a high impedance OFF-state.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	C_L = 15 pF V_{CC} = 3.3 V	10	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	37	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC(H)2827AD	24	SO24	plastic	SOT137-1
74LVC(H)2827ADB	24	SSOP24	plastic	SOT340-1
74LVC(H)2827APW	24	TSSOP24	plastic	SOT355-1

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_9	data inputs
12	GND	ground (0 V)
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Y_0 to Y_9	bus outputs
24	V_{CC}	positive supply voltage

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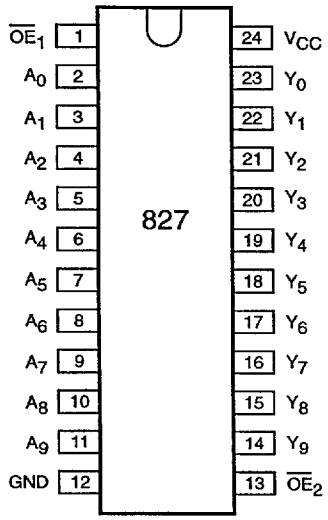


Fig.1 Pin configuration.

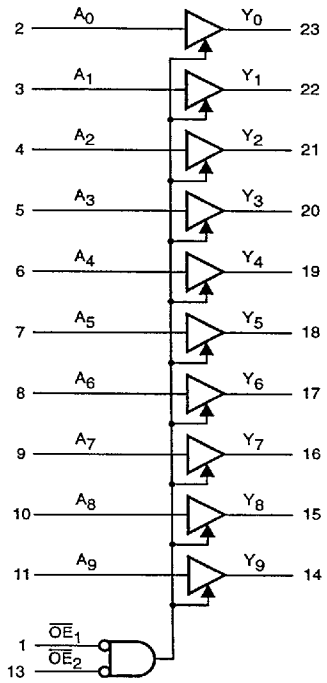


Fig.2 Logic symbol.

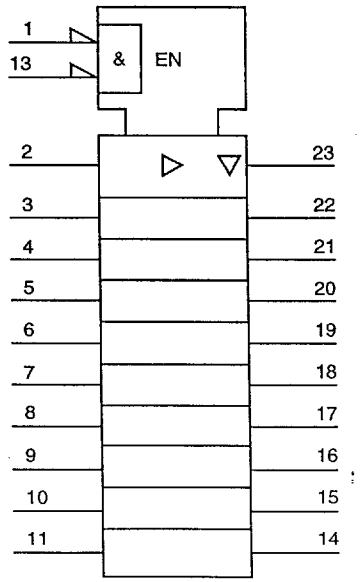


Fig.3 IEC logic symbol.

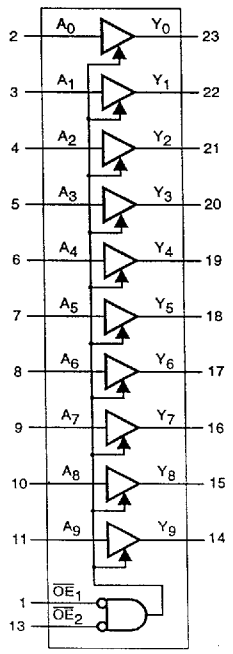


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LVC(H)2827A

For the DC characteristics see chapter "LVC(H)-A family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC(H)2827A

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay	–	–	–	ns	1.2	Figs 5, 7
	$1A_n$ to $1Y_n$;	–	–	9.0		2.7	
	$2A_n$ to $2Y_n$	–	–	8.0		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time	–	–	–	ns	1.2	Figs 6, 7
	$\overline{OE}_1$ to $1Y_n$;	–	–	10		2.7	
	OE_2 to $2Y_n$	–	–	9.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	–	–	ns	1.2	Figs 6, 7
	$\overline{OE}_1$ to $1Y_n$;	–	–	9.0		2.7	
	OE_2 to $2Y_n$	–	–	8.5		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

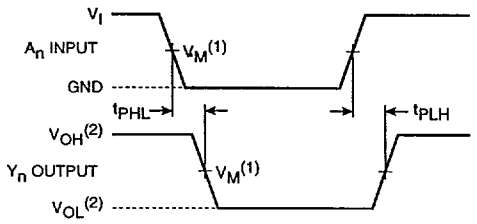


Fig.5 Waveforms showing the input (A_n) to output (Y_n) propagation delays.

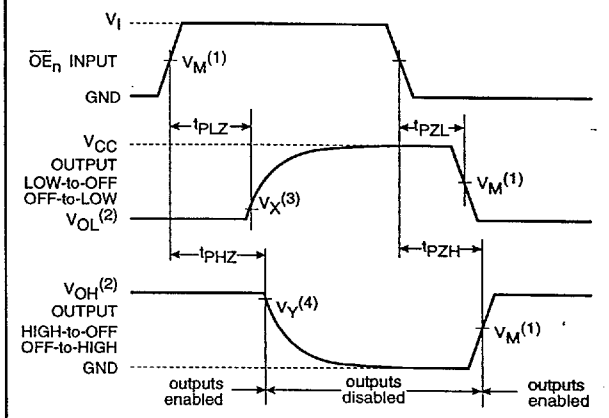
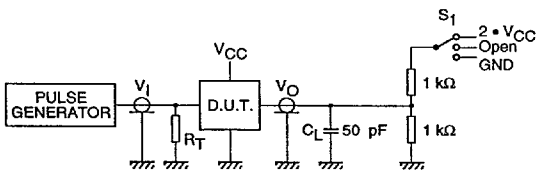


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V