

9-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger; 3-state

74LVC823A
74LVCH823A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic.
- Supply voltage range of 2.7 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages upto 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- 8-bit positive edge-triggered register
- Independent register and 3-state buffer operation
- High impedance when $V_{CC} = 0$ V
- Bushold on all data inputs (LVCH823A only).

DESCRIPTION

The 74LVC(H)823A is a low-power, low-voltage, high-performance, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC(H)823A is a 9-bit D-type flip-flop with common clock (CP), Clock Enable (CE), Master Reset ($\overline{MR}$) and 3-state outputs for bus oriented applications.

The nine flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition, provided $\overline{CE}$ is LOW. When $\overline{CE}$ is HIGH the flip-flops hold their data.

A low on $\overline{MR}$ resets all flip-flops.

When $\overline{OE}$ is LOW, the contents of the nine flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	$C_L = 50$ pF $V_{CC} = 3.3$ V	4.8	ns
f_{max}	maximum clock frequency		150	MHz
C_i	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	28	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is $V_i = \text{GND to } V_{CC}$.

ORDERING INFORMATION

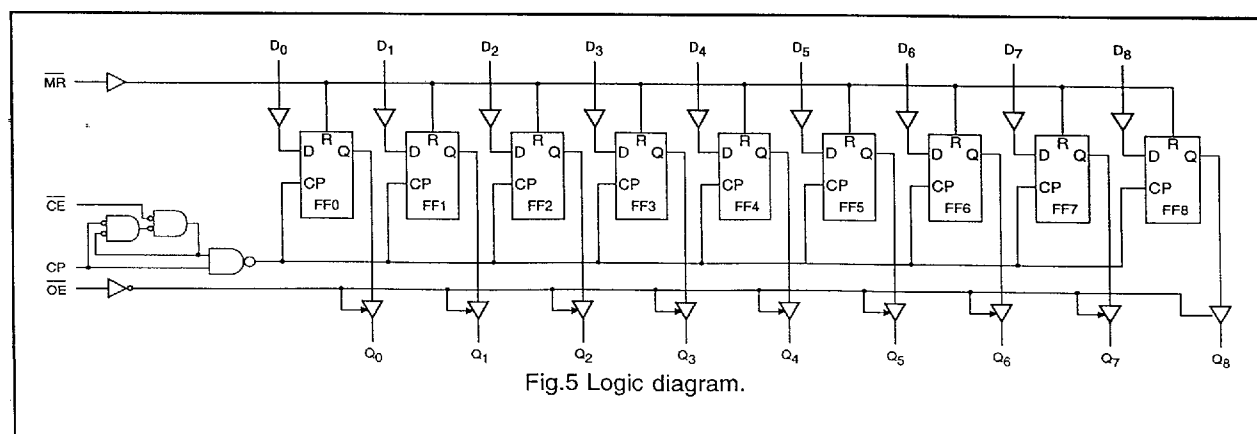
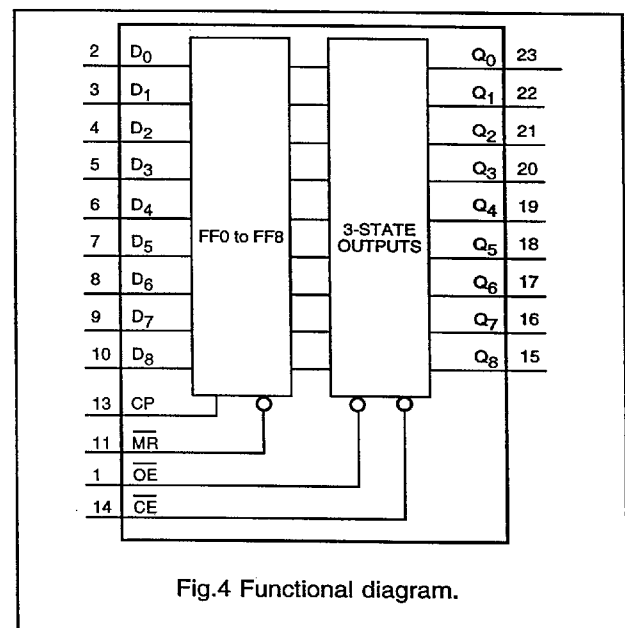
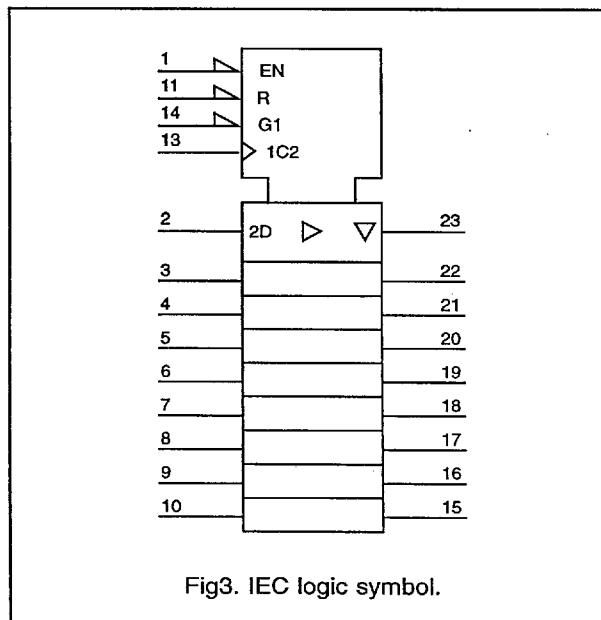
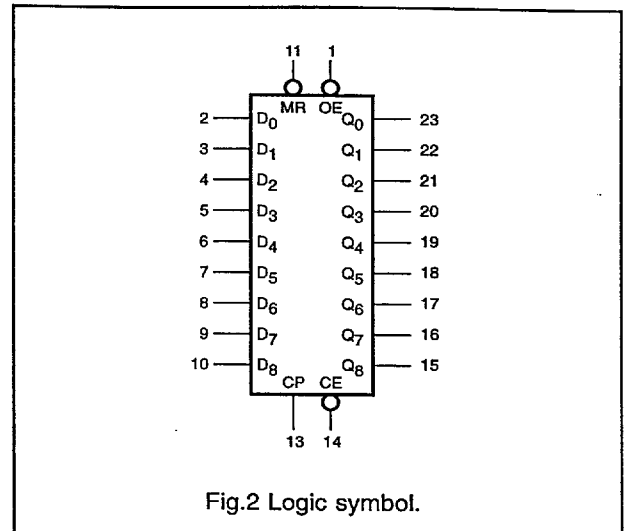
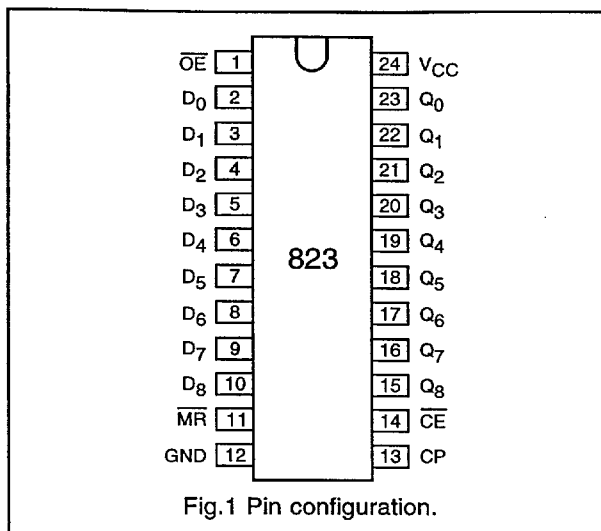
TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC(H)823AD	24	SO24	plastic	SOT137-1
74LVC(H)823ADB	24	SSOP24	plastic	SOT340-1
74LVC(H)823APW	24	TSSOP24	plastic	SOT355-1

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10	D_0 to D_8	data inputs
11	$\overline{MR}$	master reset (active Low)
12	GND	ground (0 V)
13	CP	clock pulse (active rising)
14	$\overline{CE}$	clock enable (active Low)
23, 22, 21, 20, 19, 18, 17, 16, 15	Q_0 to Q_8	3-state flip-flop outputs
24	V_{CC}	positive supply voltage

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FUNCTION TABLE

OPERATING MODES	INPUTS					INTERNAL FLIP-FLOP S	OUTPUTS Q ₀ to Q ₈
	$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	D _n		
clear	L	L	X	X	X	L	L
load and read register	L L	H H	L L	↑ ↑	l h	L H	L H
load register and disable outputs	H H	H H	L L	X X	l h	L H	Z Z
hold	L	H	H	NC	X	NC	NC

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high impedance OFF-state

↑ = LOW-to-HIGH clock transition

NC = no change

DC CHARACTERISTICS FOR 74LVC(H)823A

For the DC characteristics see chapter "LVC(H)-A family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC(H)823AGND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

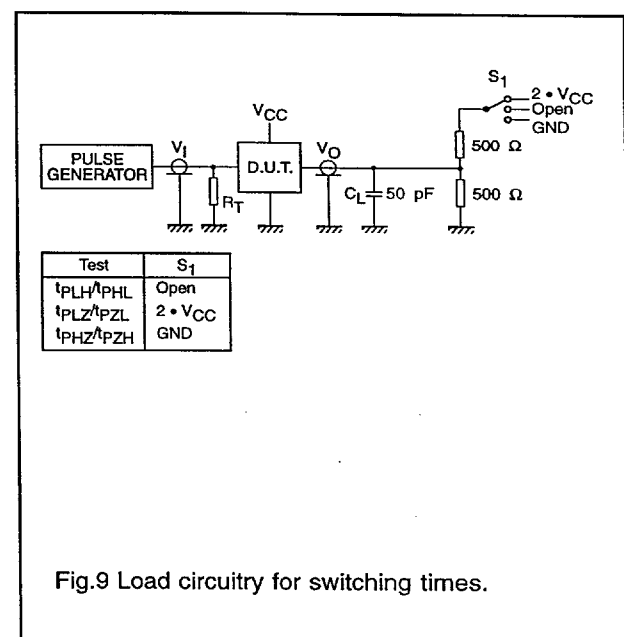
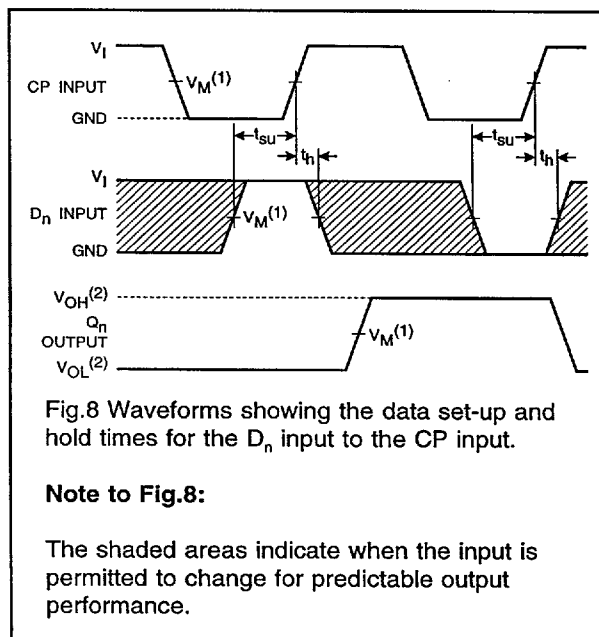
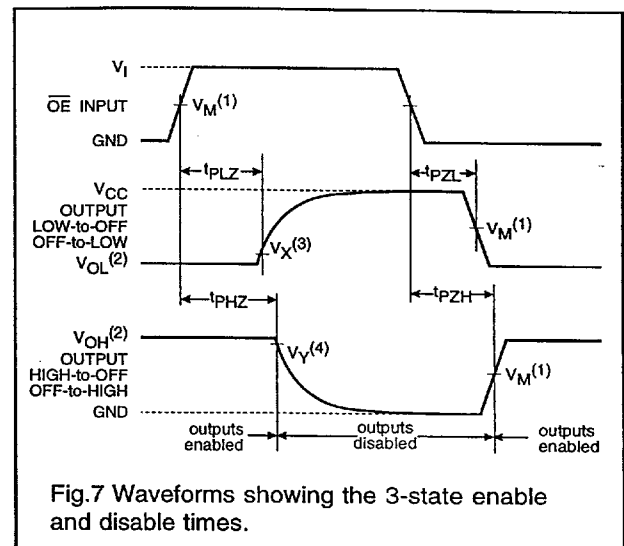
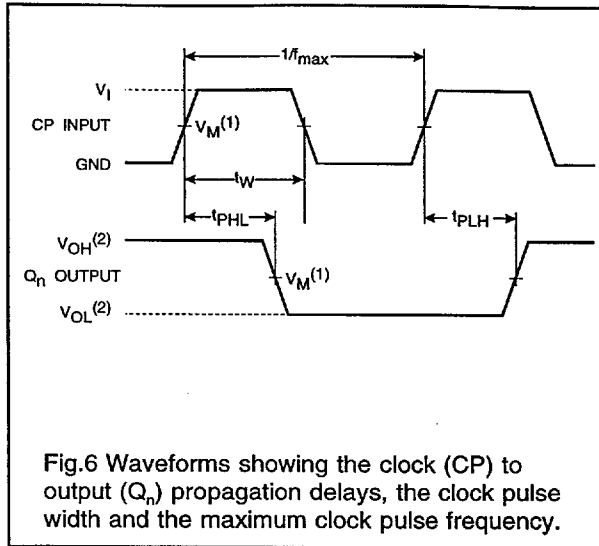
SYMBOL	PARAMETER	T _{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V _{cc} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t _{PHL} /t _{PLH}	propagation delay CP to Q _n	— — —	— — —	— 9.5 8.5	ns	1.2 2.7 3.0 to 3.6	Figs 6, 9
t _{PZH} /t _{PZL}	3-state output enable time OE to Q _n	— — —	— — —	— 8.5 8.0	ns	1.2 2.7 3.0 to 3.6	Figs 7, 9
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Q _n	— — —	— — —	— 7.5 7.0	ns	1.2 2.7 3.0 to 3.6	Figs 7, 9
t _W	clock pulse width HIGH or LOW	— —	3.0 3.0*	— —	ns	2.7 3.0 to 3.6	Fig.6
t _{su}	set-up time D _n to CP	1.0 1.0	0.3 0.3*	— —	ns	2.7 3.0 to 3.6	Fig.8
t _h	hold time D _n to CP	1.0 1.0	-0.2 -0.2*	— —	ns	2.7 3.0 to 3.6	Fig.8
f _{max}	maximum clock pulse frequency	— 75	— 150*	— —	MHz	2.7 3.0 to 3.6	Fig.6

Notes: All typical values are measured at T_{amb} = 25 °C.* Typical values are measured at V_{CC} = 3.3 V.

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AC WAVEFORMS



- Notes:**
- (1) $V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
 - (3) $V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (4) $V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$