

3.3V 16-bit transceiver with 30 Ω termination resistors (3-State)

74LVT162245B

FEATURES

- 16-bit bidirectional bus interface
- 3-State buffers
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30 Ω making external termination resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Same part as 74LVT16245B-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25°C	TYPICAL	UNIT
t _{PLH} t _{PHL}	Propagation delay nAx to nBx or nBx to nAx	C _L = 50pF; V _{CC} = 3.3V	2.5	ns
C _{IN}	Input capacitance DIR, $\overline{OE}$	V _I = 0V or 3.0V	3	pF
C _{I/O}	I/O pin capacitance	V _{I/O} = 0V or 3.0V	9	pF
I _{CCZ}	Total supply current	Outputs disabled; V _{CC} = 3.6V	70	μ A

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to +85°C	74LVT162245B DL	VT162245B DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74LVT162245B DGG	VT162245B DGG	SOT362-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	nDIR	Direction control input
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	nA0 – nA7	Data inputs/outputs (A side)
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	nB0 – nB7	Data inputs/outputs (B side)
25, 48	n $\overline{OE}$	Output enable input (active-Low)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive supply voltage

DESCRIPTION

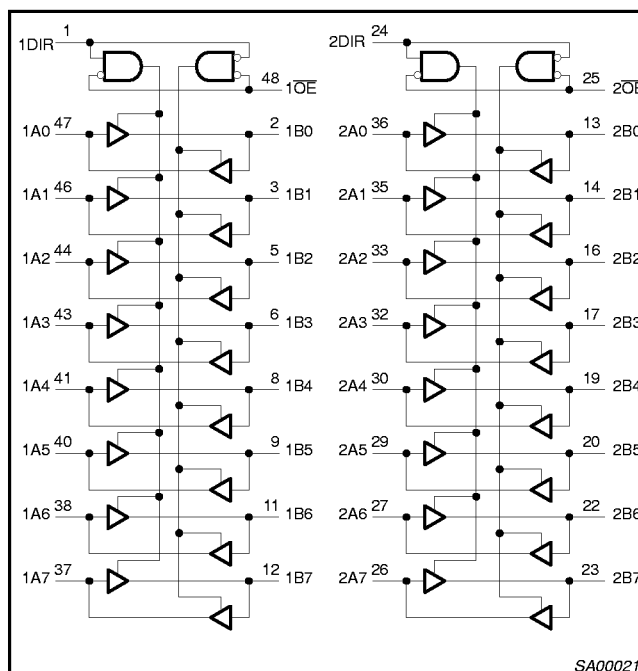
The 74LVT162245B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable (n $\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

The 74LVT162245B is designed with 30 Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74LVT162245B is the same as the 74LVT16245B-1. The part number has been changed to reflect industry standards.

LOGIC SYMBOL

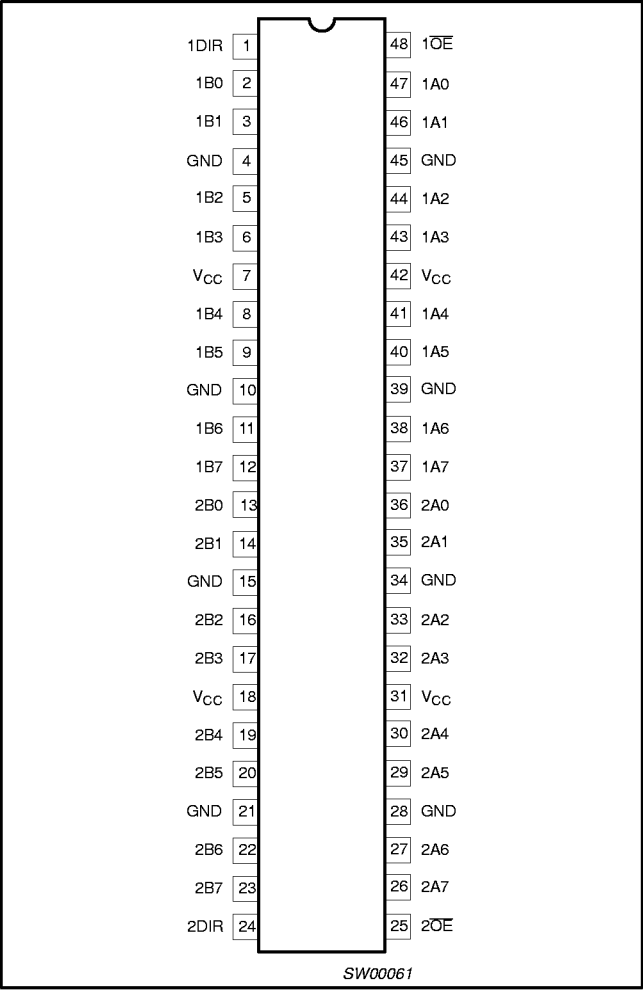


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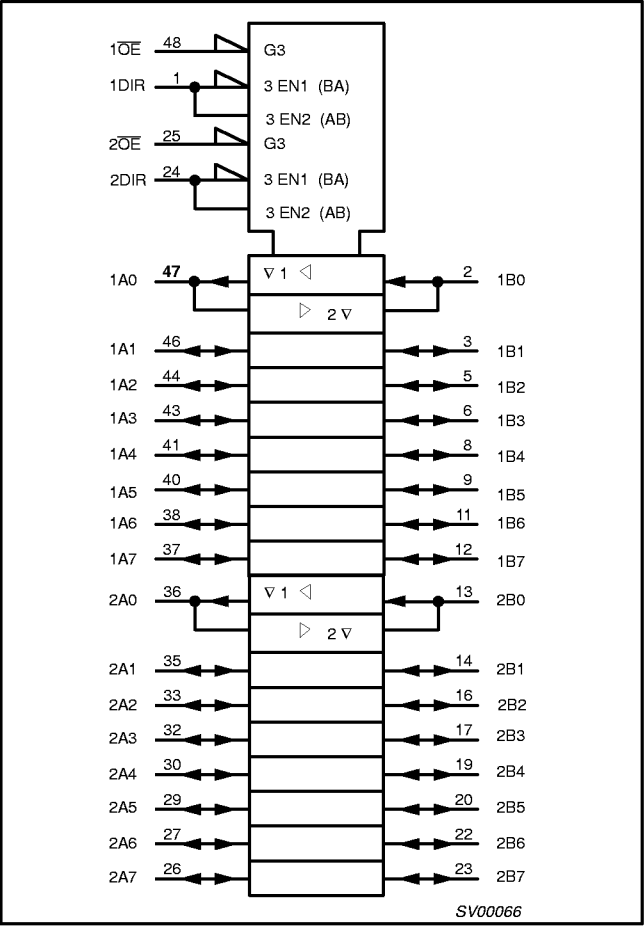
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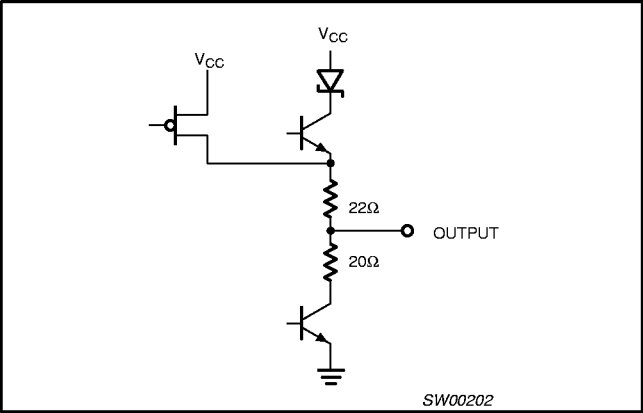
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



SCHEMATIC OF EACH OUTPUT



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
nOE	nDIR	nAx	nBx
L	L	nAx = nBx	Inputs
L	H	Inputs	nBx = nAx
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

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ABSOLUTE MAXIMUM RATINGS^{1,2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage ³		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		-12	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = −40°C to +85°C			
				MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.7V; I _{IK} = −18mA			0.8	−1.2	V
V _{OH}	High-level output voltage	V _{CC} = 3.0V; I _{OH} = −12mA		2.0	2.5		V
V _{OL}	Low-level output voltage	V _{CC} = 3.0V; I _{OL} = 12mA			0.3	0.8	V
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins		0.1	±1	μA
		V _{CC} = 0 or 3.6V; V _I = 5.5V			0.1	10	
		V _{CC} = 3.6V; V _I = V _{CC}	I/O Data pins ⁴		0.5	10	
		V _{CC} = 3.6V; V _I = 0			0.1	−5	
I _{OFF}	Output off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V			0.1	±100	μA
I _{HOLD}	Bus Hold current A or B outputs ⁶	V _{CC} = 3V; V _I = 0.8V		75	130		μA
		V _{CC} = 3V; V _I = 2.0V		−75	−130		
		V _{CC} = 0V to 3.6V; V _{CC} = 3.6V		±500			
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V			75	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = Don't care			40	±100	μA
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0			0.07	0.12	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0			4.2	6	
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵			0.07	0.12	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} −0.6V, Other inputs at V _{CC} or GND			0.1	0.2	mA

NOTES:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From $V_{CC} = 1.2V$ to $V_{CC} = 3.3V \pm 0.3V$ a transition time of 100 μ sec is permitted. This parameter is valid for $T_{amb} = 25^\circ C$ only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$; $R_L = 500\Omega$; $T_{amb} = -40^\circ C$ to $+85^\circ C$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP ¹	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to bBx or bBx to nAx	1	1.0 1.0	2.5 2.2	3.5 3.5	3.9 3.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	3.5 3.2	5.3 4.4	6.4 5.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	3.5 4.3	4.8 6.7	5.1 5.9	ns

NOTE:

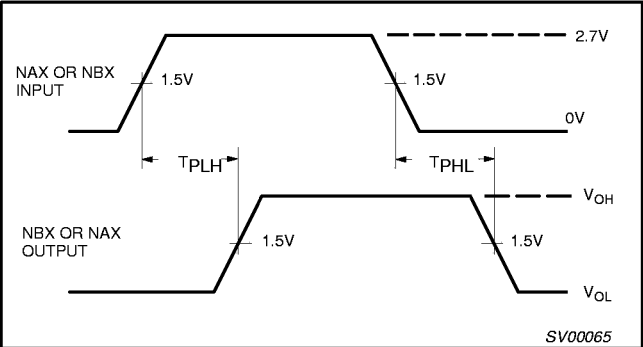
1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.

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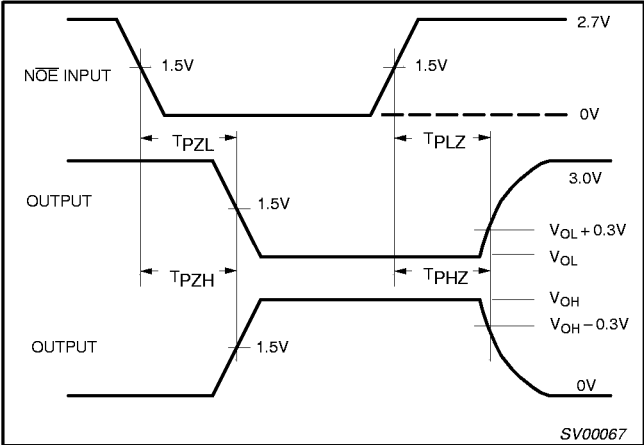
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AC WAVEFORMS

$V_M = 1.5V$, $V_{IN} = GND$ to $2.7V$

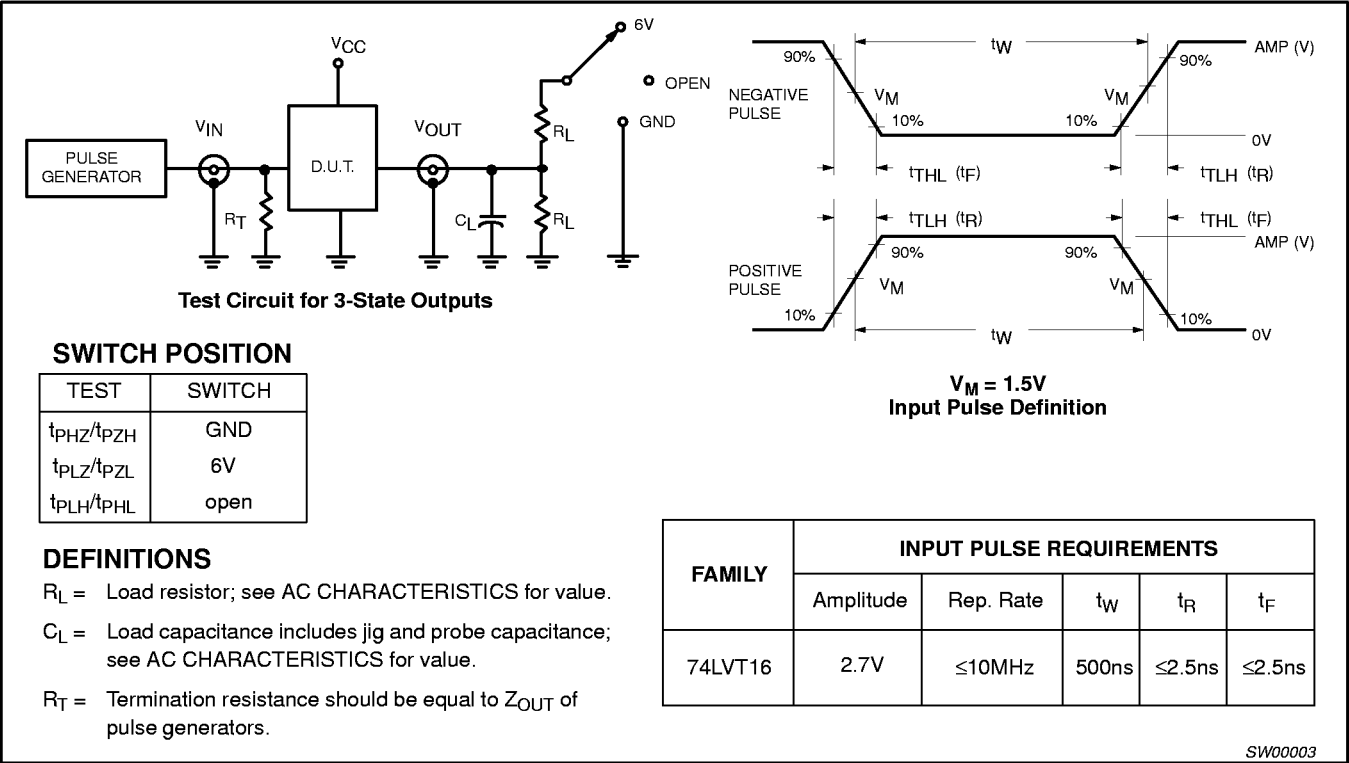


Waveform 1. Input to Output Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS

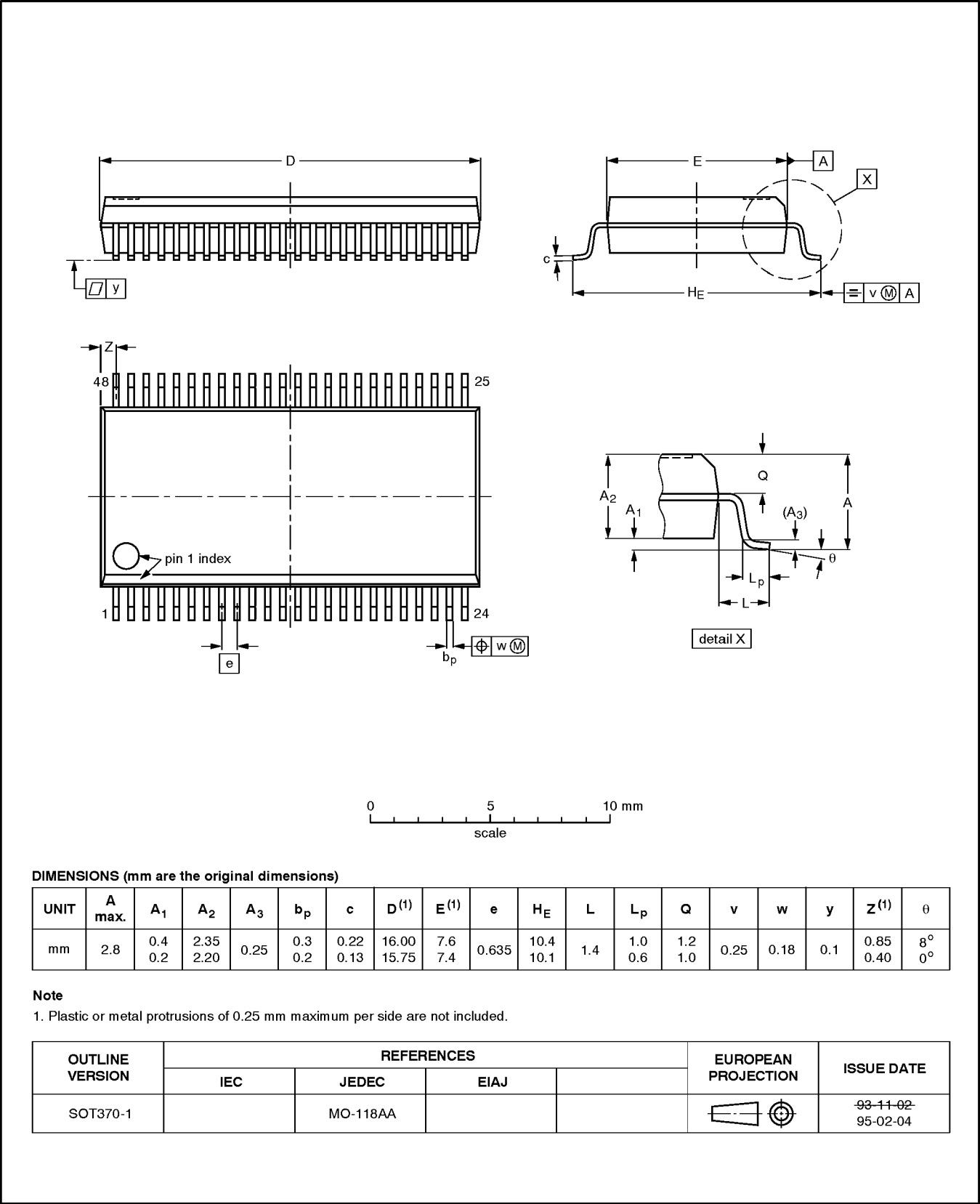


3.3V LVT 16-bit transceiver
with 30Ω termination resistors (3-State)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



3.3V LVT 16-bit transceiver with 30 Ω termination resistors (3-State)

74LVT162245B

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1

