

3.3V Octal D-type transparent latch (3-State)

74LVT573

FEATURES

- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State output buffers
- Common output enable
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- Power-up 3-State
- Power-up reset
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT573 is a high-performance BiCMOS product designed for VCC operation at 3.3V. This device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates. The 74LVT573 has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

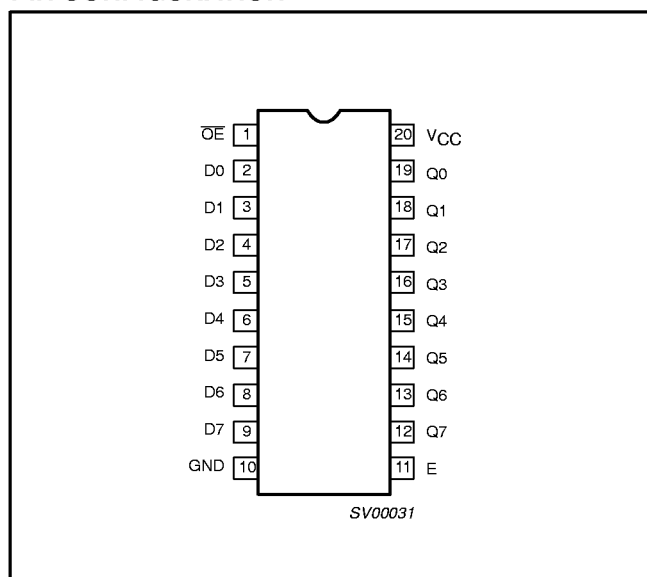
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	$C_L = 50\text{pF}; V_{CC} = 3.3\text{V}$	2.5 2.7	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 3.6\text{V}$	.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	-40°C to $+85^{\circ}\text{C}$	74LVT573 D	74LVT573 D	SOT163-1
20-Pin Plastic SSOP Type II	-40°C to $+85^{\circ}\text{C}$	74LVT573 DB	74LVT573 DB	SOT339-1
20-Pin Plastic TSSOP Type I	-40°C to $+85^{\circ}\text{C}$	74LVT573 PW	74LVT573PW DH	SOT360-1

PIN CONFIGURATION



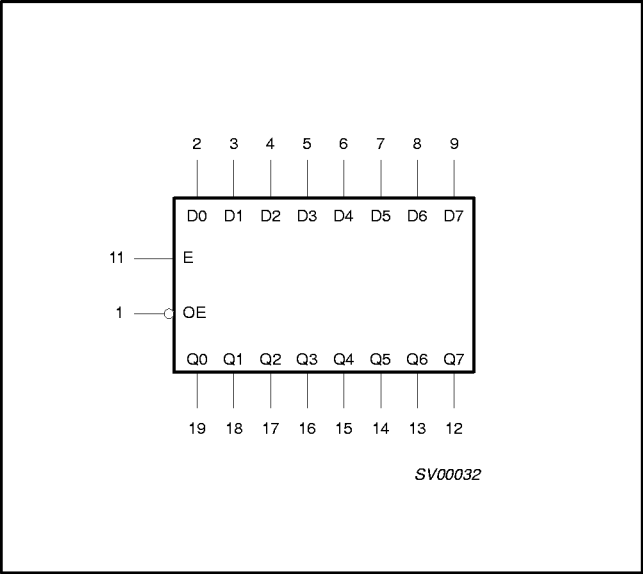
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	E	Enable input (active-High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

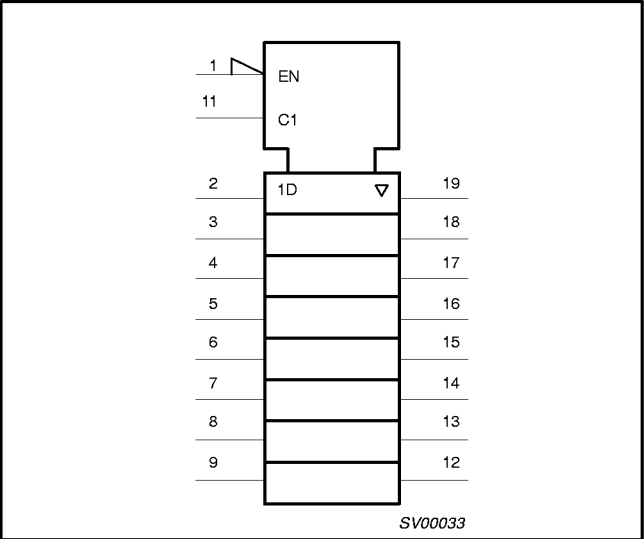
3.3V Octal D-type transparent latch
(3-State)

74LVT573

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

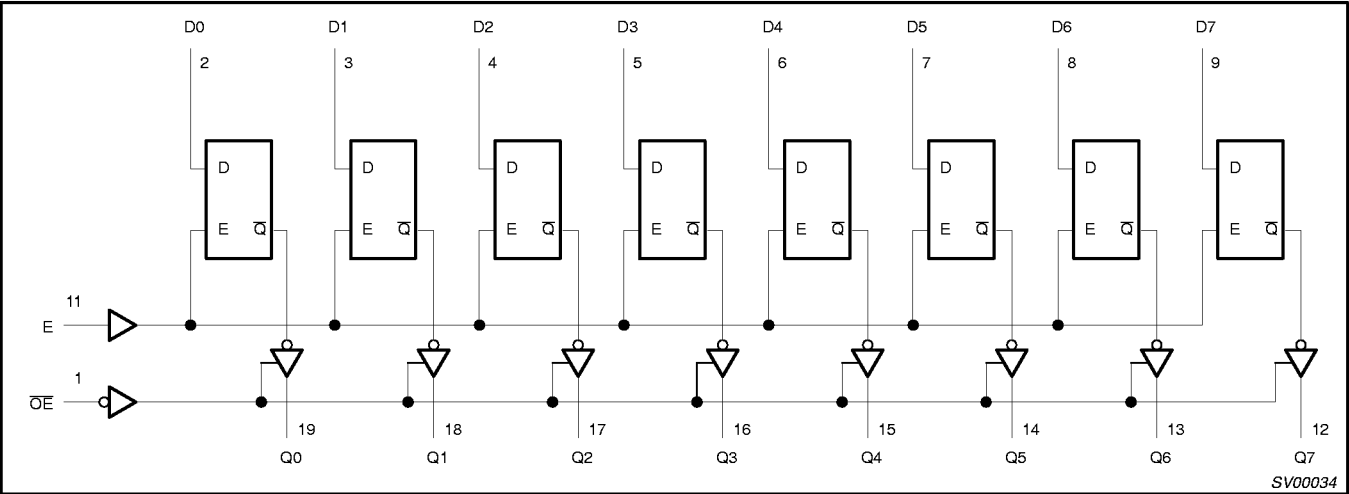


FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
OE	E	Dn		Q0 – Q7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	L	L	L	Latch and read register
L	↓	H	H	H	
L	L	X	NC	NC	Hold
H	X	X	NC	Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

LOGIC DIAGRAM



3.3V Octal D-type transparent latch (3-State)

74LVT573

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage ³		−0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage ³	Output in Off or High state	−0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, $f \geq 1$ kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

3.3V Octal D-type transparent latch (3-State)

74LVT573

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.7V; I _{IK} = −18mA			−0.9	−1.2	V
V _{OH}	High-level output voltage	V _{CC} = 2.7 to 3.6V; I _{OH} = −100μA		V _{CC} -0.2	V _{CC} -0.1		V
		V _{CC} = 2.7V; I _{OH} = −8mA		2.4	2.5		
		V _{CC} = 3.0V; I _{OH} = −32mA		2.0	2.2		
V _{OL}	Low-level output voltage	V _{CC} = 2.7V; I _{OL} = 100μA			0.1	0.2	V
		V _{CC} = 2.7V; I _{OL} = 24mA			0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 16mA			0.25	0.4	
		V _{CC} = 3.0V; I _{OL} = 32mA			0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 64mA			0.4	0.55	
V _{RST}	Power-up output low voltage ⁵	V _{CC} = 3.6V; I _O = 1mA; V _I = GND or V _{CC}			0.13	0.55	V
I _I	Input leakage current	V _{CC} = 0 or 3.6V; V _I = 5.5V			1	10	μA
		V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins		±0.1	±1	
		V _{CC} = 3.6V; V _I = V _{CC}	Data pins ⁴		0.1	1	
		V _{CC} = 3.6V; V _I = 0			−1	−5	
I _{OFF}	Output off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V			1	±100	μA
I _{HOLD}	Bus Hold current A inputs ⁷	V _{CC} = 3V; V _I = 0.8V		75	150		μA
		V _{CC} = 3V; V _I = 2.0V		−75	−150		
		V _{CC} = 0V to 3.6V; V _{CC} = 3.6V		±500			
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V			60	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = Don't care			1	±100	μA
I _{OZH}	3-State output High current	V _{CC} = 3.6V; V _O = 3V; V _I = V _{IL} or V _{IH}			1	5	μA
I _{OZL}	3-State output Low current	V _{CC} = 3.6V; V _O = 0.5V; V _I = V _{IL} or V _{IH}			−1	−5	
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0			0.13	0.19	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0			3	12	
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵			0.13	0.19	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND			0.1	0.2	mA

NOTES:

- All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND .
- This parameter is valid for any V_{CC} between $0V$ and $1.2V$ with a transition time of up to $10msec$. From $V_{CC} = 1.2V$ to $V_{CC} = 3.3V \pm 0.3V$ a transition time of $100\mu sec$ is permitted. This parameter is valid for $T_{amb} = 25^\circ C$ only.
- Unused pins at V_{CC} or GND .
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- I_{CCZ} is measured with outputs pulled to V_{CC} or GND .
- This is the bus hold overdrive current required to force the input to the opposite logic state.

3.3V Octal D-type transparent latch (3-State)

74LVT573

AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP ¹	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	2	1.0 1.0	2.5 2.7	4.2 4.3	4.7 5.2	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn	1	1.6 2.5	3.5 4.3	5.6 6.5	6.3 7.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.0 1.3	2.8 3.3	5.1 5.5	6.2 6.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	2.0 1.5	3.7 3.0	5.7 4.6	6.7 5.1	ns

NOTE:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.

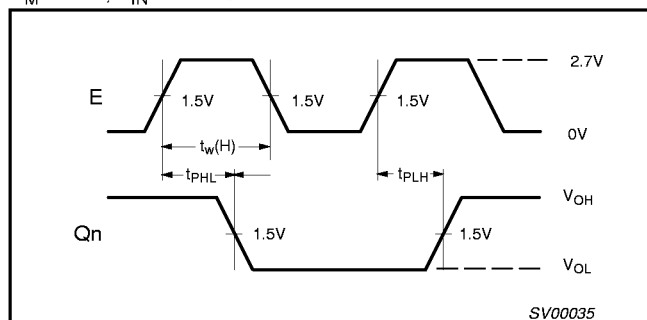
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

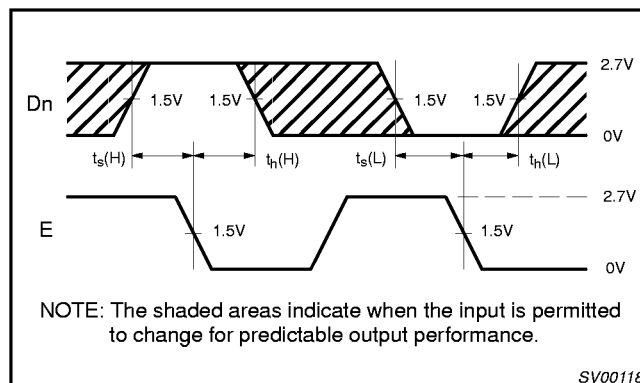
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$	
			MIN	MAX	MIN	
$t_{S(H)}$ $t_{S(L)}$	Setup time, High or Low, Dn to E	3	0.7 0.7		0.6 0.6	ns
$T_{H(H)}$ $T_{H(L)}$	Hold time, High or Low, Dn to E	3	1.6 1.6		1.8 1.8	ns
$T_W(H)$	E pulse width High	1	3.3		3.3	ns

AC WAVEFORMS

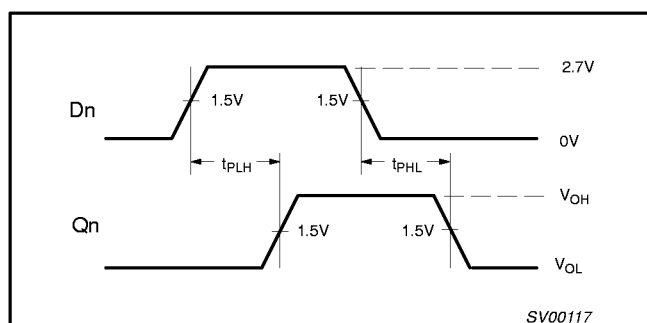
$V_M = 1.5V$, $V_{IN} = \text{GND to } 2.7V$



Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



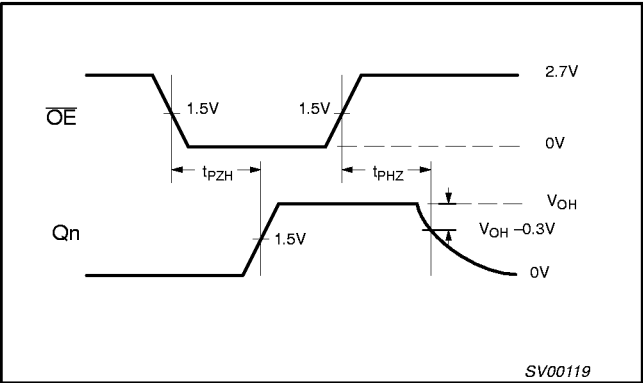
Waveform 3. Data Setup and Hold Times



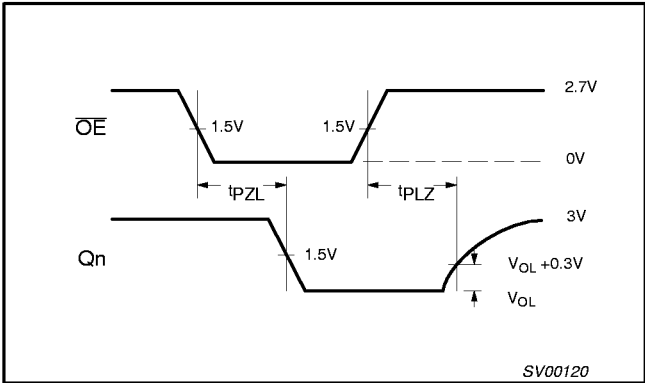
Waveform 2. Propagation Delay for Data to Outputs

3.3V Octal D-type transparent latch
(3-State)

74LVT573



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM

Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

$V_M = 1.5V$
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	$\leq 10MHz$	500ns	$\leq 2.5ns$	$\leq 2.5ns$

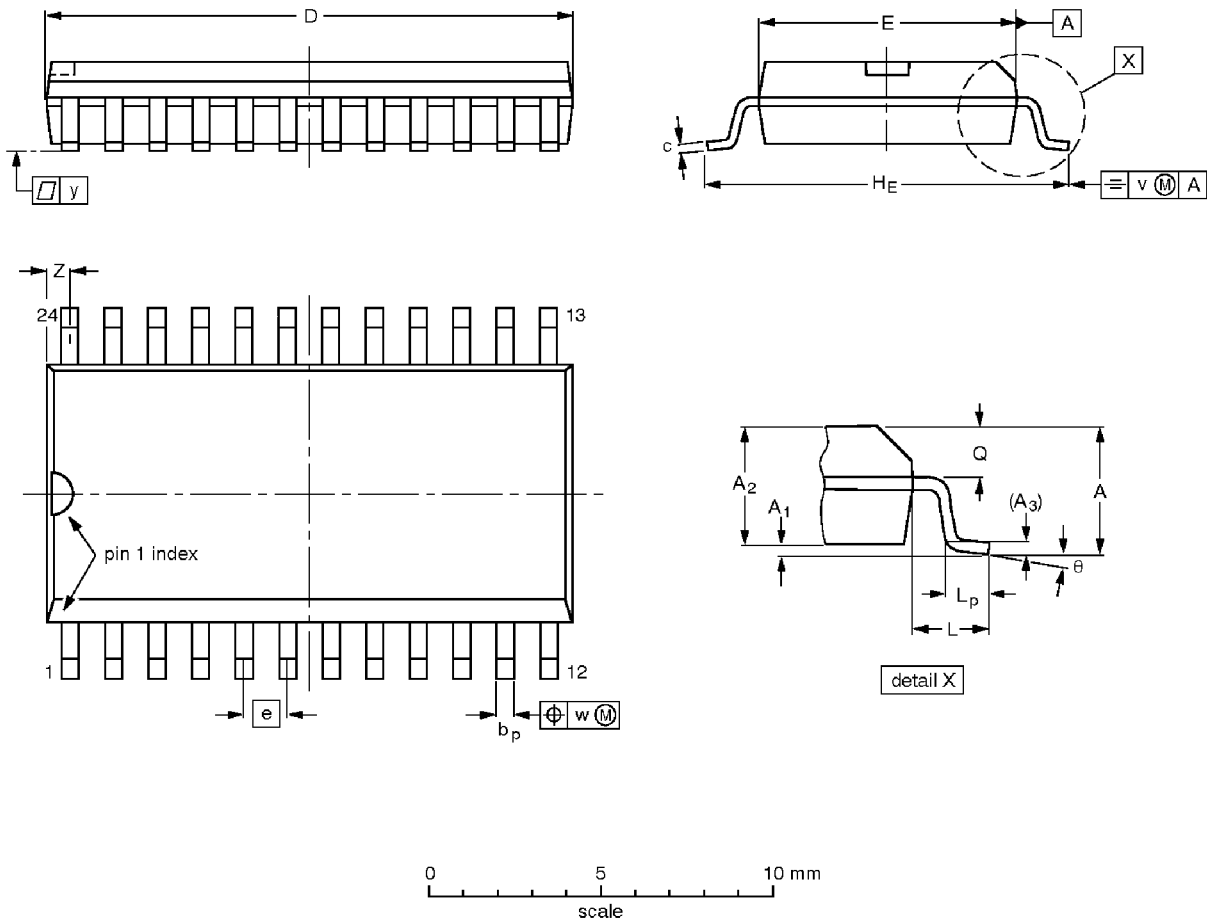
SV00092

3.3V Octal D-type transparent latch
(3-State)

74LVT573

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

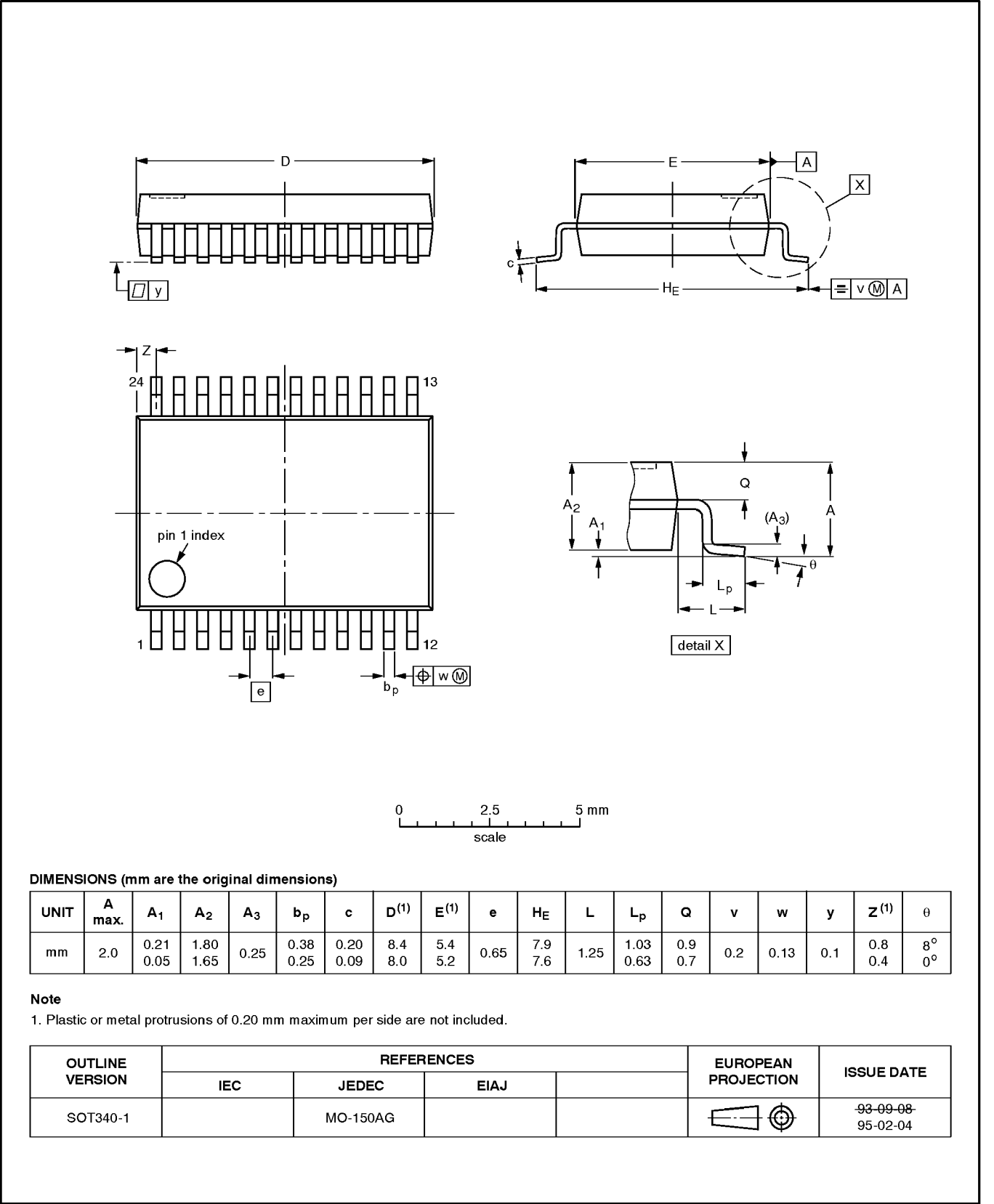
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

3.3V Octal D-type transparent latch
(3-State)

74LVT573

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



3.3V Octal D-type transparent latch
(3-State)

74LVT573

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

