National Semiconductor

PRELIMINARY
October 1995

74VHC257
Quad 2-Input Multiplexer with TRI-STATE® Outputs

General Description

The VHC257 is an advanced high speed CMOS Quad 2-Channel Multiplexer featuring TRI-STATE outputs. It is fabricated with silicon gate CMOS technology and achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of four 2-input digital multiplexers with common select and enable ($\overline{OE}$) inputs.

When the $\overline{OE}$ input is held to a logic HIGH, the outputs are switched to a high impedance state, allowing the outputs to interface directly with bus-oriented systems.

The SELECT decoding determines whether the I_{0x} or I_{1x} inputs get routed to their corresponding outputs.

An Input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

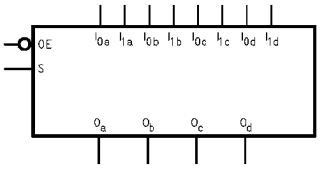
Features

- High speed
- Low power dissipation:
  I_{CC} = 4 μA (max.) at T_A = 25°C
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min.)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Wide operating voltage range: V_{CC} (opr) = 2V ~ 5.5V
- Low noise: V_{OLP} = 0.8V (max.)
- Pin and function compatible with 74HC257

Commercial	Package Number	Package Description
74VHC257M	M16A	16-Lead Molded JEDEC SOIC
74VHC257SJ	M16D	16-Lead Molded EIAJ SOIC
74VHC257MTC	MTC16	16-Lead Molded JEDEC Type 1 TSSOP
74VHC257N	N16E	16-Lead Molded DIP

Note: Surface mount packages are also available on Tapeand Reel. Specify by appending the suffix letter "X" to the ordering code.

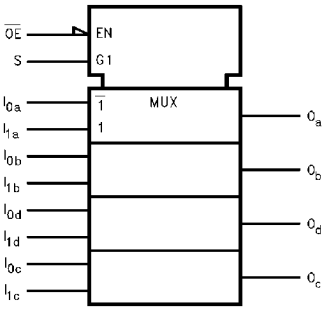
Logic Symbols



TL/F/11659–1

Pin Names	Description
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\overline{OE}$	Output Enable
S	Select Input
O_a–O_d	Outputs

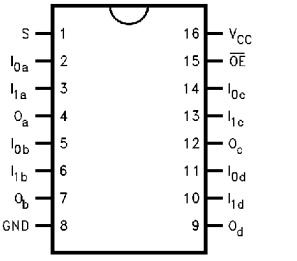
IEEE/IEC



TL/F/11659–5

Connection Diagram

Pin Assignment for DIP, TSSOP, and SOIC



TL/F/11659–2

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

 TL/F/11659

RRD-B30M125/Printed in U. S. A.

Functional Description

The 'VHC257 is a quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under the control of a Common Data Select Input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$O_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$
$O_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$
$O_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$
$O_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$

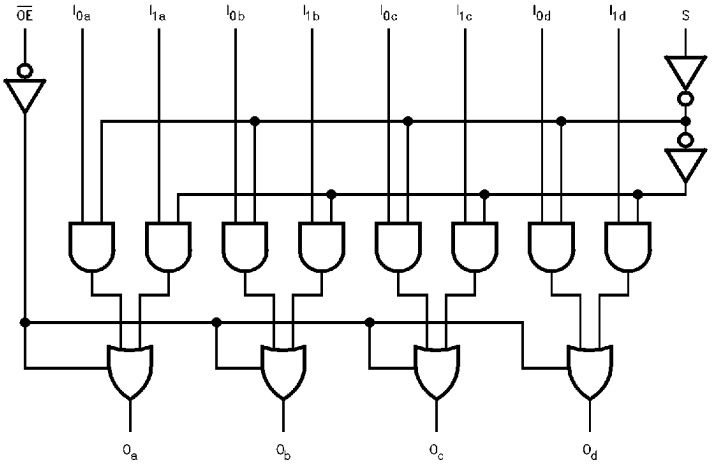
When the Output Enabler ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	O
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/11659–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices (Preliminary)

Symbol	Parameter	V_{CC} (V)	74VHC T_A = 25°C			74VHC T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0–5.5	1.50 0.7 V_{CC}			1.50 0.7 V_{CC}		V		
V_{IL}	Low Level Input Voltage	2.0 3.0–5.5			0.50 0.3 V_{CC}		0.50 0.3 V_{CC}	V		
V_{OH}	High Level Output Voltage	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0 4.5	2.58 3.94			2.48 3.80		V		I_{OH} = −4 mA I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0 4.5			0.36 0.36		0.44 0.44	V		I_{OL} = 4 mA I_{OL} = 8 mA
I_{OZ}	TRI-STATE Output Off-State Current	5.5			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

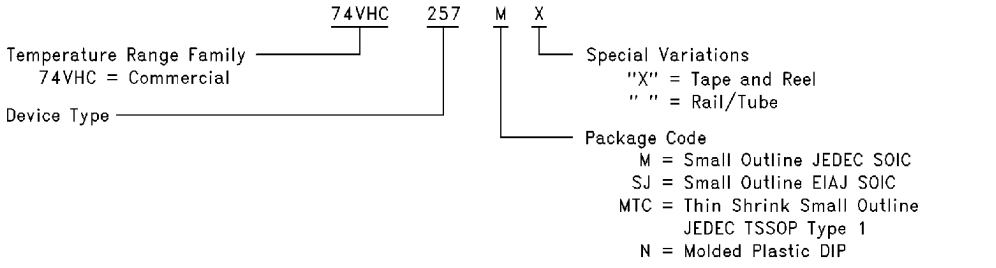
AC Electrical Characteristics (Preliminary)

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$			74VHC $T_A = -40°C$ to $+85°C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
t_{PLH}, t_{PHL}	Propagation Delay I_n to O_n	3.3 ±0.3		6.2	9.7	1.0	11.5	ns		C_L = 15 pF
				8.7	13.2	1.0	15.0			C_L = 50 pF
		5.0 ±0.5		4.1	6.4	1.0	7.5	ns		C_L = 15 pF
				5.6	8.4	1.0	9.5			C_L = 50 pF
t_{PLH}, t_{PHL}	Propagation Delay S to O_n	3.3 ±0.3		8.4	13.2	1.0	15.5	ns		C_L = 15 pF
				10.9	16.7	1.0	19.0			C_L = 50 pF
		5.0 ±0.5		5.3	8.1	1.0	9.5	ns		C_L = 15 pF
				6.8	10.1	1.0	11.5			C_L = 50 pF
t_{PZL}, t_{PZH}	TRI-STATE Output Enable Time	3.3 ±0.3		8.7	13.6	1.0	16.0	ns	R_L = 1 kΩ	C_L = 15 pF
				11.2	17.1	1.0	19.5			C_L = 50 pF
		5.0 ±0.5		5.6	8.6	1.0	10.0	ns		C_L = 15 pF
				7.1	10.6	1.0	12.0			C_L = 50 pF
t_{PLZ}, t_{PHZ}	TRI-STATE Output Disable Time	3.3 ±0.3						ns	R_L = 1 kΩ	C_L = 50 pF
		5.0 ±0.5						ns		C_L = 50 pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{OUT}	Output Capacitance							pF	V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance			20				pF	(Note 1)	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}.

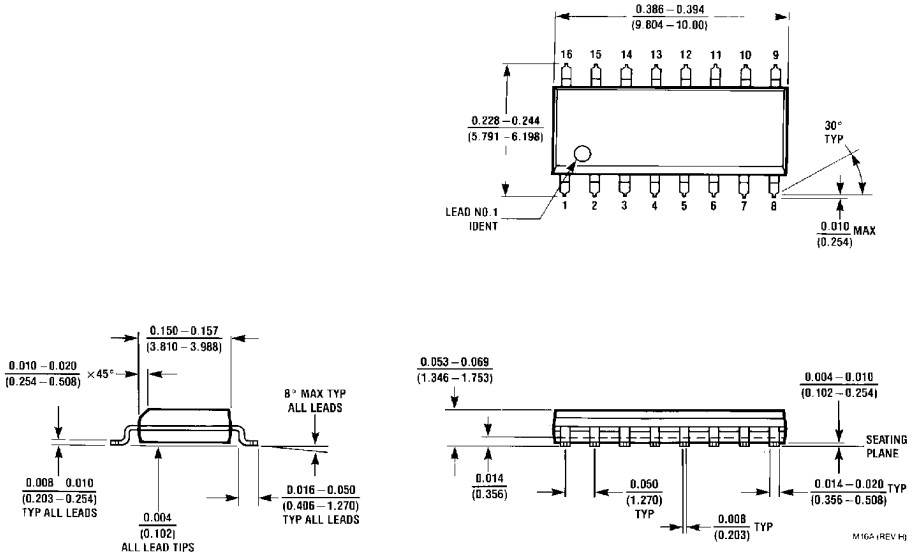
Ordering Information

The device number is used to form part of a simplified purchasing code, where the package type and temperature range are defined as follows:



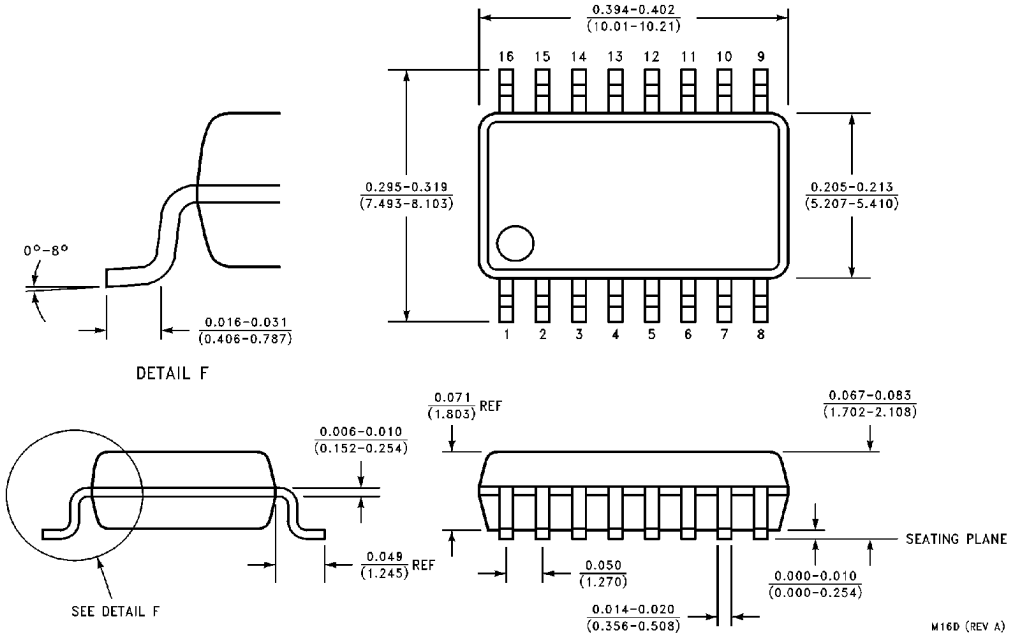
TL/F/11659–4

Physical Dimensions inches (millimeters)



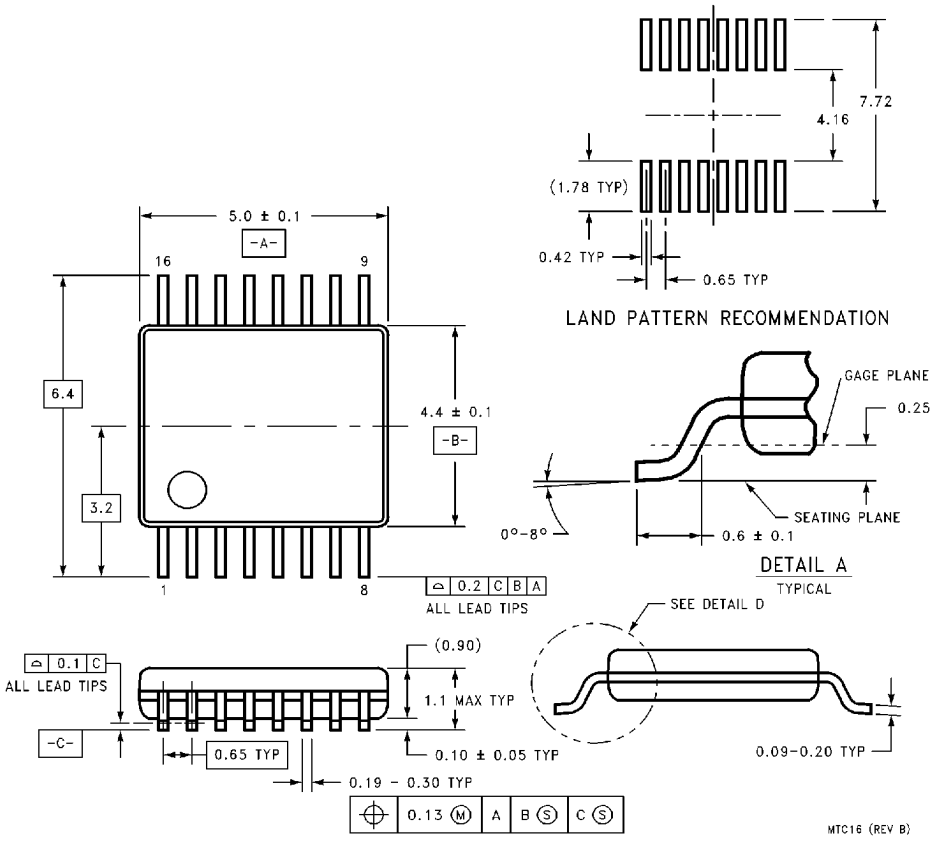
16-Lead Small Outline Integrated Circuit—JEDEC (M)
Order Number 74VHC257M
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Small Outline Package-EIAJ (SJ)
Order Number 74VHC257SJ
NS Package Number M16D

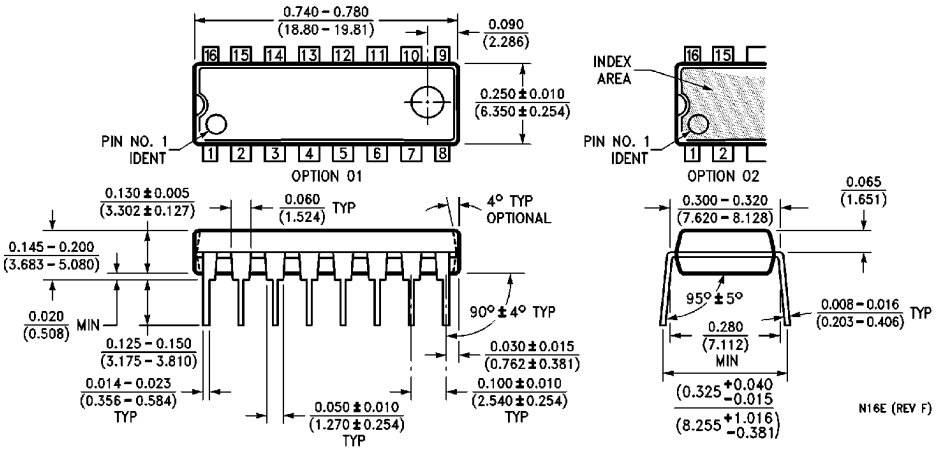
Physical Dimensions (millimeters) (Continued)



All dimensions are in millimeters.

16-Lead Molded Thin Shrink Small Outline Package; JEDEC
Order Number 74VHC257MTC
NS Package Number MTC16

Physical Dimensions inches (millimeters) (Continued)



16-Lead (0.300″ Wide) Molded Dual-In-Line Package
Order Number 74VHC257N
NS Package Number N16E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408