74VHCT16245A

16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS (NON INVERTED)

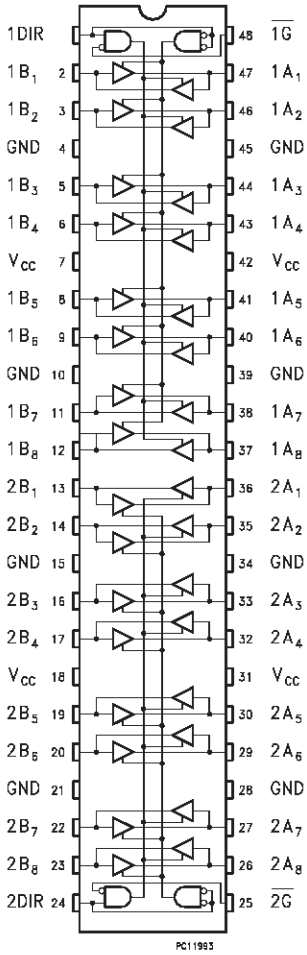
- HIGH SPEED: t_{PD} = 4.5 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION: I_{CC} = 4 µA (MAX.) at T_A=25°C
- COMPATIBLE WITH TTL OUTPUTS: V_{IH} = 2V (MIN.), V_{IL} = 0.8V (MAX)
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 8 mA (MIN)
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: V_{CC}(OPR) = 4.5V to 5.5V
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: V_{OLP} = 0.9V (MAX.)

TSSOP

ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74VHCT16245ATTR

PIN CONNECTION



DESCRIPTION

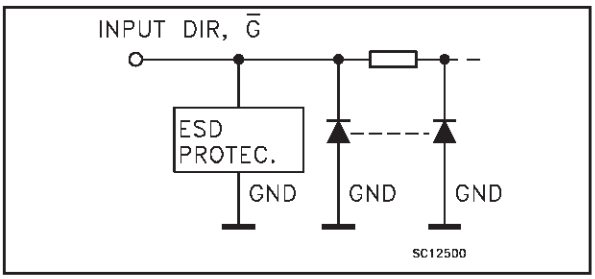
The 74VHCT16245A is an advanced high-speed CMOS 16-BIT BUS TRANSCEIVER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.

This IC is intended for two-way asynchronous communication between data busses; the direction of data transmission is determined by DIR input. The enable input $\overline{G}$ can be used to disable the device so that the busses are effectively isolated.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

All floating bus terminals during High Z State must be held HIGH or LOW.

INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

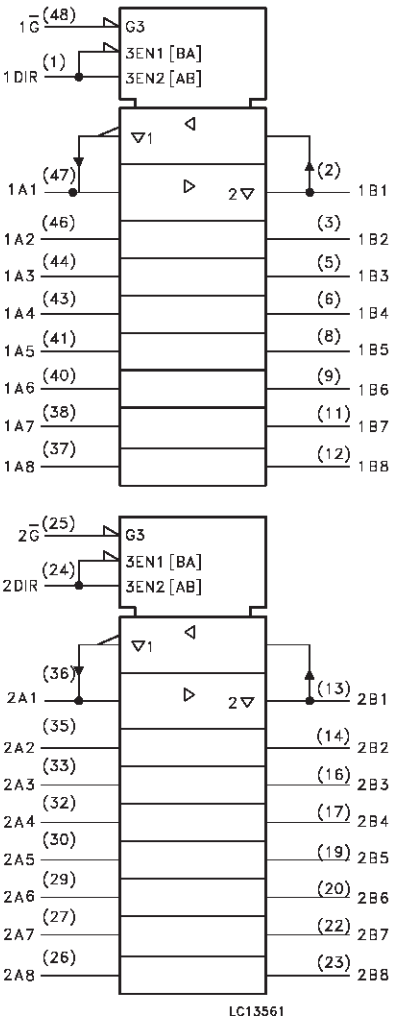
PIN No	SYMBOL	NAME AND FUNCTION
1	1DIR	Directional Control
2, 3, 5, 6, 8, 9, 11, 12	1B1 to 1B8	Data Inputs/Outputs
13, 14, 16, 17, 19, 20, 22, 23	2B1 to 2B8	Data Inputs/Outputs
24	2DIR	Directional Control
25	$2\overline{G}$	Output Enable Input
36, 35, 33, 32, 30, 29, 27, 26	2A1 to 2A8	Data Inputs/Outputs
47, 46, 44, 43, 41, 40, 38, 38	1A1 to 1A8	Data Inputs/Outputs
48	$1\overline{G}$	Output Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS		FUNCTION		OUTPUT
$\overline{G}$	DIR	A BUS	B BUS	Yn
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	Z	Z	Z

X : Don't Care
Z : High Impedance

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage (DIR, $\overline{G}$)	-0.5 to +7.0	V
$V_{I/O}$	DC BUS I/O Voltage (see note 1)	-0.5 to +7.0	V
$V_{I/O}$	DC BUS I/O Voltage (see note 2)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 75	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
1) Output in OFF State
2) High or Low State

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
$V_{I/O}$	BUS I/O Voltage (see note 1)	0 to 5.5	V
$V_{I/O}$	BUS I/O Voltage (see note 2)	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (see note 3) (V_{CC} = 5.0 ± 0.5V)	0 to 20	ns/V

1) Output in OFF State
2) High or Low State
3) VIN from 0.8V to 2V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5		2			2		2		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	I_O=-50 µA	4.4	4.5		4.4		4.4		V
		4.5	I_O=-8 mA	3.94			3.8		3.7		
V_{OL}	Low Level Output Voltage	4.5	I_O=50 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=8 mA			0.36		0.44		0.55	
Ioz	High Impedance Output Leakage Current	5.5	$V_I = V_{IH}$ or V_{IL} V_O = 0V to 5.5V			±0.25		± 2.5		± 2.5	µA
I_I	Input Leakage Current	0 to 5.5	V_I = 5.5V or GND			± 0.1		± 1.0		± 1.0	µA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND			4		40		40	µA
I_{CC}	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V_{CC} or GND			1.35		1.5		1.5	mA
I_{OPD}	Output Leakage Current	0	V_{OUT} = 5.5V			0.5		5.0		5.0	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3ns)

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (*) (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time	5.0	15			4.5	7.5	1.0	8.5	1.0	10.0	ns
		5.0	50			5.3	8.7	1.0	9.5	1.0	11.0	
t_{PZL} t_{PZH}	Output Enable Time	5.0	15	RL = 1KΩ		9.0	13.8	1.0	15.0	1.0	16.0	ns
		5.0	50			9.7	14.8	1.0	16.0	1.0	17.0	
t_{PLZ} t_{PHZ}	Output Disable Time	5.0	50	RL = 1KΩ		10.0	15.4	1.0	16.5	1.0	17.5	ns
t_{OSLH} t_{OSHL}	Output to Output Skew Time (note 1)	5.0	50				1.0		1.0		1.0	ns

(*) Voltage range is 5.0V ± 0.5V

Note 1 : Parameter guaranteed by design. $t_{soLH} = |t_{pLHm} - t_{pLHn}|$, $t_{soHL} = |t_{pHLm} - t_{pHLn}|$

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Value							Unit
			T_A = 25°C			-40 to 85°C		-55 to 125°C		
			Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance			6	10		10		10	pF
$C_{I/O}$	Bus Input Capacitance			8						pF
C_{PD}	Power Dissipation Capacitance (note 1)			18						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per circuit)

DYNAMIC SWITCHING CHARACTERISTICS

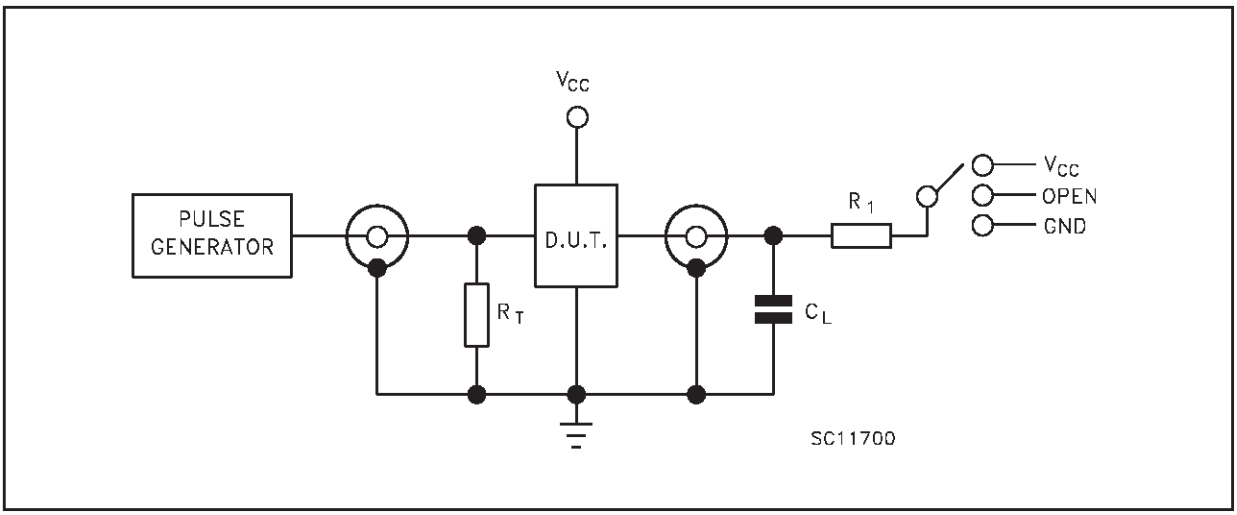
Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C_L = 50 pF		0.6	0.9					V
V_{OLV}				-0.9	-0.6						
V_{IHD}	Dynamic High Voltage Input (note 1, 3)	5.0		2.0							
V_{ILD}	Dynamic Low Voltage Input (note 1, 3)	5.0				0.8					

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.0V. Inputs under test switching: 3.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

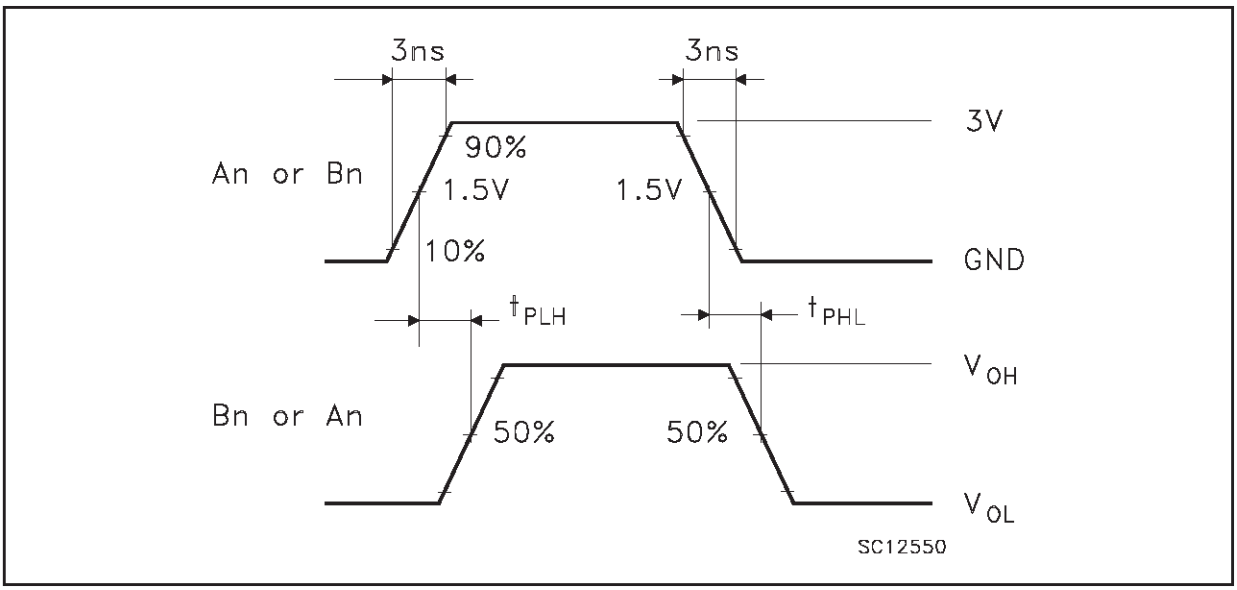
TEST CIRCUIT



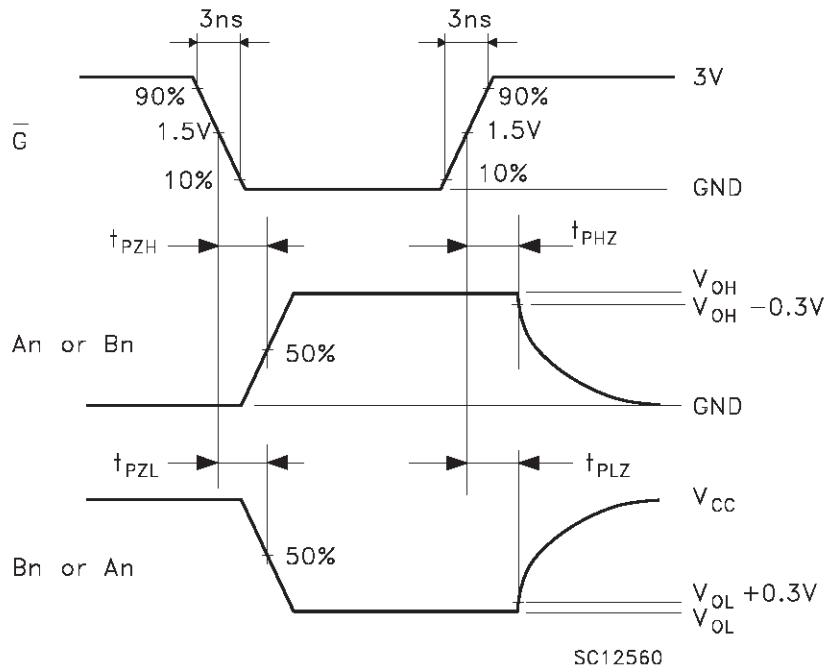
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

C_L =15/ 50pF or equivalent (includes jig and probe capacitance)
$R_L = R_1$ = 1KΩ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.408		0.496
E	7.95		8.25	0.313		0.325
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030