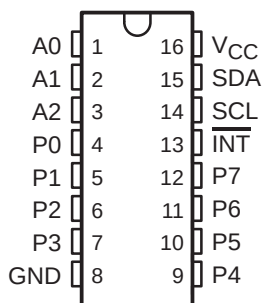


PCF8574 REMOTE 8-BIT I/O EXPANDER FOR I²C BUS

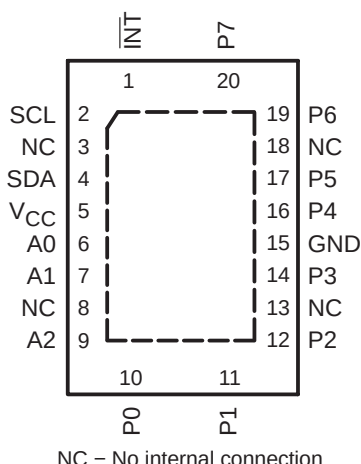
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- Low Standby-Current Consumption of 10 μ A Maximum
- I²C to Parallel-Port Expander
- Open-Drain Interrupt Output
- Compatible With Most Microcontrollers
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

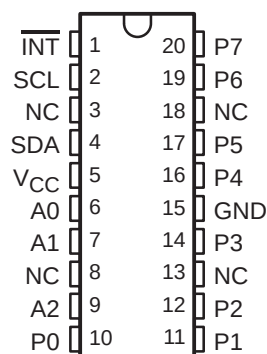
DW OR N PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



DGV OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

This 8-bit input/output (I/O) expander for the two-line bidirectional bus (I²C) is designed for 2.5-V to 6-V V_{CC} operation.

The PCF8574 provides general-purpose remote I/O expansion for most microcontroller families via the I²C interface [serial clock (SCL), serial data (SDA)].

The device features an 8-bit quasi-bidirectional I/O port (P0–P7), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source to V_{CC} is active. An additional strong pullup to V_{CC} allows fast rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs.

ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	PCF8574RGYR	PF574
	PDIP – N	Tube	PCF8574N	PCF8574N
	SOIC – DW	Tube	PCF8574DW	PCF8574
		Tape and reel	PCF8574DWR	
	TSSOP – PW	Tape and reel	PCF8574PWR	PF574
	TVSOP – DGV	Tape and reel	PCF8574DGVR	PF574

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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PCF8574

REMOTE 8-BIT I/O EXPANDER FOR I²C BUS

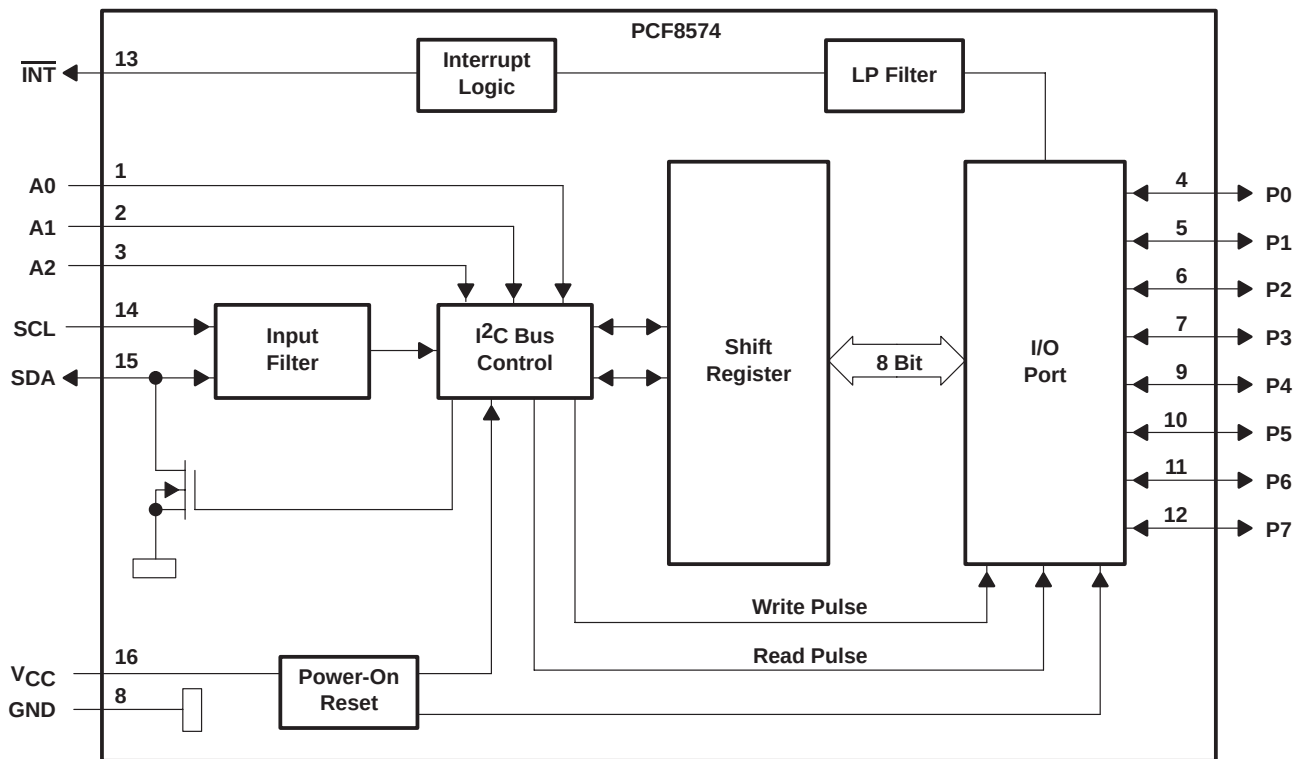
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description/ordering information (continued)

The PCF8574 provides an open-drain output ($\overline{\text{INT}}$) that can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{IV} , $\overline{\text{INT}}$ is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from, or written to, the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge bit after the rising edge of the SCL signal or in the write mode at the acknowledge bit after the high-to-low transition of the SCL signal. Interrupts that occur during the acknowledge clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and, after the next rising clock edge, is transmitted as $\overline{\text{INT}}$. Reading from, or writing to, another device does not affect the interrupt circuit.

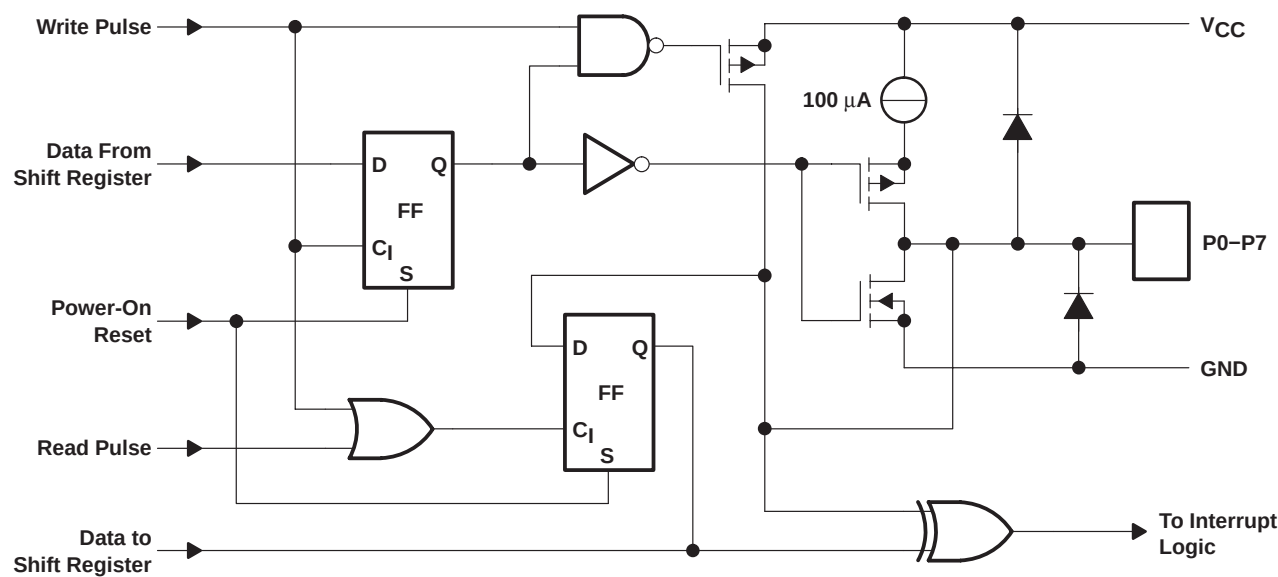
By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C bus. Therefore, the PCF8574 can remain a simple slave device.

logic diagram (positive logic)



Pin numbers shown are for the DW and N packages.

simplified schematic diagram of each P-port input/output



I²C interface

I²C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA I/O while the SCL input is high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit ($\overline{R/\overline{W}}$). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the start and the stop conditions.

The data byte follows the address acknowledge. If the $\overline{R/\overline{W}}$ bit is high, the data from this device are the values read from the P port. If the $\overline{R/\overline{W}}$ bit is low, the data are from the master, to be output to the P port. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the master, following the acknowledge, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data will be valid at time t_{PV} after the low-to-high transition of SCL and during the clock cycle for the acknowledge.

A stop condition, which is a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the master.

INTERFACE DEFINITION

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I ² C slave address	L	H	L	L	A2	A1	A0	$\overline{R/\overline{W}}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

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ADDRESS REFERENCE

INPUTS			I ² C-BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$)	–20 mA
Input/Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±400 μ A
Continuous output low current, I_{OL} ($V_O = 0$ to V_{CC})	50 mA
Continuous output high current, I_{OH} ($V_O = 0$ to V_{CC})	–4 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2): DGV package	92°C/W
(see Note 2): DW package	57°C/W
(see Note 2): N package	67°C/W
(see Note 2): PW package	83°C/W
(see Note 3): RGY package	37°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions

	MIN	MAX	UNIT
V_{CC} Supply voltage	2.5	6	V
V_{IH} High-level input voltage	$0.7 \times V_{CC}$	$V_{CC} + 0.5$	V
V_{IL} Low-level input voltage	–0.5	$0.3 \times V_{CC}$	V
I_{OH} High-level output current		–1	mA
I_{OL} Low-level output current		25	mA
T_A Operating free-air temperature	–40	85	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{IK}	Input diode clamp voltage	I _I = -18 mA	2.5 V to 6 V	-1.2			V
V _{POR}	Power-on reset voltage [‡]	V _I = V _{CC} or GND, I _O = 0	6 V		1.3	2.4	V
I _{OH}	P port	V _O = GND	2.5 V to 6 V	30		300	μA
I _{OHT}	P-port transient pullup current	High during acknowledge V _{OH} = GND	2.5 V		-1		mA
I _{OL}	SDA	V _O = 0.4 V	2.5 V to 6 V	3			mA
	P port	V _O = 1 V	5 V	10	25		
	INT	V _O = 0.4 V	2.5 V to 6 V	1.6			
I _I	SCL, SDA	V _I = V _{CC} or GND	2.5 V to 6 V			±5	μA
	INT					±5	
	A0, A1, A2					±5	
I _{IHL}	P port	V _I ≥ V _{CC} or V _I ≤ GND	2.5 V to 6 V			±400	μA
I _{CC}	Operating mode	V _I = V _{CC} or GND, I _O = 0, f _{SCL} = 100 kHz	6 V		40	100	μA
	Standby mode	V _I = V _{CC} or GND, I _O = 0			2.5	10	
C _i	SCL	V _I = V _{CC} or GND	2.5 V to 6 V		1.5	7	pF
C _{io}	SDA	V _{IO} = V _{CC} or GND	2.5 V to 6 V		3	7	pF
	P port				4	10	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] The power-on reset circuit resets the I²C-bus logic with V_{CC} < V_{POR} and sets all I/Os to logic high (with current source to V_{CC}).

I²C interface timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		MIN	MAX	UNIT
f _{SCL}	I ² C clock frequency		100	kHz
t _{sch}	I ² C clock high time	4		μs
t _{scl}	I ² C clock low time	4.7		μs
t _{sp}	I ² C spike time		100	ns
t _{sds}	I ² C serial data setup time	250		ns
t _{sdh}	I ² C serial data hold time	0	900	ns
t _{icr}	I ² C input rise time		1	μs
t _{icf}	I ² C input fall time		0.3	μs
t _{ocf}	I ² C output fall time (10-pF to 400-pF bus)		300	ns
t _{buf}	I ² C-bus free time between stop and start	4.7		μs
t _{sts}	I ² C start or repeated start condition setup	4.7		μs
t _{sth}	I ² C start or repeated start condition hold	4		μs
t _{sps}	I ² C stop-condition setup	4		μs
t _{vd}	Valid data time	SCL low to SDA output valid		3.4 μs
C _b	I ² C-bus capacitive load		400	pF



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switching characteristics over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{pv}	Output data valid	SCL	P port		4	μs
t _{su}	Input data setup time	P port	SCL	0		μs
t _h	Input data hold time	P port	SCL	4		μs
t _{iv}	Interrupt valid time	P port	$\overline{\text{INT}}$		4	μs
t _{ir}	Interrupt reset delay time	SCL	$\overline{\text{INT}}$		4	μs

PARAMETER MEASUREMENT INFORMATION

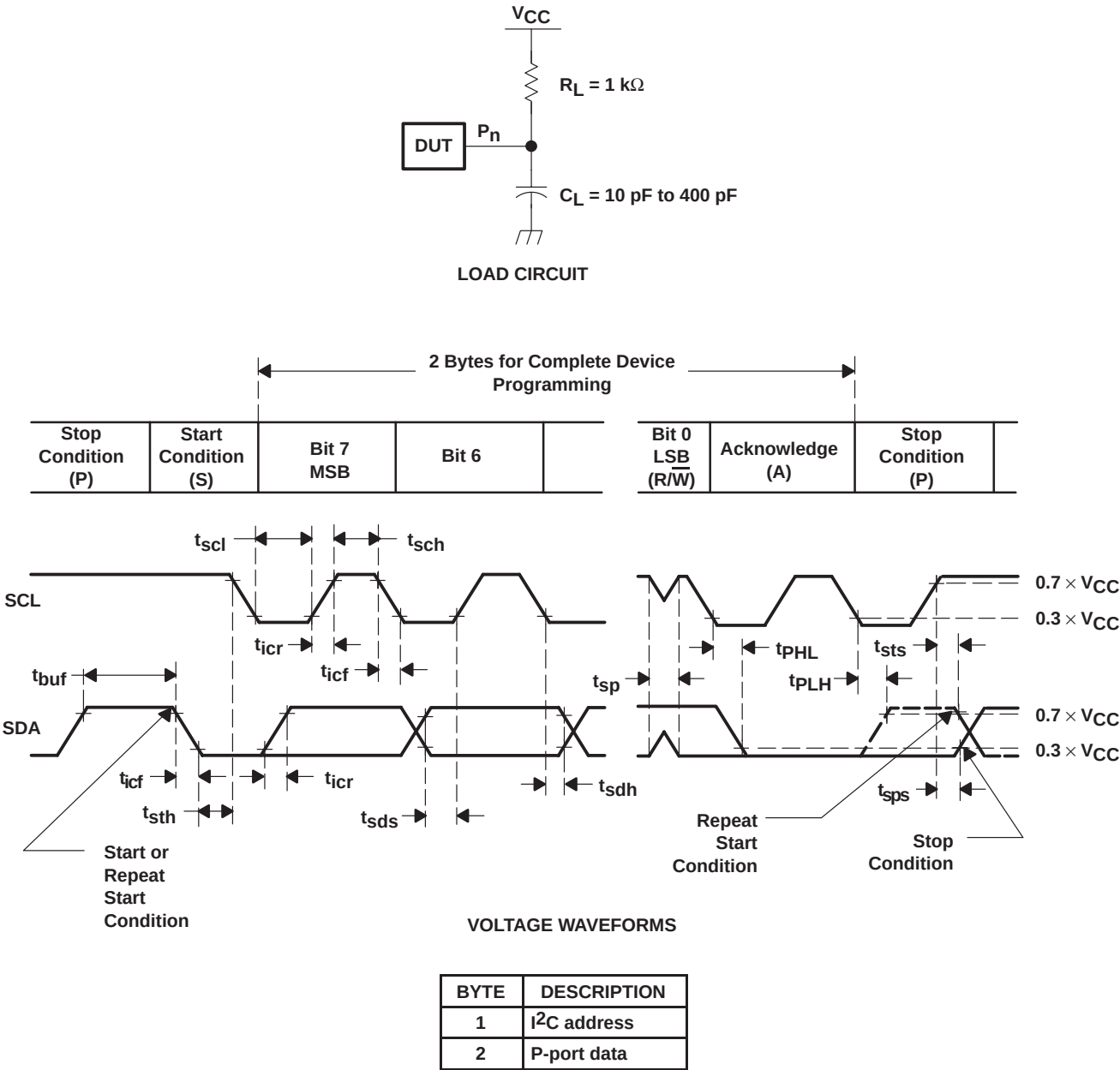


Figure 1. I²C Interface Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

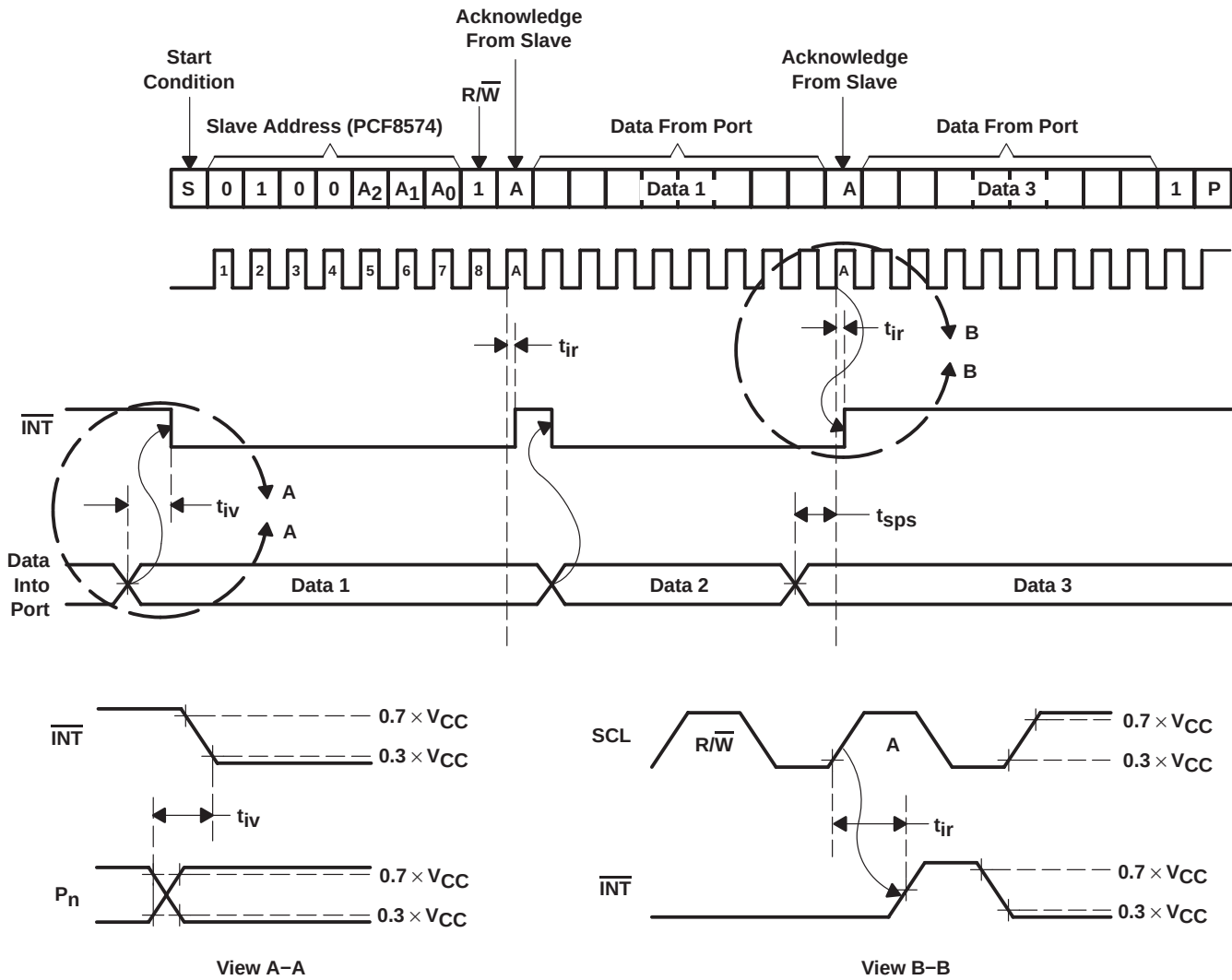


Figure 2. Interrupt-Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

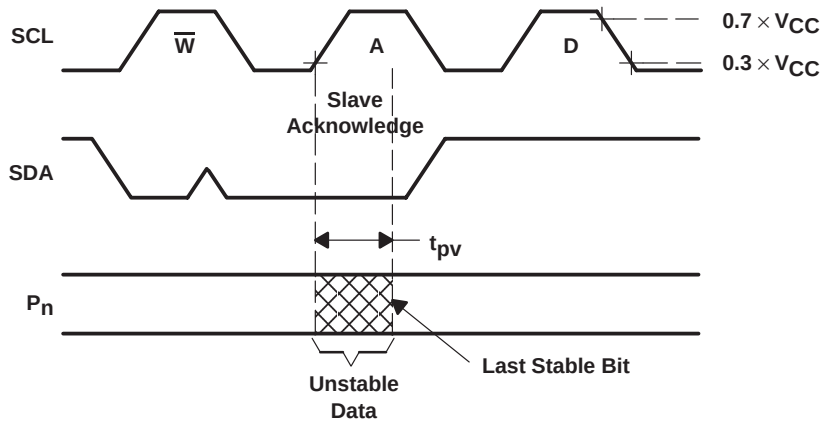


Figure 3. Write-Mode Timing

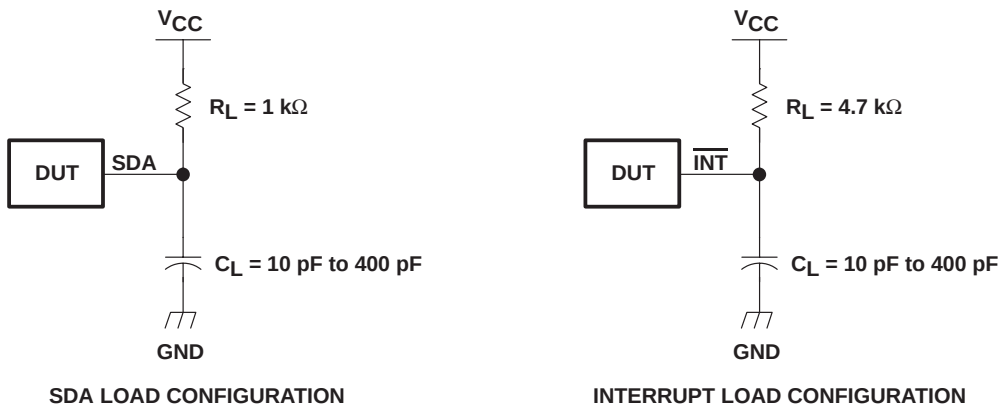


Figure 4. Load Circuits

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
PCF8574DGVR	ACTIVE	TVSOP	DGV	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
PCF8574DW	ACTIVE	SOIC	DW	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
PCF8574DWR	ACTIVE	SOIC	DW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
PCF8574N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
PCF8574PW	ACTIVE	TSSOP	PW	20	70	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
PCF8574PWR	ACTIVE	TSSOP	PW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
PCF8574RGYR	ACTIVE	QFN	RGY	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

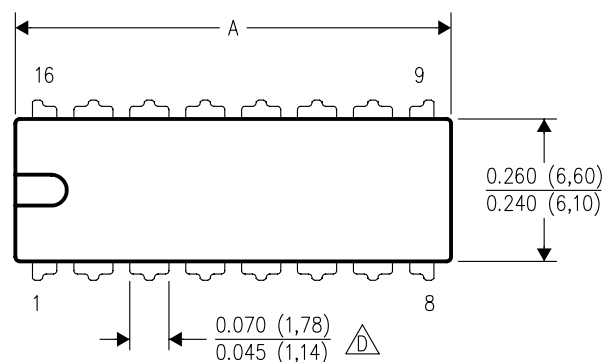
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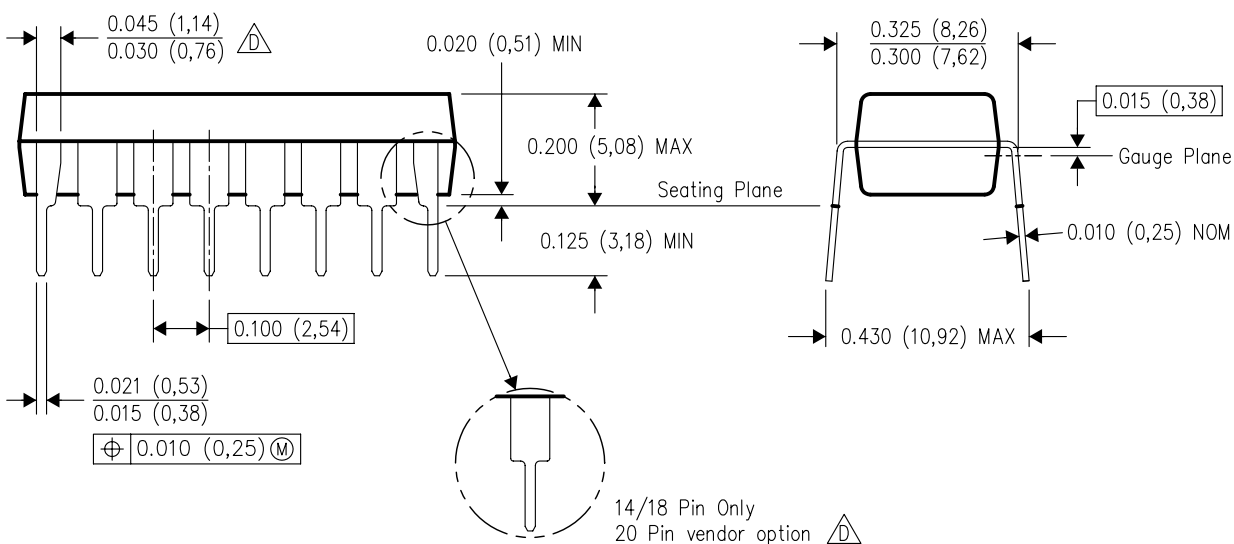
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

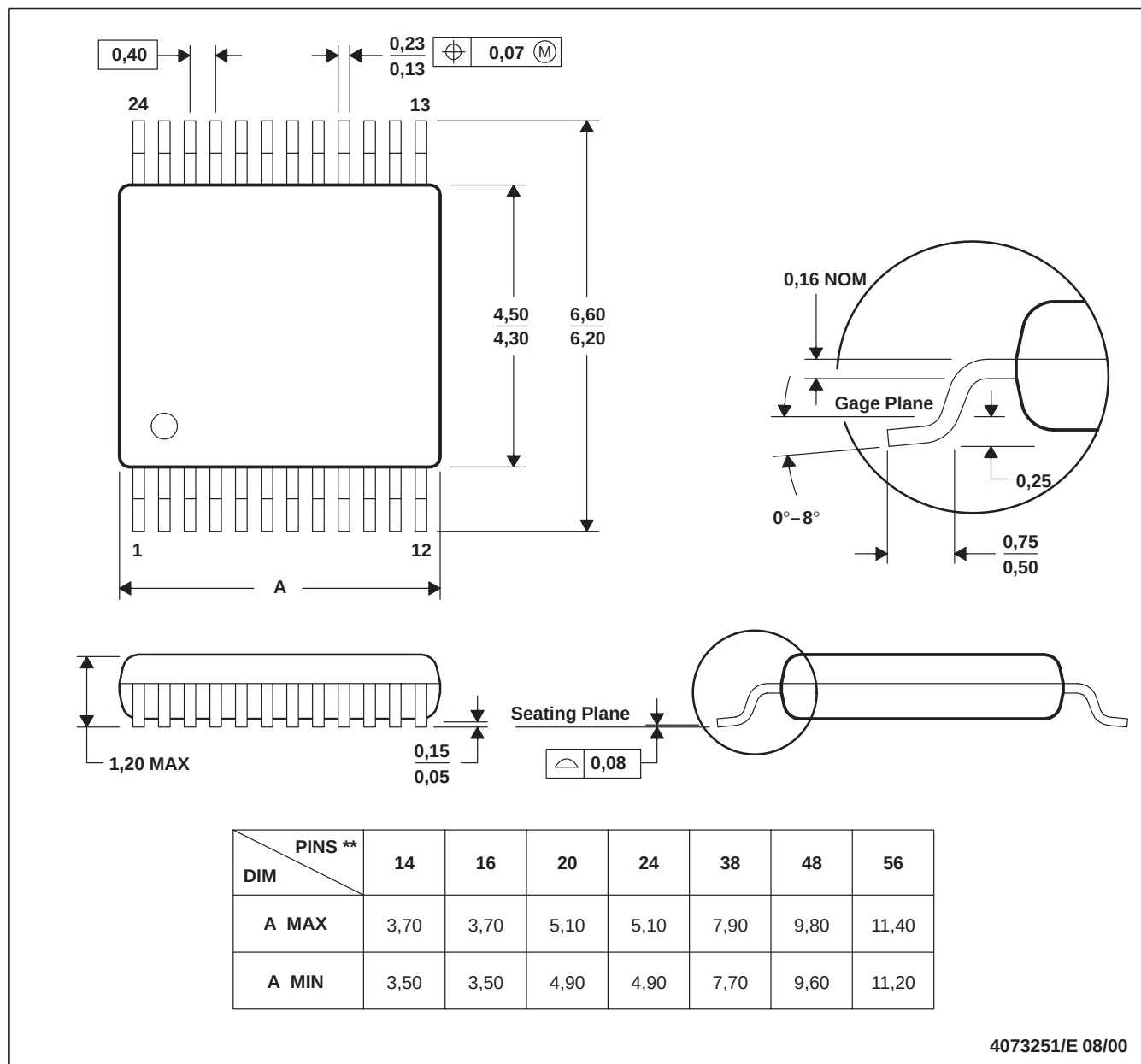
NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

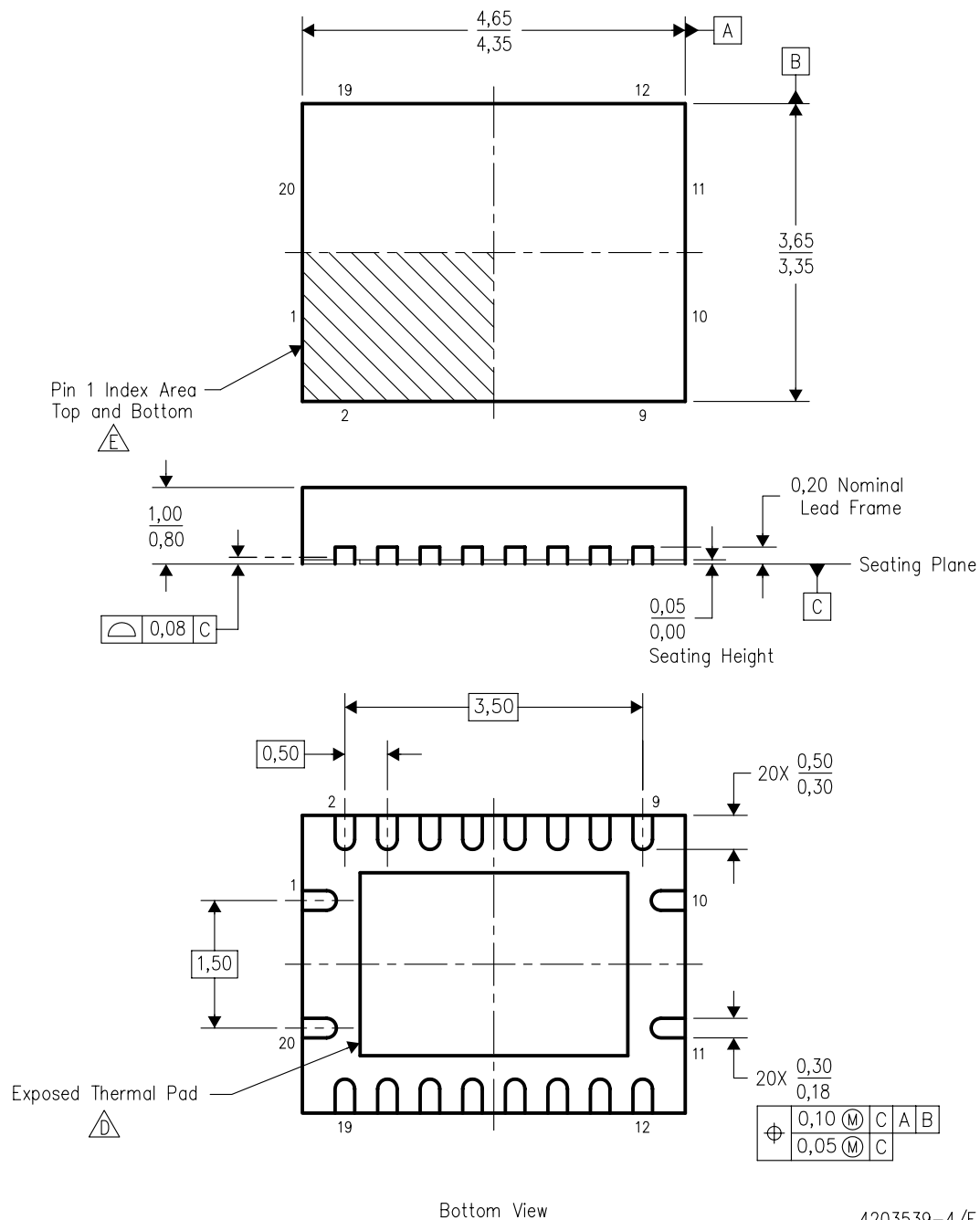
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



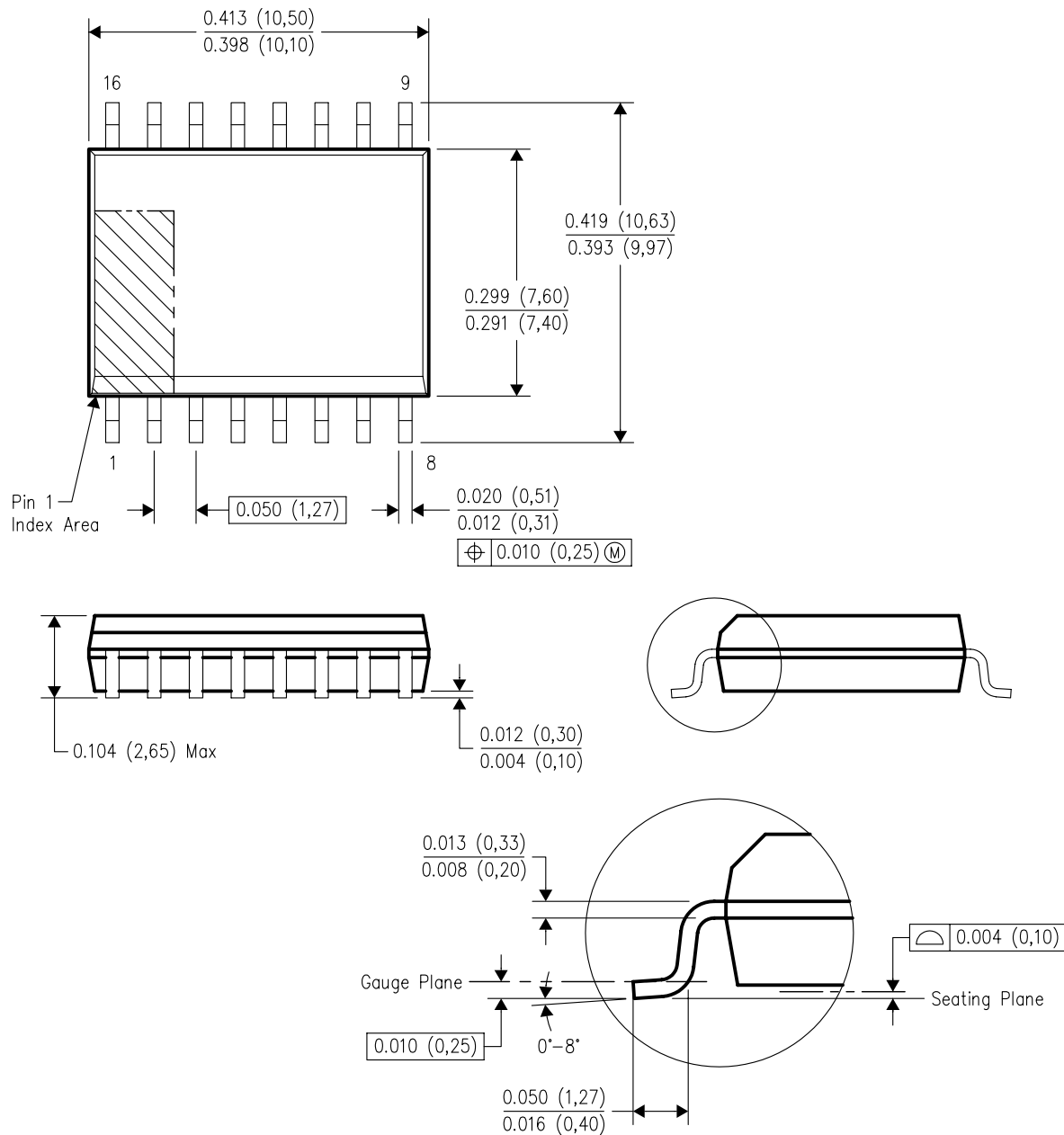
Bottom View

4203539-4/F 02/2005

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BC.

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



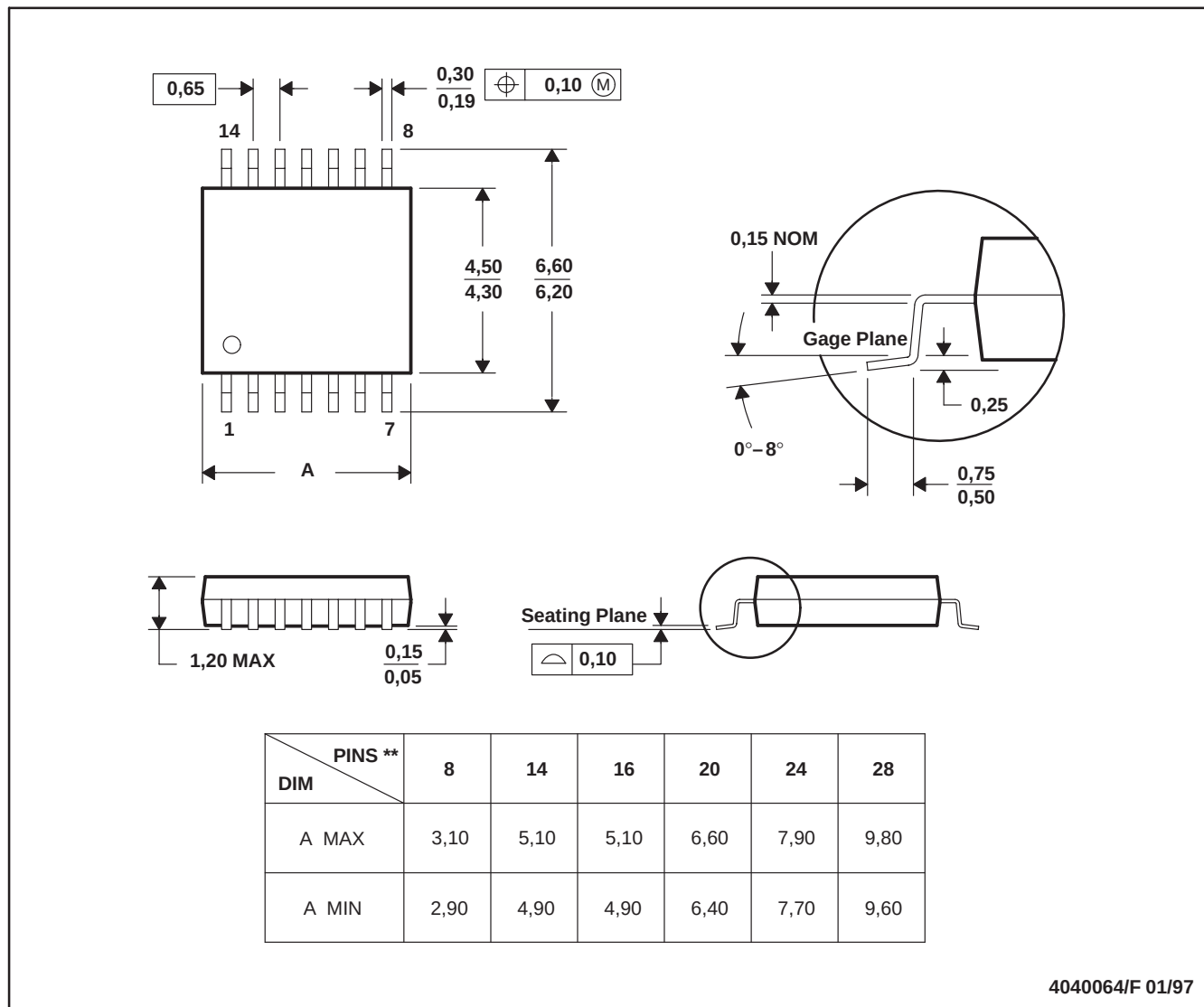
4040000-2/F 06/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AA.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
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