

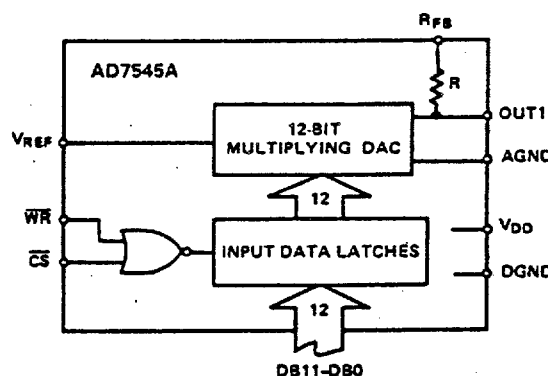
12 Bit D/A Converter - Radiation Hardened 7545ARP

CMOS 12-Bit Buffered Multiplying
Digital to Analog Converter

For Space Applications

SEI's 7545ARP (RP for RAD-PAK®) is a 12-bit CMOS multiplying DAC with internal data latches, features a minimum of 100kilorad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® packing technology, the 7545ARP features a $\overline{WR}$ pulse width of 100ns which allows interfacing to

a much wider range of fast 8-bit and 16-bit microprocessors. It is loaded by a single 12-bit wide word under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing unbuffered operation of the DAC. The 7545ARP is particularly suitable for single supply operations and applications with wide temperature variations.



7545ARP Functional Block Diagram



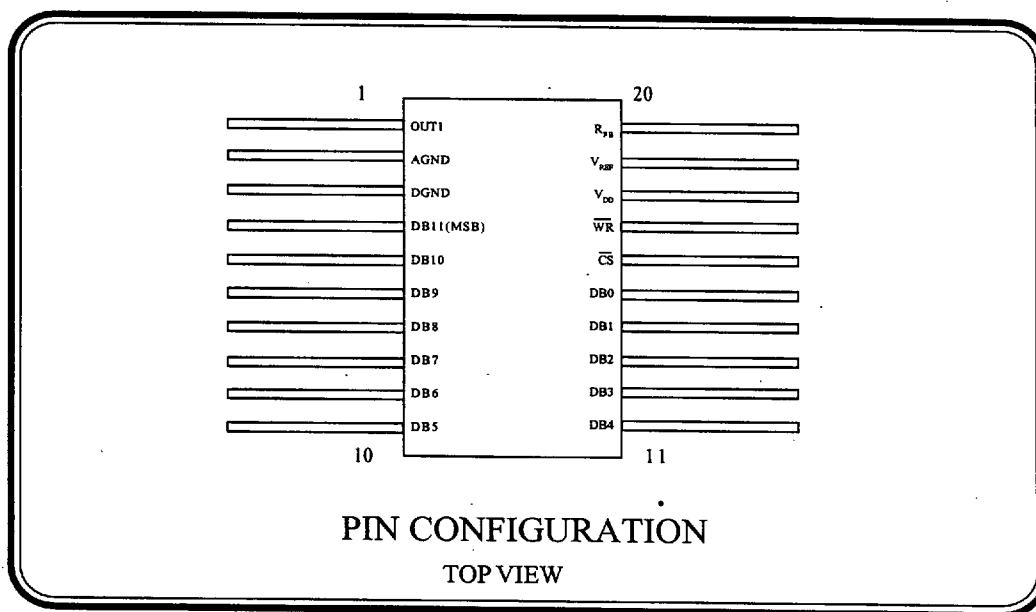
SPACE
ELECTRONICS
INCORPORATED

Tel: (619) 452-4167 Fax: (619) 452-5499

SEI 7545ARP RADHARD 12BIT DtoA CONVERTER

Radiation Hardened 7545ARP

CMOS 12 Bit Buffered Multiplying
Digital to Analog Converter



Features:

- 12-Bit Resolution
- Pin Compatible with Analog Devices AD7545A
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness > 100krad (Si)
- Excellent Single Event Effects
 - SEL LET Threshold > 120MeV/mg/cm²
 - SEU LET Threshold > 120MeV/mg/cm²
- Package:
 - 20 Pin RAD-PAK® Flat Pack
 - 20 Pin RAD-PAK® DIP
- Low Gain Temperature Coefficient:
 - 2ppm/°C typ.
- Fast Interface Timing
- Single +5V to +15V Supply

Specifications and design are subject to change without notice.



June, 1996

For Further Information Contact:

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7545ARP ABSOLUTE MAXIMUM RATINGS

(T_A = +25 °C unless otherwise noted)

PARAMETER	SYMBOL	MIN	MAX	UNITS
V _{DD} to DGND		-0.3	+17	V
Digital Input Voltage to DGND		-0.3	V _{DD} + 0.3	V
V _{RFB} , V _{REF} to DGND			+25	V
V _{PIN1} to DGND		-0.3	V _{DD} + 0.3	V
AGND to DGND		-0.3	V _{DD} + 0.3	V
Power Dissipation to +75°C Derates above +75°C by	Pd		450 6	mW mW/°C
Operating Temperature		-55	+125	°C
Storage Temperature Range	T _s	-65	+150	°C

7545ARP SPECIFICATIONS

(V_{DD} = +5V, T_A = -55°C to +125°C unless otherwise noted.)

Test	Symbol	Device	Min	Max	Test Condition / Comments	Units
Resolution	RES	-1,2		12		Bits
Relative Accuracy	RA	-1,2		1/2		± LSB
Differential Nonlinearity	DNL	-1, 2		1	12-Bit Monotonic T _{min} to T _{max}	± LSB
Gain Error	A _E	-1 -2		4 2	DAC Register Loaded with 1111 1111 1111	± LSB
Gain Temp. Coeff.	TC _{AE}	-1,2		5		± ppm/°C
Power Supply Rejection	PSRR	-1, 2		0.004	V _{DD} = ±5%	± %/%
Output Leakage Current	OUT1	-1, 2		200	DB0 - DB11 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V	± nA
Output Current Settling Time	t _{SL}	-1		1	To + 1/2LSB; OUT1 Load = 100Ω, DAC Output Measured from Falling Edge of $\overline{WR}$. $\overline{CS}$ = 0V	μs



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754SARP SPECIFICATIONS (continue)
 $(V_{DD} = +5V, T_A = -55^{\circ}C \text{ to } +125^{\circ}C \text{ unless otherwise noted.})$

Test	Symbol	Device	Min	Max	Test Condition / Comments	Units
Feedthrough Error	FT	-1, 2		10		mVp-p
Reference Input Resistance Pin 19 to Ground	R_{IN}	-1, 2	10	20		k Ω
Digital Input High Voltage	V_{IH}	-1, 2	2.4			V
Digital Input Low Voltage	V_{IL}	-1, 2		0.8		V
Digital Input Leakage Current	I_{IN}	-1, 2		10	$V_{IN} = 0V \text{ or } V_{DD}$	$\pm\mu A$
Digital Input Capacitance	C_{IN}	-1, 2		8	DB0 - DB11; $\overline{WR}, \overline{CS}$	pF
Output Capacitance	C_{OUT1}	-1, 2		70	DB0 - DB11 = 0V, $\overline{WR}, \overline{CS} = 0V$	pF
				150	DB0 - DB11 = V_{DD} , $\overline{WR}, \overline{CS} = 0V$	
Chip Select to Write Setup Time	t_{CS}	-1, 2	170		$t_{CS} \geq t_{WR}, t_{CH} \geq 0$	ns
Chip Select to Write Hold Time	t_{CH}	-1, 2	0			
Write Pulse Width	t_{WR}	-1, 2	170			
Data Setup Time	t_{DS}	-1, 2	150			
Data Hold Time	t_{DH}	-1, 2	5			
Supply Current from V_{DD}	I_{DD}	-1, 2		2	All Digital Inputs V_{IL} or V_{IH}	mA
				100	All Digital Inputs 0 or V_{DD}	μA



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7545ARP SPECIFICATIONS
($V_{DD} = +15V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$ unless otherwise noted.)

Test	Symbol	Device	Min	Max	Test Condition / Comments	Units
Resolution	RES	-1,2		12		Bits
Relative Accuracy	RA	-1,2		1/2		$\pm$ LSB
Differential Nonlinearity	DNL	-1, 2		1	12-Bit Monotonic T_{min} to T_{max}	$\pm$ LSB
Gain Error	A_E	-1		4	DAC Register Loaded with 1111 1111 1111	$\pm$ LSB
		-2		2		
Gain Temp. Coeff.	TC_{AE}	-1,2		5		$\pm$ ppm/ $^{\circ}C$
Power Supply Rejection	PSRR	-1, 2		0.004	$V_{DD} = \pm 5\%$	$\pm$ %/%
Output Leakage Current	OUT1	-1, 2		200	DB0 - DB11 = 0V; $\overline{WR}$, $\overline{CS} = 0V$	$\pm$ nA
Output Current Settling Time	t_{SL}	-1		1	To + 1/2LSB; OUT1 Load = 100 Ω , DAC Output Measured from Falling Edge of $\overline{WR}$. $\overline{CS} = 0V$	μs
Feedthrough Error	FT	-1, 2		10		mVp-p
Reference Input Resistance Pin 19 to Ground	R_{IN}	-1, 2	10	20		k Ω
Digital Input High Voltage	V_{IH}	-1, 2	13.5			V
Digital Input Low Voltage	V_{IL}	-1, 2		1.5		V
Digital Input Leakage Current	I_{IN}	-1, 2		10	$V_{IN} = 0V$ or V_{DD}	$\pm \mu A$
Digital Input Capacitance	C_{IN}	-1, 2		8	DB0 - DB11; $\overline{WR}$, $\overline{CS}$	pF
Output Capacitance	C_{OUT1}	-1, 2		70	DB0 - DB11 = 0V, $\overline{WR}$, $\overline{CS} = 0V$	pF
				150	DB0 - DB11 = V_{DD} , $\overline{WR}$, $\overline{CS} = 0V$	



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7545ARP SPECIFICATIONS (continue)
 ($V_{DD} = +15V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$ unless otherwise noted.)

Test	Symbol	Device	Min	Max	Test Condition / Comments	Units
Chip Select to Write Setup Time	t_{CS}	-1, 2	95		$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	ns
Chip Select to Write Hold Time	t_{CH}	-1,2	0			
Write Pulse Width	t_{WR}	-1,2	95			
Data Setup Time	t_{DS}	-1,2	80			
Data Hold Time	t_{DH}	-1,2	5			
Supply Current from V_{DD}	I_{DD}	-1,2		2	All Digital Inputs V_{IL} or V_{IH}	mA
				100	All Digital Inputs 0 or V_{DD}	μA



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7545ARP PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	OUT1	Output Current
2	AGND	Analog Ground
3	DGND	Digital Ground
4	DB 11	Data Bit 11 (MSB)
5	DB 10	Data Bit 10
6	DB 9	Data Bit 9
7	DB 8	Data Bit 8
8	DB 7	Data Bit 7
9	DB 6	Data Bit 6
10	DB 5	Data Bit 5
11	DB 4	Data Bit 4
12	DB 3	Data Bit 3
13	DB 2	Data Bit 2
14	DB 1	Data Bit 1
15	DB 0	Data Bit 0 (LSB)
16	$\overline{CS}$	Chip Select (Active Low)
17	$\overline{WR}$	Write (Active Low)
18	V _{DD}	Digital Supply Voltage
19	V _{REF}	Reference Input
20	R _{FB}	Feedback Resistance



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