Beckman Series 7555 and 7556 MICROPROCESSOR COMPATIBLE CMOS 12-BIT A-TO-D CONVERTERS

Effective date: March, 1979

Beckman Series 7555 and 7556 are the first CMOS 12-bit Successive Approximation Analog-to-Digital Converters to offer the combination of complete 8-bit microprocessor compatibility, real 12-bit accuracy, and TTL or CMOS logic output compatibility within a single package. Their features include:

- Low Cost
- 12-bit resolution
- ±½ LSB linearity
- No missing codes
- 50 μs conversion time
- Three-state outputs for direct data bus drive
- Microprocessor compatible 4-bit/8-bit output bytes for direct 12-bit output to an 8-bit data bus
- Serial and parallel output
- TTL or CMOS logic compatibility
- Commercial and military temperature range versions
- Low power CMOS circuitry
- All thin film resistors for superior stability and precision performance
- Internal clock can operate at user preset frequency or synchronized to system clock
- Ratiometric operation

Three-State Outputs

All digital outputs for Series 7555 and 7556 are three-state outputs to allow maximum application flexibility. This facilitates a variety of busing schemes for the data bit outputs as well as the Serial Register Output and the End of Conversion output.

Microprocessor Compatibility

The three-state output buffers for each data bit parallel output are separated into a 4-bit MSB byte and an 8-bit LSB byte. Each bit grouping has a separate inhibit line—LBI for the LSB's and HBI for theMSB's —to control when each group drives the data bus.

True 12-bit Performance

±½ LSB linearity (±0.012% FSR) is guaranteed over the full operating temperature range for each model of Series 7555. Similarly, worst case limits are specified for initial gain setting error and gain error temperature coefficient for both the 7555 and 7556 and for the Series 7556, zero offset and zero offset temperature coefficient are guaranteed.

Serial and Parallel Outputs

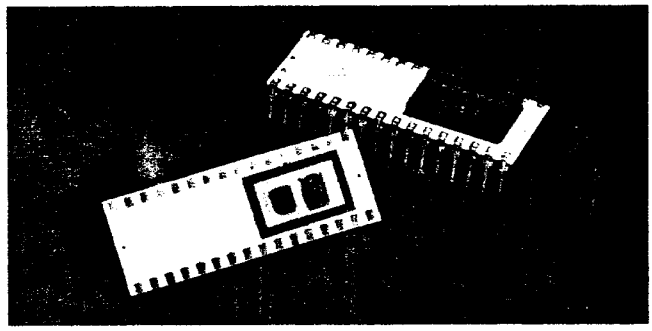
Both serial and parallel outputs are available with the Serial Register Output (SRO) outputting data after each bit decision. The parallel output word is available after the rise of the End of Conversion (EOC) output.

TTL or CMOS Compatible

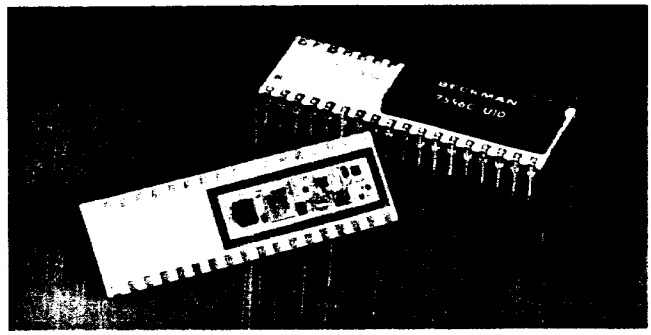
All of the digital outputs can drive TTL or CMOS gates depending on the supply levels chosen. All digital outputs are capable of driving one 54/74 gate loads or four 54LS/74LS gate loads.

Military and Commercial Versions

Commercial versions are available in a polymer sealed package (eg., 7555C) with performance specifications guaranteed over 0°C to +70°C. The Mil performance versions utilize a hermetically sealed package with performance guaranteed over −55°C to +125°C (e.g., 7555M).



Series 7555 12-Bit A-to-D Converter With Clock



Series 7556 Complete 12-Bit A-to-D Converter With Clock, Reference and Comparator

Internal Configuration

Precision thin film nichrome resistors are deposited on an alumina substrate to achieve optimum stability and uncompromised linearity and tracking performance. A separate CMOS chip contains the control logic, internal clock, successive approximation registers, three-state output buffers, and switches and is silicon nitride passivated to insure high reliability performance for both commercial and military requirements. These devices are assembled on a thick film substrate to provide the most cost effective overall assembly.

Both Complete and Building Block Models Available

Series 7555 provides a flexible A-to-D converter building block by including the successive approximation register, switch and clock chip and the thin film ladder network and input scaling resistor. It allows the external addition of a comparator and any reference between +10V and −10V for optimum flexibility. Series 7556 is a complete A-to-D converter, including the 7555 circuitry, plus a high speed comparator and a precision −10V reference.

Both series can take advantage of the same logic input/output flexibility, but the 7556 also solves the interface design considerations in marrying the ladder and switches to a fast comparator.

Very Low Power Consumption

Both Series 7555 and 7556 offer an excellent speed-power trade-off. The 7556, including reference and high speed comparator, provides a full 12-bit conversion in 50 μs while typically consuming only 200 mW.

Either model is an ideal choice for battery or DC-to-DC converter operated analog input systems.

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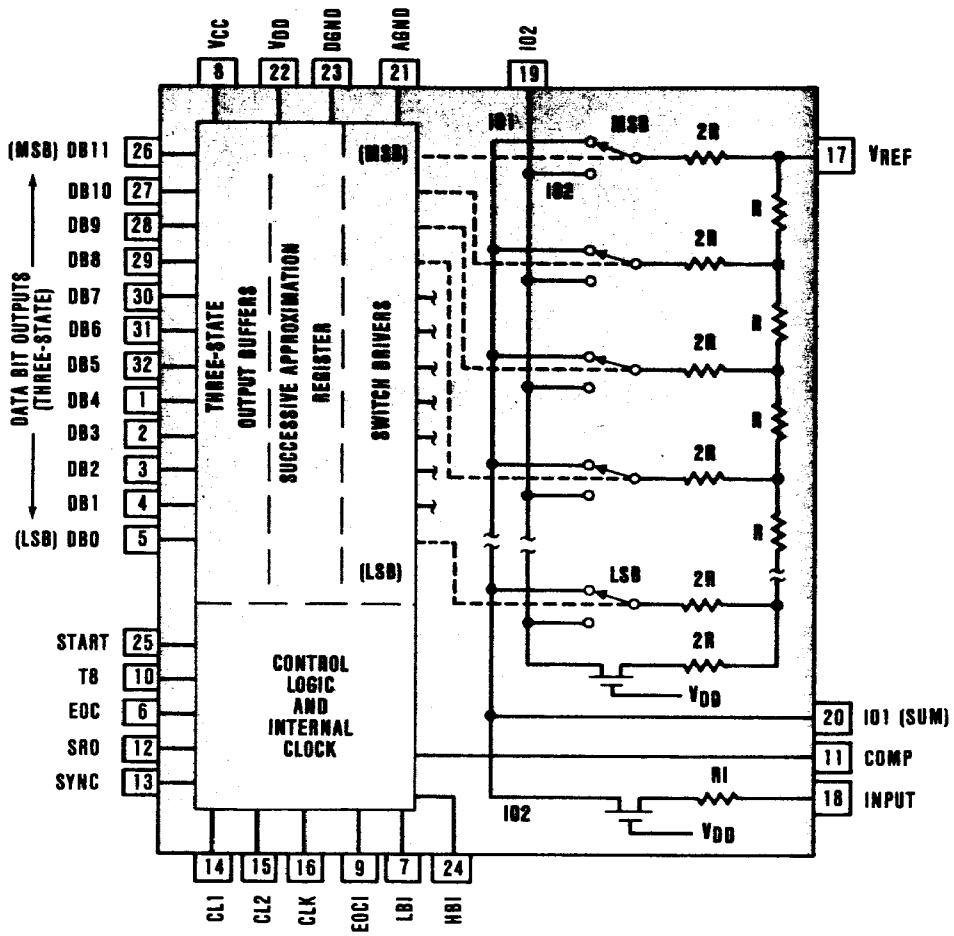


Figure 1. Series 7555 Block Diagram

Series 7555 Operation

As shown in Figure 1, Series 7555 uses an inverted R-2R ladder configuration and CMOS switches to develop binary weighted currents at I01. This current is summed against the current developed by the input voltage across RI for input to the external comparator at pin 20. The comparator decision on each bit trial is fed back to the control logic at pin 11 to reject or retain each bit tried. The resulting decision is available during the next clock period at the Serial Register Output (SRO) as well as each parallel Data Bit Output (DB11 through DB0). The full 12-bit parallel word will be available at the parallel Data Bit outputs following the rise of End Of Conversion (see timing section).

Internal Compensation

The "on" resistances of the CMOS switches are binary weighted with the MSB set at 30Ω. Linearity is dependent upon the ratio accuracies of the switch resistances and not upon their absolute values. Excellent switch ratio tolerances account for small linearity errors over the operating temperature range specified. Also, the low power density inherent in the CMOS switch configuration eliminates transient thermal gradients normally encountered with bipolar current switches.

The input resistor RI also has series FET compensation for the absolute magnitude of the switch resistances to maintain the proper gain relationship over temperature. This is a unique feature of Beckman CMOS converter designs which improves supply rejection associated with switch resistance changing in response to CMOS chip supply variations.

Operating Modes

Both the 7555 and 7556 can be operated with internal or external clock. The internal clock frequency is established by external components (see Clock Frequency Setting section). Both models can be configured to execute continuous conversions or single conversions upon command.

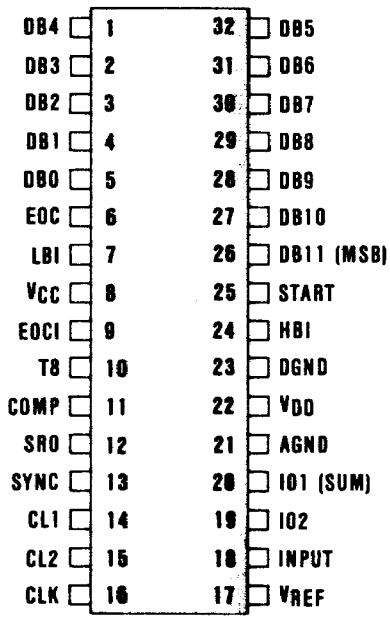


Figure 2. Series 7555 Pin Assignments

Table I—Series 7555 Performance Specifications (Note 1)

	Parameter		Conditions	Minimum	Typical	Maximum	Units
Accuracy	Resolution					12	Bits
	Linearity		Guaranteed Over Operating Temperature Range		±¼	±½	LSB
	Differential Linearity				±½		LSB
	No Missing Codes		Over Operating Temperature Range		Guaranteed		—
	Input Gain Setting (Note 2)		T_C = +25°C		±0.07	±0.2	%FSR
	Gain Tempco (Note 3)	7555C	Guaranteed Over Operating Temperature Range		±2	±5	p/10⁶FSR/°C
		7555M			±1	±2	
	Output Leakage Current					100	nA
Analog Input	INPUT Resistance (RI)			18	20	22	kΩ
	V_{REF} Input Resistance (R)			18	20	22	kΩ
	V_{REF} Voltage Range			−10		+10	V
I01 (Sum)	I01 Voltage Compliance (Note 4)					±1.0	mV
	I01 Output Capacitance	C_{101}	DB0-DB11 = "1"		200		pF
		C_{102}	DB0-DB11 = "1"		150		pF
		C_{101}	DB0-DB11 = "0"		125		pF
		C_{102}	DB0-DB11 = "0"		70		pF
Digital Inputs	Digital Input Voltage	V_{IL}	V_{CC} = +5V			+0.8	V
		V_{IH}	V_{CC} = +5V	+3.0			V
		V_{IL}	V_{CC} = +15V			+2.5	V
		V_{IH}	V_{CC} = +15V	+12.5			V
	Clock Input Voltage (Note 5)	V_{IL}	V_{DD} = +15V			+2.5	V
		V_{IH}	V_{DD} = +15V	+12.5			V
	I_{IL} and I_{IH}		0 ≤ V_{IN} ≤ V_{CC}			1.0	μA
	C_{IN}				2		pF
Digital Outputs	Digital Output Voltage	V_{OL}	V_{CC} = +5V, 1 TTL Load			+0.8	V
		V_{OH}	V_{CC} = +5V, 1 TTL Load	+3.0			V
		V_{OL}	V_{CC} = +15V, I_{SINK} = −3.0 mA			+1.5	V
		V_{OH}	V_{CC} = +15V, I_{SOURCE} = +1.0 mA	+13.5			V
	$I_{LEAKAGE}$ (Floating)				5		nA
	C_{OUT} (Floating)				5		pF
Timing	Conversion Time (Per Fig. 18)				100	200	μs
	LBI, HBI, EOC Propagation Delay	t_{ON}	Logic Level = 0 to +3V		300	500	ns
		t_{OFF}	Data Bit Load = 5kΩ, 15 pF		300	500	ns
	START Pulse Width			750		(Note 6)	ns
Power Supply	I_{DD}		+5V ≤ V_{DD} ≤ +15V		1.0	2.0	mA
	I_{CC}		+5V ≤ V_{CC} ≤ V_{DD}		0.1	2.0	mA
	Supply Rejection (V_{CC}, V_{DD})				±.001	±0.002	%FSR/%V
	Power Consumption				20	40	mW
Temp	Specification Temperature Range	7555C		0		+70	°C
		7555M		−55		+125	°C

Notes (7555)

1. Unless otherwise specified, performance guarantees apply for V_{DD} = +15V, V_{CC} = +5V, V_{REF} = +10,000V, and over the operating temperature ranges of 0°C to +70°C for 7555C and −55°C to +125°C for 7555M. Units typically meet performance specifications for +12V ≤ V_{DD} ≤ +15V and +5V ≤ V_{CC} ≤ V_{DD}.
2. Internally adjustable to zero.
3. The input gain determining resistor RI has been laser pretrimmed to establish the proper gain ratio against the ladder resistance R. RI is also compensated for the ladder switch characteristics by a series FET.
4. The linearity specifications are based on using an external comparator with less than ± 1 mV offset.
5. The internal clock circuitry operates from V_{DD} which is normally tied to the analog supplies. See applications section Digital Input/Output Logic Levels.
6. See application sections on START Timing.

Package Construction

Series 7555 and 7556 A-to-D converters utilize thick film conductors fired to an alumina substrate. Interconnections between these conductors, the thin film resistor network and the CMOS and bipolar semiconductor devices are made by thermal compression gold wire bonding. The ceramic cover (metal cover for Mil. models) is then sealed to the substrate using a polymer seal for commercial models and a hermetic seal for military versions. The lead frame is reflow soldered to terminal pads on both sides of the substrate to complete the rugged cost effective package.

Power Supply Considerations

Every operating configuration should include 1.0 μF decoupling capacitors on all power supplies to avoid introducing noise into each bit decision. The decoupling capacitors should be placed as close to the supply pins as possible. If electrolytic capacitors are used, they should be paralleled by 0.01 μF ceramic capacitors to obtain better high frequency performance.

Separate digital and analog ground returns designated DGND and AGND, respectively, are provided so that noisy ground currents normally associated with digital circuits can be separately returned to the system power supply ground. Both AGND and DGND must be connected to a common ground potential within the system. The converter will perform within specification with up to ±0.5V between the two grounds.

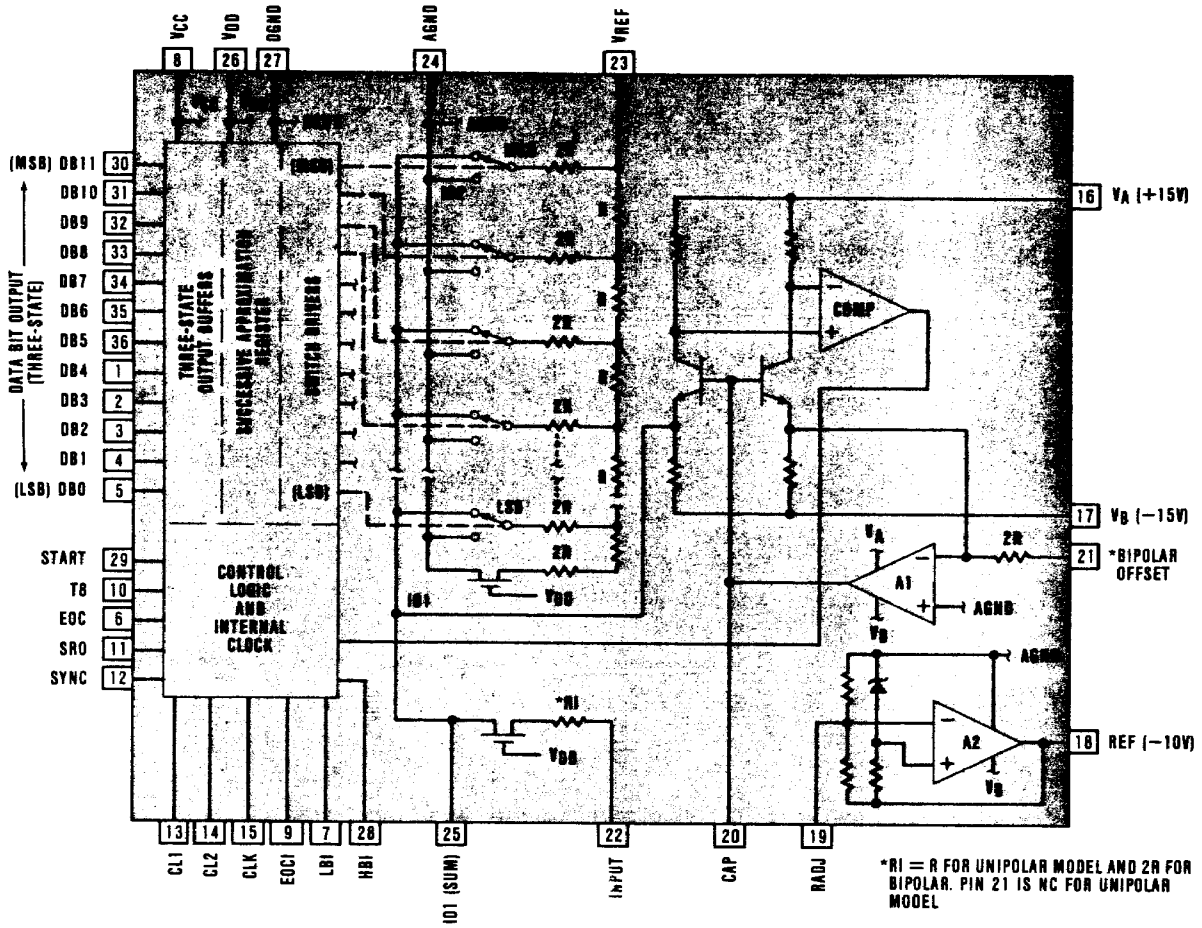


Figure 3. Series 7556 Block Diagram

Series 7556 Operation

Series 7556 includes all of the logic circuitry and flexibility of the 7555 plus a precision reference, fast comparator, and is available in both bipolar and unipolar models. The bipolar version input resistor RI is 2R (instead of R for unipolar) to provide the correct scale factor. In addition, zero offsets and gain adjustments are functional trimmed to achieve the performance guarantees shown in Table II.

Series 7556 Precision Internal Reference

The internal voltage reference is trimmed to −10V ±10 mV and may be adjusted over a range of ±0.5V without degrading tempco. The −10V reference level provides analog input ranges of 0 to +10V for the unipolar versions and −10V to +10V for the bipolar versions.

The internal reference may be externally connected to the V_{REF} input, or other references may be used if desired.

The internal reference can supply up to 5 mA to other converters or other system requirements without degrading its performance.

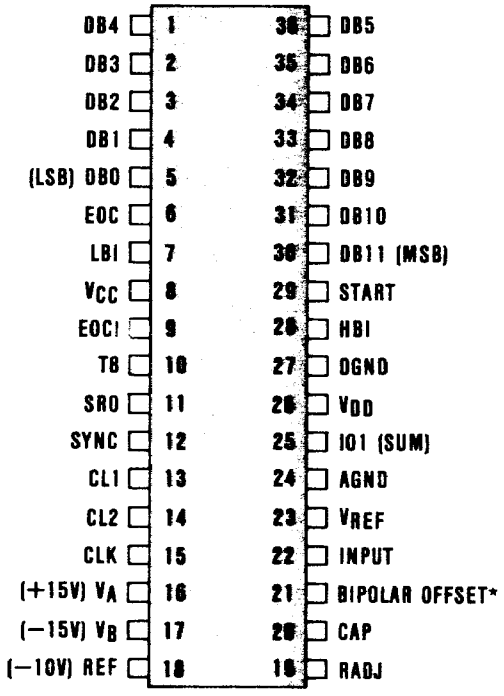


Figure 4. Series 7556 Pin Assignments

Table II—Series 7556 Performance Specifications (Note 1)

	Parameter		Conditions	Minimum	Typical	Maximum	Units
Accuracy	Resolution					12	Bits
	Linearity		$T_C = +25°C$		±¼	±½	LSB
	Linearity	7556 CU, CB	$0°C \le T_C \le +70°C$		±½	±1	LSB
		7556 MU, MB	$-55°C \le T_C \le +125°C$		±½	±1	LSB
	Differential Linearity		Over Spec Temp Range		±½		LSB
	No Missing Codes		Over Spec Temp Range		Guaranteed		—
	Input Gain Setting		$T_C = +25°C$		±0.07	±0.2	%FSR
	Input Gain Tempco (Note 2)	CU, CB	$0°C \le T_C \le +70°C$		±10	±30	p/10⁶FSR/°C
		MU, MB	$-55°C \le T_C \le +125°C$		±10	±25	p/10⁶FSR/°C
	Unipolar Zero Offset (Note 3)	CU	$T_C = +25°C$		±0.05	±0.1	%FSR
		MU	$T_C = +25°C$		±0.03	±0.05	%FSR
	Bipolar Zero Offset (Note 3)	CB	$T_C = +25°C$		±0.1	±0.15	%FSR
		MB	$T_C = +25°C$		±0.05	±0.1	%FSR
	Unipolar Offset Tempco	CU	$0°C \le T_C \le +70°C$		±3	±10	p/10⁶FSR/°C
		MU	$-55°C \le T_C \le +125°C$		±3	±10	p/10⁶FSR/°C
	Bipolar Offset Tempco	CB	$0°C \le T_C \le +70°C$		±10	±20	p/10⁶FSR/°C
		MB	$-55°C \le T_C \le +125°C$		±7	±15	p/10⁶FSR/°C
Analog Inputs	Input Resistance	CU, MU		13.5	15	16.5	kΩ
		CB, MB		27	30	33	kΩ
	Input Voltage Range	CU, MU	With Internal −10 V Ref.		0 to +10		V
		CB, MB	With Internal −10 V Ref.		−10 to +10		V
	Reference Input Resistance			13.5	15	16.5	kΩ
Reference	Reference Output Voltage		$T_C = +25°C$	−9.990	−10.000	−10.010	V
	Output Load Current					−5	mA
	Reference Output Voltage Tempco	CU, CB	$0°C \le T_C \le +70°C$		±15	(Note 4)	p/10⁶/°C
		MU, MB	$-55°C \le T_C \le +125°C$		±10	(Note 4)	p/10⁶/°C
Digital Inputs	Digital Input Voltage	V_{IL}	$V_{CC} = +5V$			+0.8	V
		V_{IH}	$V_{CC} = +5V$	+3.0			V
		V_{IL}	$V_{CC} = +15V$			+2.5	V
		V_{IH}	$V_{CC} = +15V$	+12.5			V
	Clock Input Voltage (Note 5)	V_{IL}	$V_{DD} = +15V$			+2.5	V
		V_{IH}	$V_{DD} = +15V$	+12.5			V
	I_{IL} and I_{IH}		$0 \le V_{IN} \le V_{CC}$			1.0	μA
	C_{IN}				2		pF
Digital Outputs	Digital Output Voltage	V_{OL}	$V_{CC} = +5V$, 1 TTL Load			+0.8	V
		V_{OH}	$V_{CC} = +5V$, 1 TTL Load	+3.0			V
		V_{OL}	$V_{CC} = +15V$, $I_{SINK} = -3.0$ mA			+1.5	V
		V_{OH}	$V_{CC} = +15V$, $I_{SOURCE} = +1.0$ mA	+13.5			V
	$I_{LEAKAGE}$ (Floating)				5		nA
	C_{OUT} (Floating)				5		pF
Timing	Conversion Time				40	50	μs
	LBI, HBI, EOC Propogation Delay	t_{ON}	Logic Level = 0 to +3V		300	500	ns
		t_{OFF}	Data Bit Load = 5kΩ, 15pF		300	500	ns
	START Pulse Width			750		(Note 6)	ns
Power Supply	I_{DD}		$V_{DD} = +15V$		1.0	2	mA
	I_{CC}		$V_{CC} = +5V$		0.7	2	mA
	I_A		$V_A = +15V$		6.0	10.0	mA
	I_B		$V_B = -15V$		5.0	8.0	mA
	Power Supply Rejection	V_{CC}, V_{DD}	$V_{CC} = +5V$, $V_{DD} = +15V$		±0.001	±0.002	%FSR/%V
		V_A, V_B	$V_A = +15V$, $V_B = -15V$		±0.002	±0.004	%FSR/%V
Temp.	Power Consumption				200	300	mW
	Specification Temp Range	CU, CB		0		+70	°C
		MU, MB		−55		+125	°C
	Storage Temp Range			−65		+125	°C

Notes (7556)

1. Unless otherwise specified, performance guarantees apply for $V_{DD} = +15V$, $V_{CC} = +5V$, $V_A = +15V$, $V_B = -15V$, $V_{REF} = -10.000V$ (pin 18 is connected to pin 23 for unipolar operation and also pin 21 for bipolar operation), and over the operating temperature range of 0°C to +70°C for 7555 CU or CB, and over −55°C to +125°C for 7556 MU or MB. Units typically meet performance specifications for $+12V \le V_{DD} \le +15V$ and $+5V \le V_{CC} \le V_{DD}$.
2. The input gain determining resistor RI has been laser pre-trimmed to establish the proper gain ratio against the ladder resistance R. RI is also compensated for the ladder switch characteristics by a series FET. The specification shown is based on using the internal reference and includes reference tempco.
3. Externally adjustable to zero.
4. Maximum reference tempco is included in guarantee for maximum Input Gain Tempco.
5. The internal clock circuitry operates from V_{DD} which is normally tied to the analog supplies. See applications section Digital Input/Output Logic Levels.
6. See application sections on START Timing.

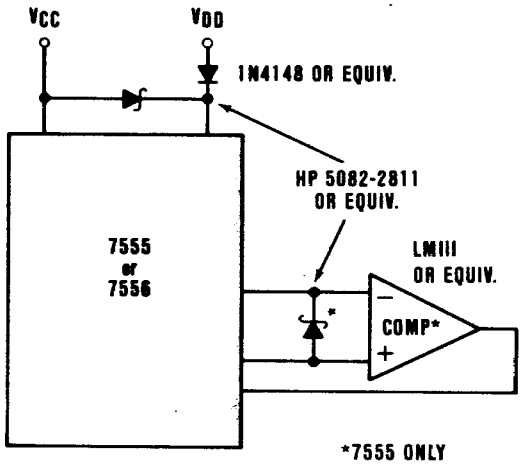


Figure 5. Diode Protection

Diode Protection

Since V_{CC} should never exceed V_{DD} by more than 0.4V, diode protection may be required if the power supply sequence is unknown or V_{CC} comes on prior to V_{DD}. Typical components and the suggested configuration are shown in Figure 5.

Digital Inputs and Outputs

The digital inputs and outputs of the 7555 and 7556 are functionally described as follows:

DB0-DB11 — Data Bit outputs are all three-state to allow direct data bus drive. DB0 is the LSB, DB11 is the MSB. Each can drive one TTL gate load or four 54LS/74LS TTL gate loads.

LBI — Low Byte Inhibit provides three-state control for the eight LSB's (DB0-DB7). Logic "0" causes the eight LSB's to float, and logic "1" allows the eight LSB's to drive the data bus.

HBI — High Byte Inhibit functions the same as LBI but for the four MSB's (DB8-DB11).

START — Logic "1" on the START input initiates conversion as long as START returns to logic "0" prior to the rise of the succeeding clock. START may be initiated by an external command for single conversions or by EOC (see below) for continuous conversion applications.

EOC — End Of Conversion is a logic "1" output simultaneous with the output of the LSB decision signifying that the conversion sequence is complete. EOC can be used to restart the conversion sequence and/or indicate that the entire 12-bit word is available at the parallel Data Bit outputs.

EOCI — End Of Conversion Inhibit operates the same as LBI and HBI and can be used where EOC lines of multiple converters are bused and one converter at a time is allowed to output EOC.

SRO — Serial Register Output provides each data bit decision as it is made throughout the conversion sequence (positive true). SRO is a three-state output that is automatically enabled at the start of the conversion sequence. SRO returns to the floating state one clock after the rise of the EOC unless continuous conversion is in progress.

SYNC — The SYNC output provides a series of rising edges to be used for the output transfer of stable SRO data. SYNC is a three-state output automatically enabled at the start of the conversion sequence and returning to the floating state one clock period after the rise of EOC.

T8 — T8 allows the user to truncate the conversion sequence after 8 bits for more efficient intermixing of 8-bit and 12-bit conversions where required. All other functions (START, LBI, etc.) are unaffected. Logic "0" truncates the conversion after 8 bits. Logic "1" allows conversion to proceed through 12 bits. EOC rises simultaneous with the decision of the LSB of the 8-bit word.

CLK — The clock input, CLK, is either driven by the system clock or connected to CL1 and CL2 through the RC network in Figure 9 for internal clocking (see Clocking Configurations section).

COMP — The external comparator output is fed back to the control logic at COMP (7555 only).

Digital Output Coding

The digital output words corresponding to various analog inputs are shown for unipolar and bipolar operation in Tables III and IV. The Full Scale (FS) magnitude is equal to the reference voltage but opposite polarity.

Table III. Unipolar Operation (Binary)

Analog Input	Digital Output Code MSB LSB
FS-LSB	1 1 1 1 1 1 1 1 1 1 1 1
FS-2LSB	1 1 1 1 1 1 1 1 1 1 1 0
¾ FS	1 1 0 0 0 0 0 0 0 0 0 0
½ FS + 1LSB	1 0 0 0 0 0 0 0 0 0 0 1
½ FS	1 0 0 0 0 0 0 0 0 0 0 0
½ FS-1LSB	0 1 1 1 1 1 1 1 1 1 1 1
¼ FS	0 1 0 0 0 0 0 0 0 0 0 0
1 LSB	0 0 0 0 0 0 0 0 0 0 0 1
0	0 0 0 0 0 0 0 0 0 0 0 0

Table IV Bipolar Operation (Offset Binary)

Analog Input	Digital Output Code MSB LSB
+(FS-1LSB)	1 1 1 1 1 1 1 1 1 1 1 1
+(FS-2LSB)	1 1 1 1 1 1 1 1 1 1 1 0
+(½ FS)	1 1 0 0 0 0 0 0 0 0 0 0
+(1LSB)	1 0 0 0 0 0 0 0 0 0 0 1
0	1 0 0 0 0 0 0 0 0 0 0 0
−(1LSB)	0 1 1 1 1 1 1 1 1 1 1 1
−(½ FS)	0 1 0 0 0 0 0 0 0 0 0 0
−(FS-1LSB)	0 0 0 0 0 0 0 0 0 0 0 1
−FS	0 0 0 0 0 0 0 0 0 0 0 0

Maximum Ratings (7555 and 7556)

V_{REF} to GND . . . . . ±25V
V_{DD} to GND . . . . . +17V
V_{CC} to GND . . . . . +17V
V_{CC} to V_{DD} . . . . . +0.4V
101 to GND; 102 to GND . . . . . −100mV to V_{DD}
Operating Temperature Range (C) . . . . . 0°C to +70°C
Operating Temperature Range (M) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +125°C
Digital Input Voltage Range . . . . . V_{DD} to GND

Operation Cautions

1. Do not apply voltages (from a source which can supply more than 5mA) lower than ground to 101 or 102 terminals. (See Figure 7)
2. Do not apply voltages higher than V_{DD} or less than GND to any other input/output terminal except V_{REF} or input.
3. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Store units in conductive foam.
4. V_{CC} should never exceed V_{DD} by more than 0.4V.

System Timing

The system timing for a single conversion sequence using the internal clock is shown in Figure 6. All data bit outputs are positive true. The internally generated clock is indirectly available by monitoring $\overline{CL}$ at CL1.

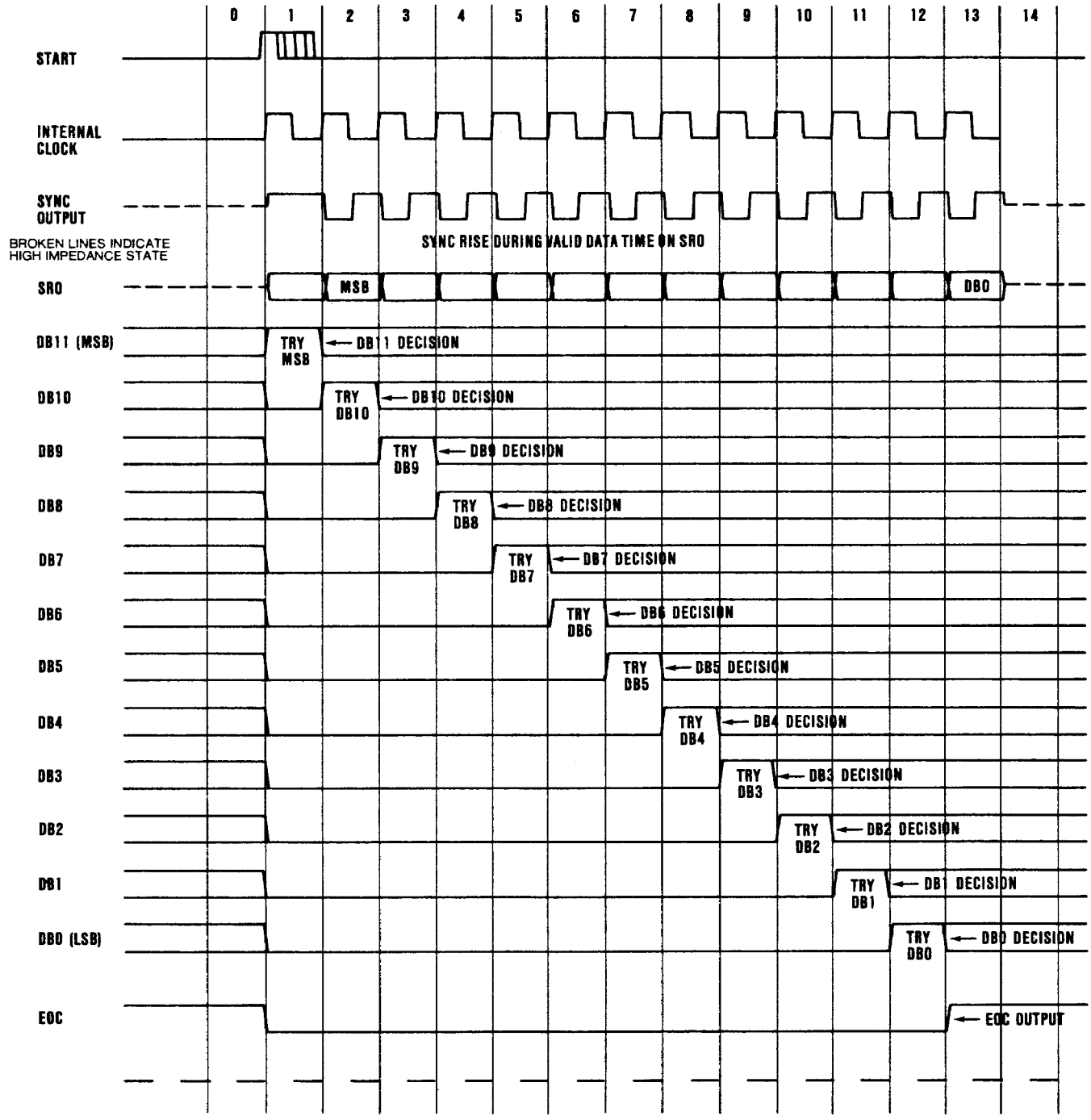


Figure 6. System Timing Diagram

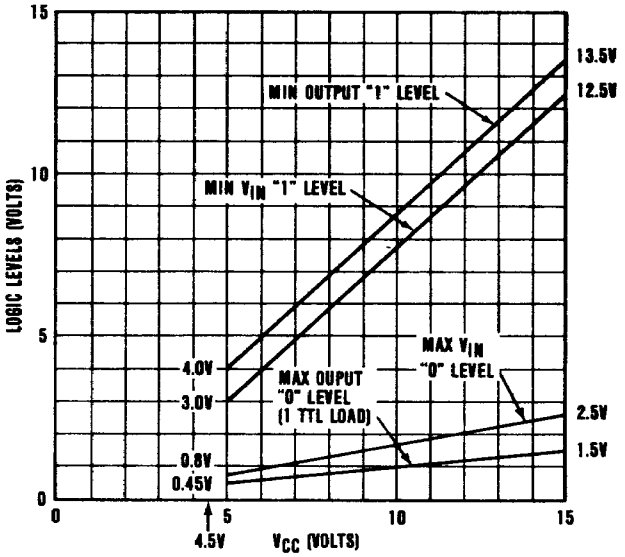


Figure 7. Input/Output Logic Levels

Digital Input/Output Logic Levels

The minimum and maximum voltage levels for digital inputs and outputs are shown in Figure 7. These logic levels provide compatibility with TTL for V_{CC} = +5V and CMOS for V_{CC} levels up to +15V.

Note: The system internal clock circuitry operates from the $+V_{DD}$ supply which is normally +12V to +15V. Although the converter functions properly with V_{DD} levels down to +5V, linearity specifications are guaranteed only for +12 to +15V. Consequently, TTL applications utilizing an external clock are typically configured as shown in Figure 8. V_A and V_B (7556) are designed for ±15V operation.

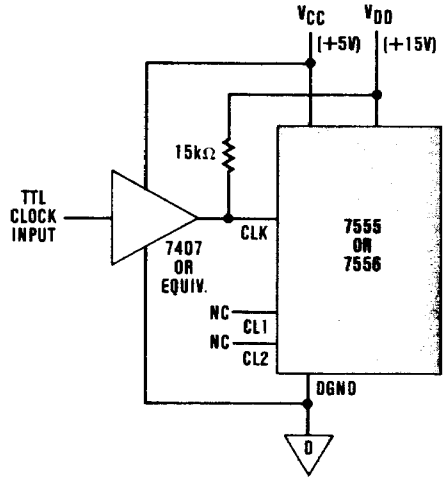


Figure 8. External TTL Clock Drive

Clocking Configurations

Both series 7555 and 7556 may be driven by the system clock or operated with an internally generated clock. The two alternatives are shown in Figure 9 below.

The typical clock frequency for various C1 values and two sets of R values are shown in Figure 10. Note that R1 should always equal ten times R2.

The approximate values may be calculated as follows:

$$f_{CLK} = \frac{0.45}{(R2)\,(C)}$$

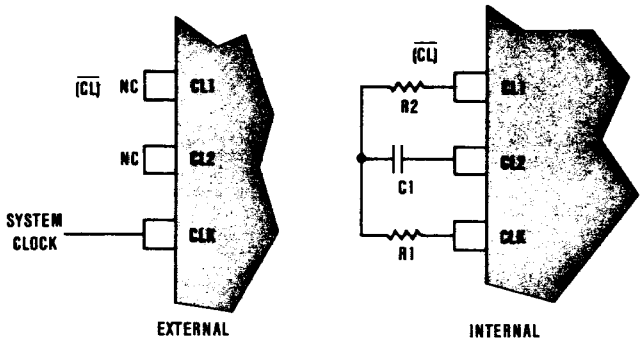


Figure 9. Clocking Configurations

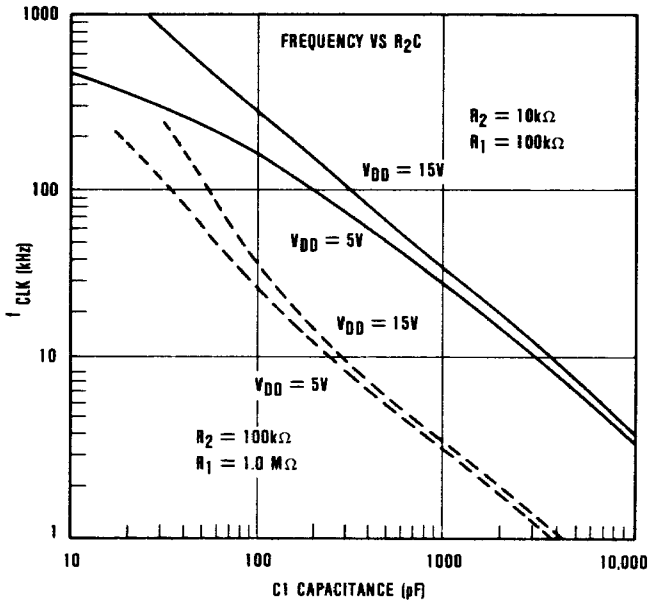


Figure 10. Clock Frequency Setting

START Timing—Internal Clock

START timing is very straight forward for the internal clock configuration since the rise of START initiates the internal clock which runs only during the conversion sequence. This timing relationship is shown in Figure 11 below.

In addition to starting the clock, the rise of the START pulse sets the MSB to "1" for the first bit trial, sets all other bits to "0", sets EOC to "0" and indirectly enables the three-state SYNC and SRO outputs.

The START pulse must remain high at least 750 ns and must return to "0" at least 200 ns prior to the rise of the next clock pulse to insure starting during the first clock period.

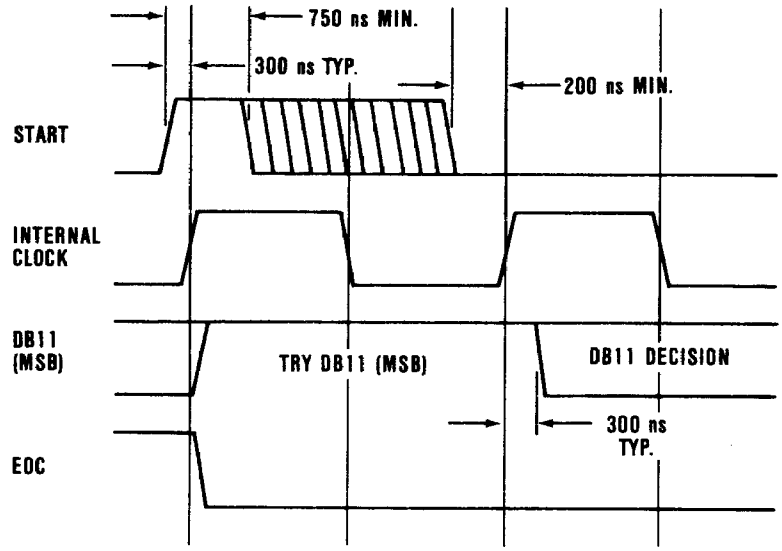


Figure 11. START Timing—Internal Clock

START Timing—External Clock

The START line must rise while the external clock is low to assure proper latching of the START command and resetting of internal flip-flops. The 200 ns boundaries at each end of the clock low state, shown in Figure 12, will insure proper control of the start timing. The fall of the START command follows the same guide lines as with the internal clock.

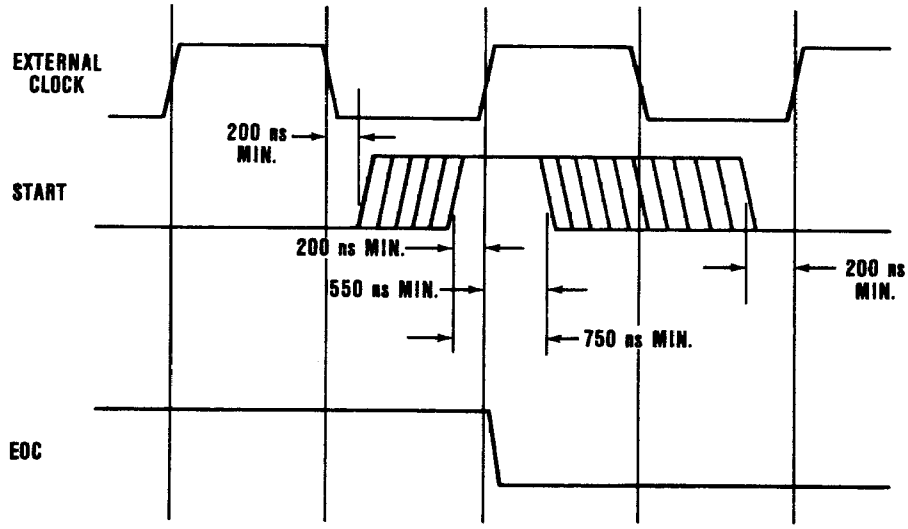


Figure 12. START Timing—External Clock

RUN/STOP Operation

Both Series 7555 and 7556 can be operated in a RUN/STOP mode using the internal clock in the configuration shown in Figure 13. Since EOC remains high at the end of conversion, raising RUN/STOP to logic "1" will start a new conversion sequence at its beginning simultaneously enabling the free running internal clock. Switching RUN/STOP to logic "0" (after the 750 ns minimum START time of Figure 11) will cause the converter to complete the initiated conversion sequence and then wait for a new RUN command.

RUN/STOP operation with an external clock must comply with the START timing requirements of Figure 12. Since EOC must be "1" for a START to occur, RUN/STOP cannot interrupt the conversion sequence.

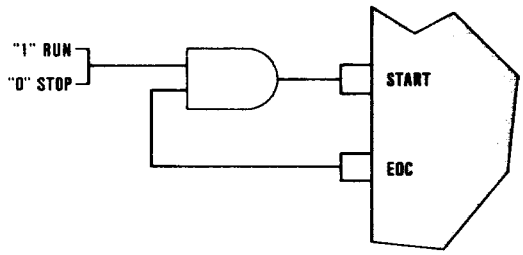


Figure 13. RUN/STOP Operation

Continuous Conversion—EOC/START

EOC can be connected to START to continuously initiate new conversion cycles. START will initiate a new conversion sequence beginning with the MSB trial one clock period after the rise of EOC and outputting the MSB decision two clock periods after the rise of EOC (13 clock periods per 12-bit conversion).

Priority Re-START Operation

Forcing START to logic "1" in the middle of a conversion sequence will interrupt the conversion in progress at the next rise of $\overline{CL}$. Returning START to logic "0" per Figures 11 or 12 will allow a new conversion sequence to be initiated. Holding START at logic "1" for successive clock periods will simply cause the internal flip-flops to continuously reset for the MSB trial until START is returned to logic "0" with the proper timing.

12-Bit Parallel Output

Figure 14 shows the basic connections for 12-bit parallel output with LBI and HBI tied together to simultaneously enable or inhibit the twelve three-state data bit outputs. T8 is tied to logic "1" to allow the successive approximation sequence to proceed through 12 bits. The propogation delay from the time LBI or HBI rise to logic "1" until each three-state data bit output is driving the data line is typically 300 ns. The parallel word is available after the rise of EOC and will remain stable until a new START is initiated.

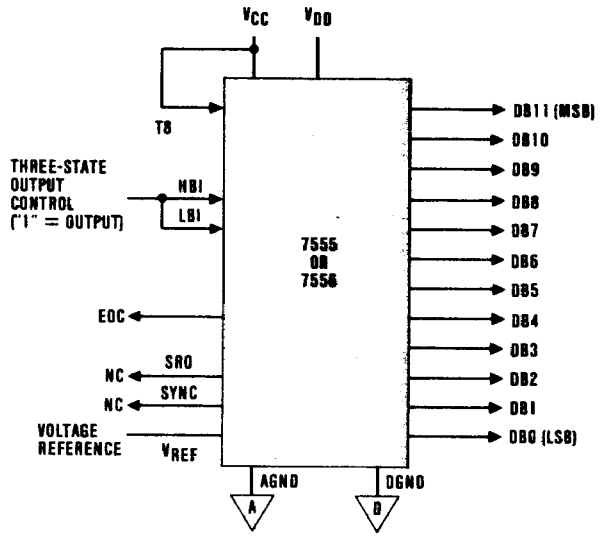


Figure 14. 12-Bit Parallel Output

12-Bit Output To An 8-Bit Data Bus

Figure 15 shows the basic connections for separately transferring the four MSB's and eight LSB's to an 8-bit microprocessor data bus using the HBI and LBI control inputs (after the rise of EOC).

The four MSB data bits are shown arbitrarily connected to D0-D3 to create the word format shown in Figure 16. Other data handling or software preferences may require their connection to other data bus lines. The format shown is one of the most efficient arrangements for the 8080/8085 microprocessor family because both 8-bit words can be loaded into adjacent register locations utilizing the single program instruction LHLD.

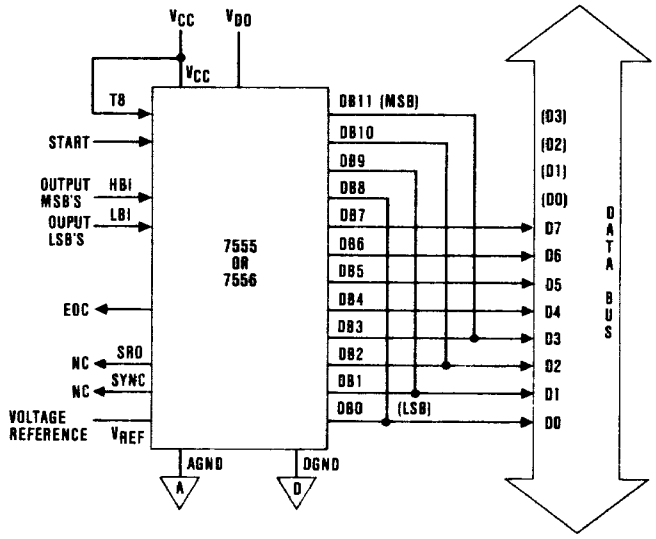


Figure 15. 12-Bit Output to 8-Bit Data Bus

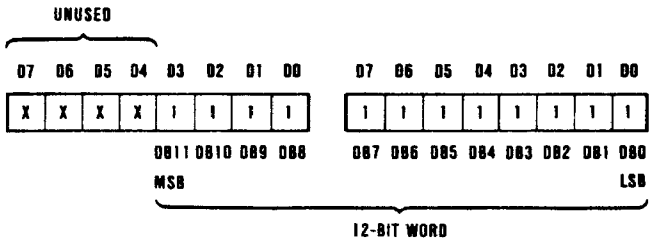


Figure 16. 12-Bit Data Format

Serial Data Output

The basic connections for serial data output are shown in Figure 17. Using the rising edge of SYNC pulse (external or internal clock) assures that output data is stable at the time of transfer.

The 100kΩ resistor shown assures that the SYNC line will be pulled up to logic "1" to avoid the further transfer of data after the LSB data output period since SYNC is a three-state output.

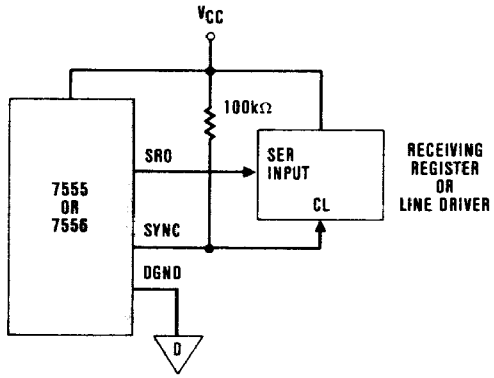


Figure 17. Serial Data Transfer

Unipolar Operation (7555)

The basic analog connections for unipolar operation of Series 7555 are shown in Figure 18. Gain and offset adjustment provisions are shown with the most basic external comparator configuration, including an output pull-up resistor and input clamping diodes.

This configuration uses a −10V external reference to provide an input voltage range of 0V (000000000000) to +10V −1 LSB (111111111111).

Input Polarity Reversal and Ratiometric Operation (7555)

The input voltage range may be modified to provide 0V (000000000000) to −10V (111111111111) by using a +10V reference and reversing the polarity of the comparator inputs (IO1 to − and IO2 to +). In addition, any reference (and input) level between −10V and +10V may be used.

Bipolar Operation (7555)

The modifications for bipolar operation are shown in Figure 21. The offset adjustment is more easily implemented at the input summing amplifier.

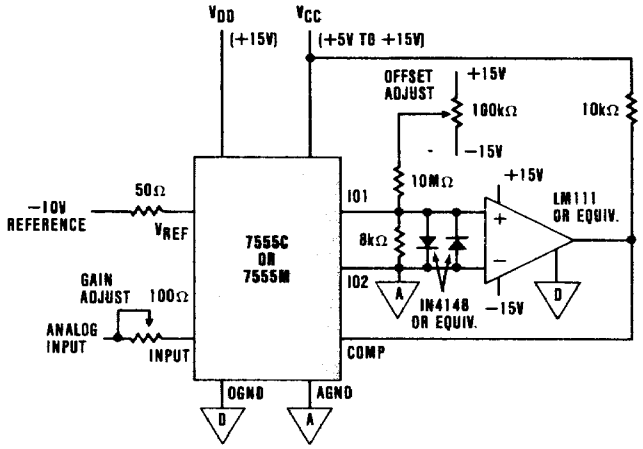


Figure 18. Unipolar Operation (7555)

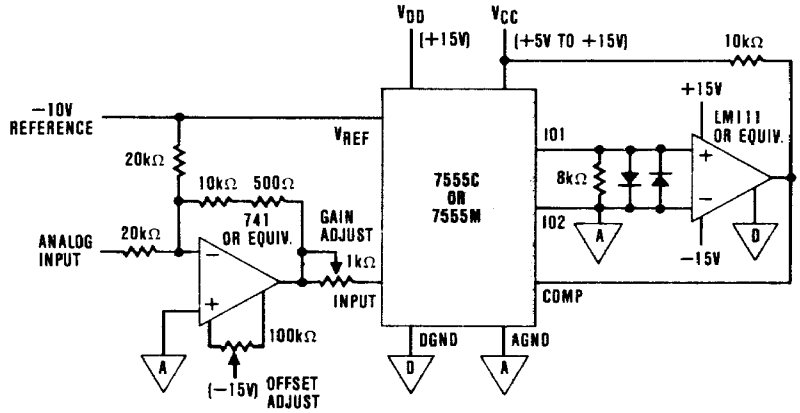


Figure 19. Bipolar Operation (7555)

High Speed Comparator

The comparator circuitry can be modified to increase conversion speed typically by a factor of four. This circuitry is shown in Figure 20 with suggested component values to achieve 12-bit performance. The value of C depends on the board layout stray capacitance. C rolls off the current comparator thereby making it less susceptible to digital "noise" created by the comparator's output transitions. The best board layout design would allow C to approach zero. Therefore, the most practical objective should be to make C as small as possible. C values higher than 10 pF begin to compromise the speed advantage of adding the current comparator.

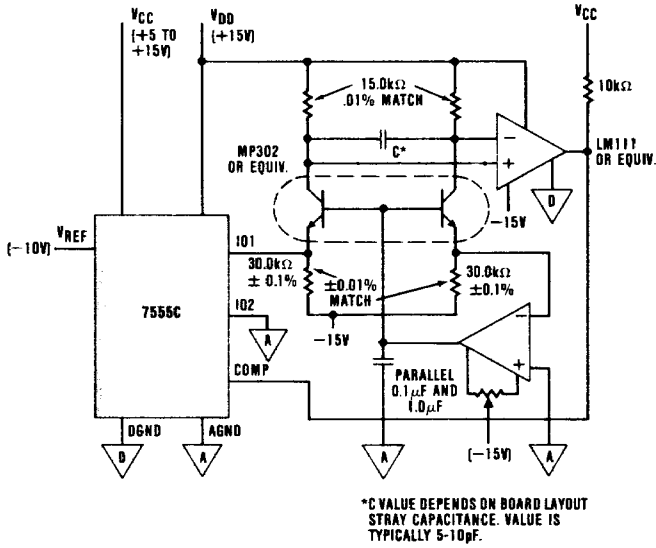


Figure 20. High Speed Unipolar Configuration (7555)

Unipolar Operation (7556)

The basic connections for unipolar operation of Series 7556 are shown in Figure 21. Gain and zero offset adjustment are shown but are optional additions because the 7556 is laser functional trimmed to the tolerances shown in Table II.

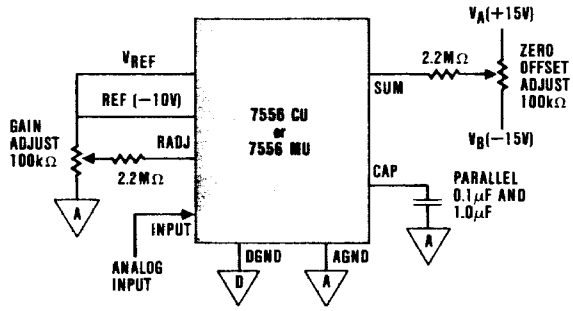


Figure 21. Unipolar Operation (7556) With Optional Gain and Offset Adjustments

External Reference Applications (7556)

Although 7556 has a precision internal reference, the converter's reference input (V_{REF}) is not internally tied and can accept other reference inputs. The gain adjust circuitry shown in Figure 18 may be used for Series 7556 in external reference applications.

Bipolar Operation (7556)

The bipolar configuration for 7556 is the same as unipolar operation shown in Figure 21 with the addition that BIPOLAR OFFSET (pin 21) is connected directly to the voltage reference (external or internal).

8080 CPU Interface

A typical interface configuration for the 8080 basic chip set is shown in Figure 22. A typical subroutine for initiating an A-to-D conversion sequence and inputting the resulting data is shown in Figure 23. For simplicity this example assumes that the single A-to-D converter is memory mapped and occupies the entire 8000H section of memory (location 32768 through 65535). Address line A15 (8XXXH) serves the function of chip select and other specific blocks of memory perform other command functions (e.g., 8XX8H is used for START).

In this example the microprocessor and ADC operate at independent clock frequencies and, therefore, the microprocessor utilizes a test loop to wait until EOC indicates that conversion is complete and that valid data can be made available on the system data bus.

Many alternative forms of address decoding are easily implemented to allow the selection of multiple ADC's or to more conservatively allocate portions of the memory map for memory and/or other peripherals. For example, a four to sixteen line decoder chip could much more efficiently select converters and/or other peripherals by decoding A12 through A15 into sixteen individual chip select outputs.

The subroutine shown returns to the calling program leaving the ADC output data word in the microprocessor's H and L registers. This is convenient for temporary storage while other program steps are performed and leaves the data very accessible as an operand for subsequent program steps.

WAIT State May Be Required

Systems operating with $\overline{MEMR}$ pulse widths less than 500 ns may require one or more "WAIT" states to ensure adequate pulse widths for START and other ADC commands.

```
START   EQU 8008H       ;Address of START command
EOCI    EQU 8004H       ;Address of EOCI
LBIA    EQU 8001H       ;Address of LBI
ADIN:   LXI H,START     ;Point H and L to START
        MOV A,M         ;Start ADC conversion
        LXI H,EOCI      ;Point H and L to EOC
LOOP:   MOV A,M         ;Check EOC
        ANI 01H         ;Test for EOC = "1"
        JZ LOOP         ;Re-test for EOC = "1"
        LHLD LBIA       ;Load H and L with ADC data
        RET             ;Return to calling program
```

Figure 23. 8080 ADC Input Subroutine.

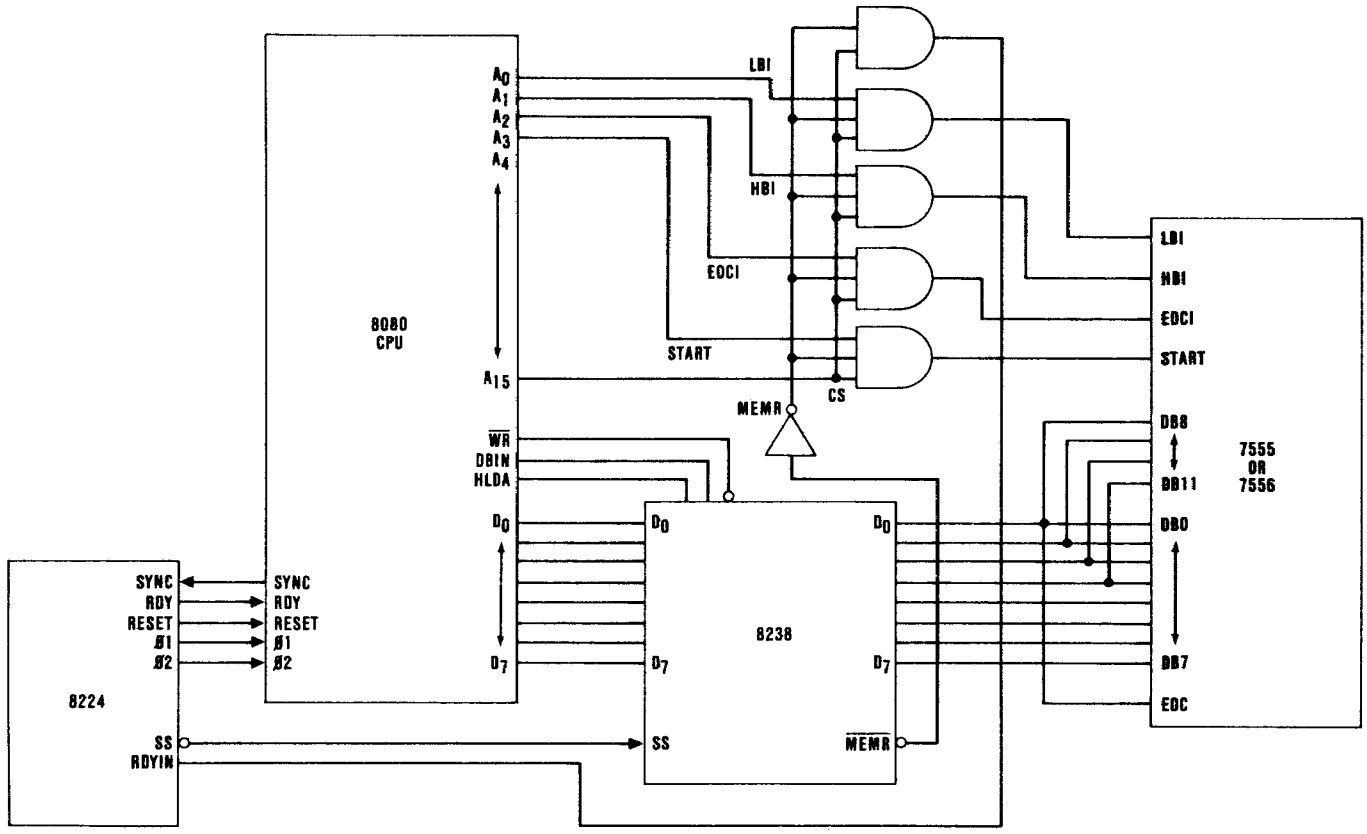
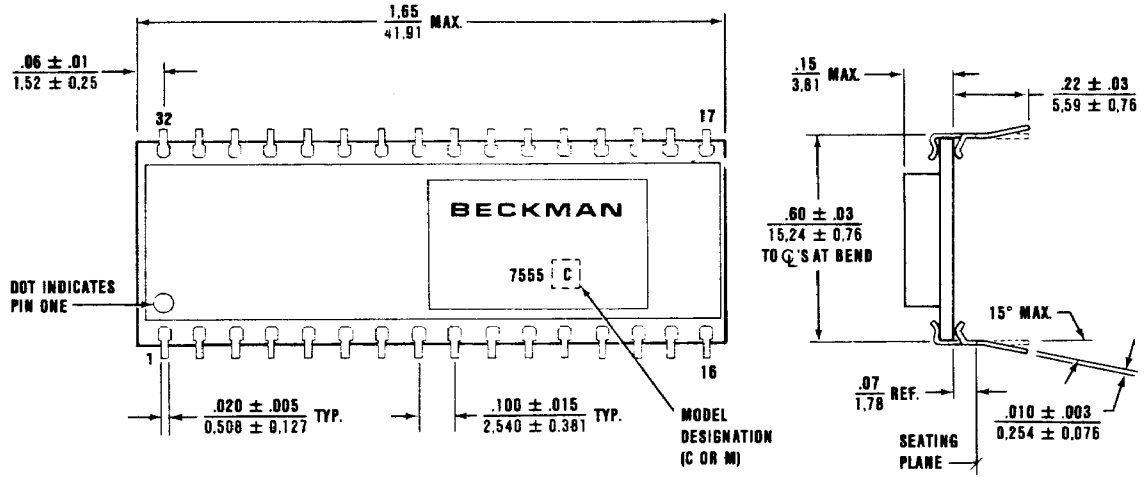
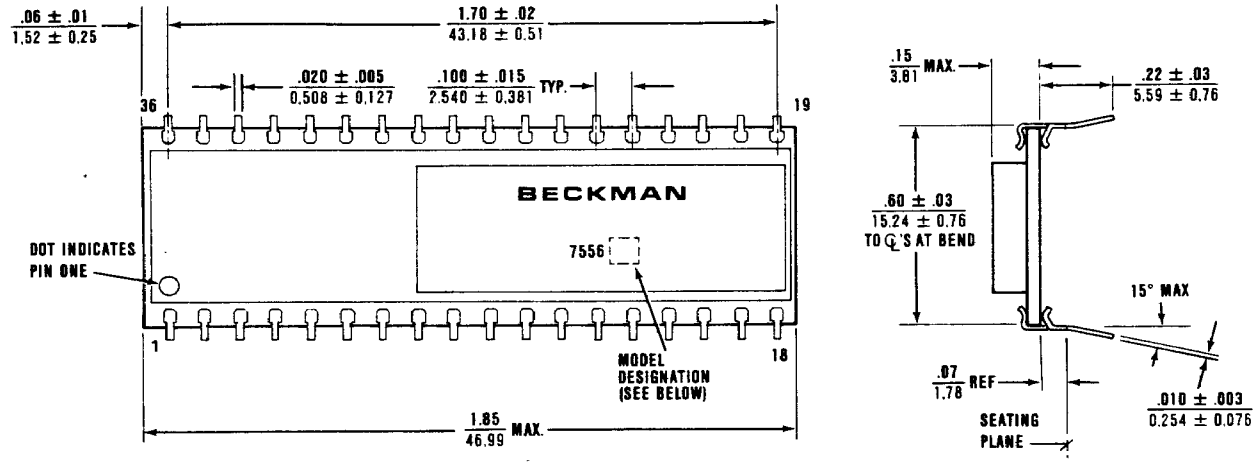


Figure 22. CPU Interface Configuration

Outline Drawing—Series 7555



Outline Drawing—Series 7556



Ordering Information

7556 C B
- B — 7556 only; Unipolar = U and Bipolar = B
- C — Commercial or Mil Temp Range
- 7556 — Basic Series—7555 or 7556

DIMENSIONS: INCH (mm) — THIRD ANGLE PROJECTION

Tolerances unless otherwise specified ± .005 inch and ± 0.127 mm angular ±2°

Metric equivalents, based upon 1 inch = 25.4 mm are rounded to the same number of decimal places as in the original English units and are provided for general information only.

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