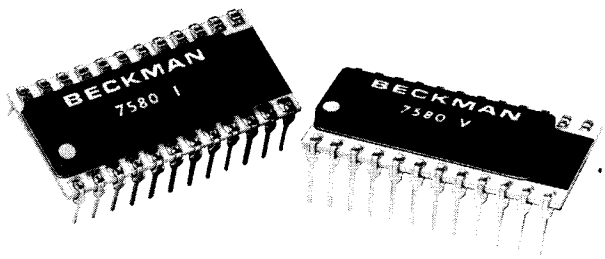
Series 7580
CMOS, 12-Bit General Purpose D/A Converters



Beckman Models 7580V and 7580I are the first 12-bit CMOS digital-to-analog converters to combine the low power advantages of CMOS with the completeness and versatility of the popular DAC80. The 7580V includes the output buffer amplifier or multiple output voltage ranges, and the 7280I provides current output, also with multiple output ranges selected by external connections.

Models 7580V voltage output and 7580I current output use a proprietary CMOS switch design, combined with a thin film R-2R ladder network to achieve very low total power dissipation, typically 150 mW. Also, each model can operate from ±12V to ±17V supplies and neither requires +5V, thereby achieving complete noise isolation from the logic supply.

Both models include an internal reference and both can be driven from either TTL or CMOS logic. Their outstanding features include:

- Low cost for a complete converter
- Pin-for-pin replacement for DAC80
- Low power CMOS switching—150 mW
- One model for ±12V to ±17V supplies
- ±0.012%(±½LSB) linearity guaranteed over 0°C to +70°C
- Monotonicity guaranteed over 0°C to +70°C
- No +5V supply required
- ±0.002%FSR/%V supply rejection for both supplies
- ±0.002% pretrimmed zero offset (max.)
- Four-quadrant multiplying capability

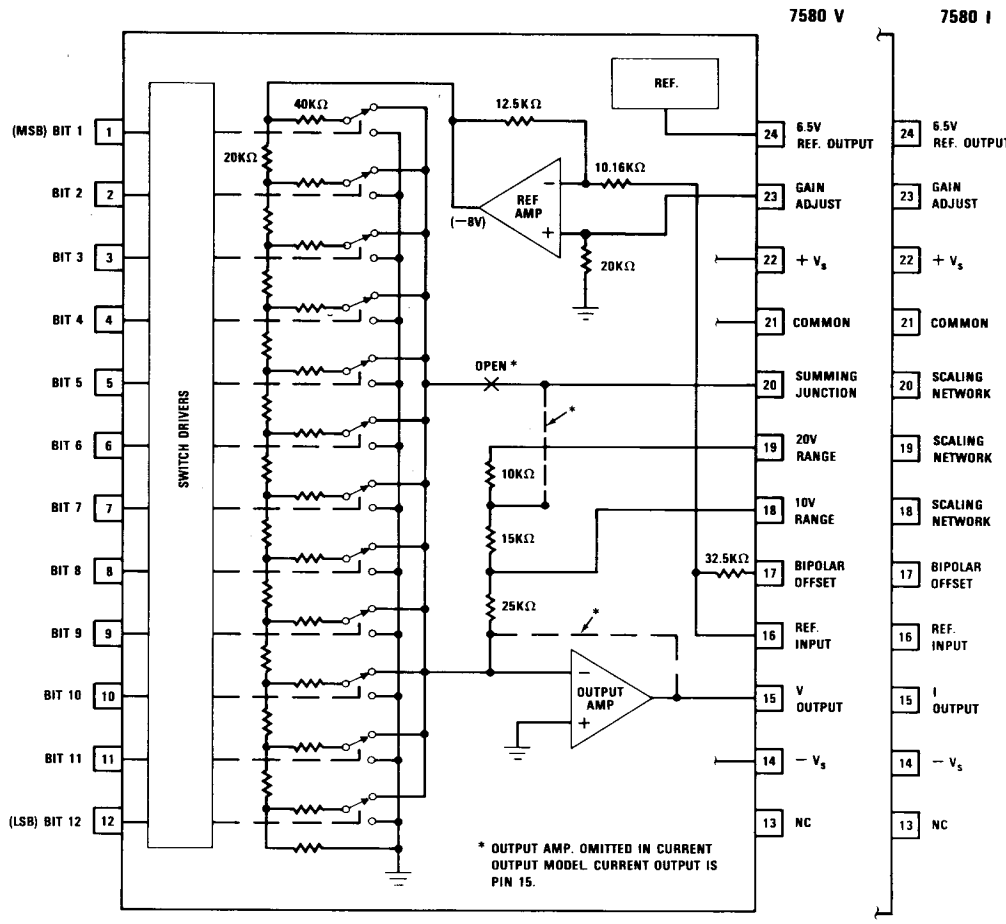


Figure 1. Series 7580 Block Diagram

Operation

The 7580 uses an "inverted R-2R" thin film ladder network and precisely matched CMOS switches to switch the 2R leg currents of the ladder network into COMMON or the output amplifier summing node (or current output terminal). Matched thin film feedback resistors are included to allow the selection of multiple output voltage (current) ranges while maintaining precise gain temperature tracking to the R of the ladder network.

The internal reference similarly uses matched thin film resistors to achieve excellent performance over the specified operating temperature range. Both gain and offset are actively laser trimmed to achieve more precise initial settings than previous DAC80 versions.

Accuracy

Series 7580 really offers true 12-bit performance.

- ±½ LSB (0.012%) linearity guaranteed over 0°C to 70°C
- ±½ LSB differential linearity guaranteed over 0°C to +70°C
- Monotonicity guaranteed over 0°C to +70°C

The ±½ LSB linearity spec guarantees that each step in the output voltage "staircase" will be no further than ±½ LSB maximum from an ideal straightline between the output range end points (inputs all "1's" and inputs all "0's"). This specification also guarantees monotonic output (an increase in digital input code will always cause an increase in analog output). The differential linearity spec guarantees that each output staircase step will be 1 LSB ±½ LSB, i.e., each step will not be smaller than ½ LSB nor larger than 1½ LSB.

Table 1—Performance Specifications (Note 1)

	Parameter		Condition	7580V			7580I			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Digital Input	Resolution					12			12	bits
	Input Voltage	Logic "1"	Complementary Binary Input	+2.4		$+V_S$	+2.4		$+V_S$	V
		Logic "0"	Complementary Binary Input	−0.3		+0.8	−0.3		+0.8	V
	Input Current		"0" or "1"		1			1		μA
Accuracy	Linearity		0°C to +70°C		±¼	±½		±¼	±½	LSB
	Differential Linearity		0°C to +70°C		±¼	±½		±¼	±½	LSB
	Gain Error		(adjustable to zero)		±0.05	±0.2		±0.05	±0.2	% FSR
	Offset Error		(adjustable to zero)		±0.005	±0.02		±0.005	±0.02	% FSR
	Monotonicity Temp. Range		(guaranteed minimum)	0		+70	0		+70	°C
	Offset Drift Unipolar		0°C to +70°C		±1	±2		±1	±2	p/10^6 FSR/°C
	Offset Drift Bipolar		0°C to +70°C		±10	±15		±10	±15	p/10^6 FSR/°C
	Gain Drift (incl. ref.)		0°C to +70°C			±30			±30	p/10^6 FSR/°C
	Gain Drift (not incl. ref.)		0°C to +70°C		±5			±5		p/10^6 FSR/°C
	Reference Voltage				+6.5			+6.5		V
	Reference Current					+200			+200	μA
	Reference Tempco				±20			±20		p/10^6 FSR/°C
Speed	Settling Time (Note)		FSR Settling to 0.01% 50KΩ Feedback		50			6		μs
			FSR Settling to 0.01% 25KΩ Feedback		25			5		μs
			for 1 LSB change		3			1.5		μs
			Summing Node Current to 0.01% FSR		—			2		μs
	Slew Rate				0.5			—		V/μs
Output	Output Current		V_{OUT} = +2.5V, ±5V, ±10V, 0 to +15V, 0 to +10V	±5				—		mA
	Output Impedance		7580V		0.05			—		Ω
	Output Impedance		7580I Unipolar		—			20		kΩ
			7580I Bipolar		—			12		kΩ
Power Supply	Supply Sensitivity					±0.002			±0.002	%FSR/%V
	Supply Voltage Range		(Note 3) $+V_S$	+11.4		+17.0	+11.4		+17.0	V
			(Note 3) $-V_S$	−11.4		−17.0	−11.4		−17.0	V
	Supply Current		$+V_S$ = +15.0V		6	13		5	10	mA
			$-V_S$ = −15.0V		4	9		3	6	mA
Temp.	Specification Range			0		+70	0		+70	°C
	Storage Range			−55		+100	−55		+100	°C

Note 1. Unless otherwise specified, performance specifications apply at T_C = +25°C, +12.0V ≤ $+V_S$ ≤ +15.0V and −12.0V ≤ $-V_S$ ≤ −15.0V. Also, for 7580V, I_L ≤ +5mA and for 7580I, I OUTPUT is held at virtual ground.
Note 2. See paragraph entitled Conversion Speed.
Note 3. 7580V supplies must be ±12.0V minimum for ±10.0V output ($+V_S$ = +12.0V minimum for 0 to +10V).

Complete Pin-For-Pin Compatibility With DAC80

The 7580 pin assignments and functions are completely compatible with the DAC80 in every way, although the internal circuit configuration is implemented with an R-2R ladder approach and internal resistor values are higher.

The only exception is the lack of requirement for a +5V logic supply at pin 13. Consequently, pin 13 of both the 7580V and 7580I has no internal connection, and the bypass capacitor can be eliminated.

Conversion Speed

The settling time for the 7580 is specified three ways. First, the 7580V voltage output model settling time includes switching time, current settling time at the summing node, output amplifier slew time, and finally settling within ±0.012% FSR of final value. Since the 7580 series emphasizes low cost and low power, a "741 type" output amplifier is used, providing a typical settling time of 25 μs

The 7580I settling time is specified two ways. First, since the inverted R-2R ladder network, leg currents are steered into COMMON or the summing node, settling time is specified in terms of the current settling time into virtual ground. This is a legitimate theoretical concept but very difficult to measure on a practical basis; therefore, the 7580I settling time is also specified using an external LM-318 op amp. This approach converts the very low summing node currents back into an easily measurable 10 volt full scale, and from a more practical viewpoint, includes all of the real world settling time ingredients listed above for the voltage output model.