Device 01 inactive for new design. Use M38510/31513B--.

C Remove vendor CAGE 18324. Add LCC package, logic diagram, and waveforms. Convert to military drawing format. Change code ident. no. to 67268.

CURRENT CAGE CODE 67268

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1. SCOPE

- 1.1 <u>Scope</u>. This drawing describes the requirements for monolithic silicon, low power Schottky TTL, counter microcircuits. This drawing provides a level of microcircuit quality and reliability assurance for acquisition of microcircuits in accordance with MIL-M-38510.
 - 1.2 Part number. The complete part number shall be as shown in the following example:







1.2.1 Device type. The device type shall identify the circuit function as follows:

Device	type

Generic number

Circuit

01

54LS190

Synchronous 4 bit BCD counter with mode control

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter

E F

Case outline

D-2 (16-lead, 1/4" x 7/8"), dual-in-line package F-5 (16-lead, 1/4" x 3/8"), flat package C-2 (20-terminal .350" x .350"), square chip carrier package

1.3 Absolute maximum ratings.

1.4 Recommended operating conditions.

 $\overline{1/\text{ Must withstand}}$ the added P_D due to short circuit test (e.g., I_{OS}).

MILITARY DRAWING

DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510

- Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883

Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

- 2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.
 - 3. REQUIREMENTS
- 3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.
- 3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.
 - 3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.
 - 3.2.2 Logic diagram. The logic diagram shall be as specified on figure 2.
 - 3.2.3 Truth table. The truth table shall be as specified on figure 3.
 - 3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.
- 3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.
- 3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

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DESC FORM 193A

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- 3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.
- 3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.
- 3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).
- 3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
 - 4. QUALITY ASSURANCE PROVISIONS
- 4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).
- 4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:
 - a. Burn-in test (method 1015 of MIL-STD-883).
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125^{\circ}C$, minimum.
 - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- 4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method $\overline{5005}$ of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.
 - 4.3.1 Group A inspection.
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 4, 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.
 - c. Subgroup 7 tests shall verify the truth table.
 - 4.3.2 Groups C and D inspections.
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125^{\circ}C$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

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ТАВ	LE I. E	ectrical performance characteristi	cs.			
Test	Symbol	Conditions	Group A		nits	Unit
		Conditions -55°C < T _C < +125°C unless otherwise specified	subgroups	Min	Max	Γ
High-level output voltage	Voн	$ V_{CC} = 4.5 \text{ V}; I_{OH} = -400 \mu \text{A}$ $ V_{IN} = 0.7 \text{ V or } 2.0 \text{ V}$	1, 2, 3	 2.5 	 	! ! Y !
Low-level output voltage	V ₀ L	$ V_{CC} = 4.5 \text{ V}; I_{OL} = 4 \text{ mA}$ $ V_{I,N} = 0.7 \text{ V or 2.0 V}$	1, 2, 3		0.4	 V
Input clamp voltage	VIC	 V _{CC} = 4.5 V; I _{IN} = -18 mA T _C = +25°C	1 1		 -1.5 	V
High level input current at all inputs except enable	IIHI	V _{CC} = 5.5 V; V _{IN} = 2.7 V	1, 2, 3		20	μ Α
	I IH2	V _{CC} = 5.5 V; V _{IN} = 5.5 V	1, 2, 3		100	Ι μ Α
High level input current at enable	I _{IH3}	V _{CC} = 5.5 V; V _{IN} = 2.7 V	1, 2, 3		 60 	 μΑ
	I IH4	V _{CC} = 5.5 V; V _{IN} = 5.5 V	1, 2, 3		300	μ Α
Low level input current at inputs except enable	I _{IL1}	V _{CC} = 5.5 V; V _{IN} = 0.4 V	1, 2, 3		 40 	mA
Low level input current at enable	IIL2	V _{CC} = 5.5 V; V _{IN} = 0.4 V	1, 2, 3		-1.2	mA
Short circuit output current	Ios	V _{CC} = 5.5 V <u>1</u> /	1, 2, 3	-15	 -130 	l inA l
Current supply	Icc	 V _{CC} = 5.5 V	1, 2, 3		 35 	mA
Functional tests		 See 4.3.1c 	7 7		 	
Maximum clock frequency	FMAX	$ V_{CC} = 5.0 \text{ V}$ $ C_L = 15 \text{ pF } \pm 10\%$ $ R_L = 2 \text{ k}\Omega \pm 5\%$	9	20		MHz
	; 		10, 11	15		MHz
<u>2</u> /	<u> </u> 		9	15		MHz

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10, 11

1 10

MHz

TABLE	I. Electri	cal performance	characteristics - Co	ontinued.			
Test	Symbol	Cond	litions	 Group A		nits	Unit
		-55°C < T unless othe	C < +125°C rwise specified	subgroups	subgroups Min		
Propagation delay time, high-to-low level	t _{PHL} 1	$ V_{CC} = 5.0 \text{ V}$ $ R_{L} = 2 \text{ k}\Omega \pm 5\%$	C _L = 15 pF ±10%	9		50	ns
output from load to Q outputs		See figure 4		10, 11		70	ns
<u>2</u> /			C _L = 50 pF ±10%	9		55	ns
		 		10, 11		 77 	ns
Propagation delay time, low-to-high level output from load to	t _{PLH1}		C _L = 15 pF ±10%	9	 	33	ns
Q outputs				10, 11	 	46	ns
2/			C _L = 50 pF ±10%	j 9	i ! !	38	l ns
		<u> </u>		10, 11	t 	53	l ns
Propagation delay time, high-to-low level output from data to	t _{PHL2}		C _L = 15 pF ±10%	9	 	40	ns
Q outputs				10, 11		56	ns
<u>2</u> /	ļ ļ		$C_L = 50 \text{ pF } \pm 10\%$	9		45	l ns
		<u> </u>		10, 11	İ 	63	i ns
Propagation delay time, low-to-high level output from data to	t _{PLH2}		C _L = 15 pF ±10%	9	<u> </u> 	32	ns
Q outputs				10, 11	<u> </u>	45	ns
<u>2</u> /			C _L = 50 pF ±10%	9		37	ns
	!	ļ		10, 11		52	ns

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Test	Symbol	Cond	itions	Group A	Limits	Unit
1630		-55°C < T	√ +125°C wise specified	subgroups	Min Ma	
Propagation delay time, high-to-low level	t _{PHL3}	$ V_{CC} = 5.0 \text{ V}$ $ R_{L} = 2 \text{ k}\Omega \pm 5\%$	C _L = 15 pF ±10%	9	2	4 ns
output from clock to ripple clock		See figure 4 		10, 11	3	4 ns
<u>2</u> /		 	C _L = 50 pF ±10%	9	2	9 ns
				10, 11	4	1 ns
Propagation delay time, low-to-high level	t _{PLH3}	T 	C _L = 15 pF ±10%	9	2	0 ns
output from clock to ripple clock	 			10, 11	2	8 ns
2/	 		C _L = 50 pF ±10%	9	2	5 ns
		[10, 11	3	5 ns
Propagation delay time, high-to-low level	tpHL4	1	C _L = 15 pF ±10%	9	 3	6 ns
output from clock to Q outputs				10, 11	 	60 ns
<u>2</u> /	! 	[[C _L = 50 pF ±10%	9	4	1 ns
	l 		 	10, 11	 5	7 ns
Propagation delay time, low-to-high level	tpLH4	T 	C _L = 15 pF ±10%	9	2	24 ns
output from clock to Q outputs			1	10, 11] 3	84 ns
<u>2</u> /	2/	C _L = 50 pF ±10%	9	2	.9 ns	
	ļ		į Į	10, 11	4	1 ns

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DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO		REV	С		PAGE	7

TABLE 1	Liectri	cal performance (<u>characteristics</u> - Co				
Test	Symbol	Cond	litions	Group A	Limits		 Unit
		-55°C < T unless othe	litions C < +125°C rwise specified	subgroups	Min	Max	
Propagation delay time, high-to-low level	t _{PHL} 5	$ V_{CC} = 5.0 \text{ V}$ $ R_L = 2 \text{ k}\Omega \pm 5\%$	C _L = 15 pF *10%	9		52	ns
output from clock to MAX/MIN		See figure 4		10, 11		73	ns
<u>2</u> /	 	 	C _L = 50 pF ±10%	9		 57 	ns
	 	 		10, 11		l 80 	l ns
ropagation delay time, low-to-high level	t _{PLH5}	T -	C _L = 15 pF ±10%	9		 42 	ns
output from clock to MAX/MIN				10, 11		59	ns
<u>2</u> /		 	C _L = 50 pF ±10%	9		47	ns
				10, 11		66	ns
ropagation delay time, high-to-low level	t _{PHL6}		C _L = 15 pF ±10%	9		45	ns
output from down/up to ripple clock				10, 11		63	ns
<u>2</u> /		 	 C _L = 50 pF ±10%	9		50	ns
				10, 11		70	l l ns
ropagation delay time, low-to-high level	t _{PLH6}		C _L = 15 pF ±10%	9		45	l ns
output from down/up to ripple clock				10, 11		63	l ns
2/		 	C _L = 50 pF ±10%	9		i 50	l ns
				10, 11	ļ	70	ns

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T 4	C.mbal	Cond	 Group A	Lir	nits	Unit	
Test	Symbol	-55°C < T unless othe	litions C < +125°C crwise specified	subgroups	Min	Max	
Propagation delay time, high-to-low level	t _{PHL} 7	$\begin{vmatrix} V_{CC} = 5.0 & V \\ R_L = 2 & k\Omega & \pm 5\% \end{vmatrix}$	C _L = 15 pF ±10%	9		33	ns
output from down/up to MAX/MIN	to See figure 4 	10, 11		46	ns		
<u>2</u> /	. 	 	C _L = 50 pF ±10%	9		 38 	l ns
				10, 11		 53 	ns
Propagation delay time, low-to-high level	t _{PLH7}	T	C _L = 15 pF ±10%	9] 33 	ns
output from down/up to MAX/MIN				10, 11		 46 	ns
<u>2</u> /		 		9		38	ns
		 		10, 11		 53 	ns
Propagation delay time, high-to-low level	t _{PHL8}	- †	C _L = 15 pF ±10%	9		33	ns
output from enable to ripple clock	İ			10, 11	l	46	ns

 $|C_L = 50 pF \pm 10\%$

C_L = 15 pF ±10%

 $|C_L = 50 pF \pm 10\%$

9

10, 11

9

10, 11

9

10, 11

38

53

33

46

38

53

ns

ns

ns

ns

ns

ns

TABLE I. Electrical performance characteristics - Continued.

1/ Not more than one output should be shorted at a time, and the duration of the short circuit condition should not exceed 1 second.

tPLH8

Propagation delay time testing and maximum clock frequency testing may be performed using either $C_{\parallel}=15$ pF or $C_{\parallel}=50$ pF. However, the manufacturer must certify and guarantee that the microcircuits meet the switching test limits specified for a 50 pF load.

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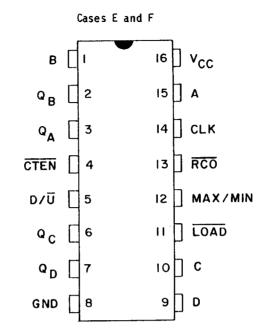
2/

Propagation delay time, low-to-high level

ripple clock

2/

output from enable to



Case 2

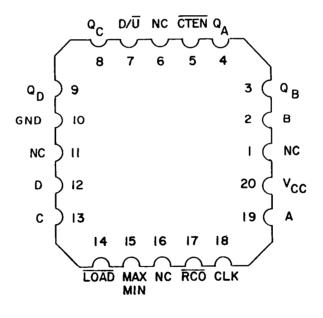
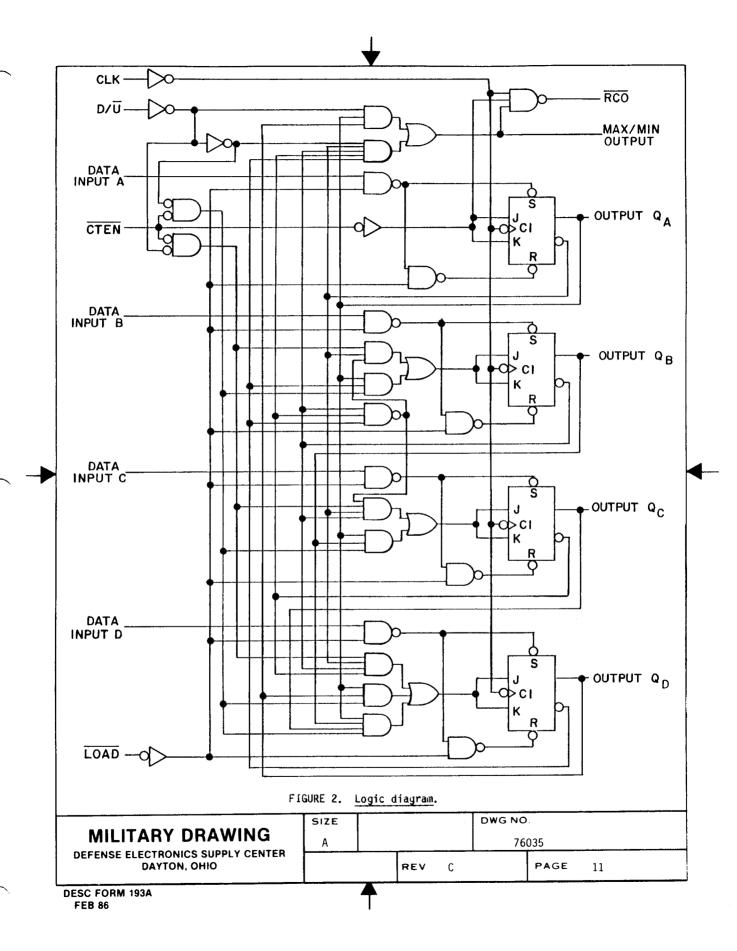


FIGURE 1. Terminal connections.

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Mode select table

 	Inpu	Mode		
Load	Enable G	Down/up	CK	
н	L	L	1	Count up
н	L	 H	1	Count down
 L	x	i x	X	 Preset (asyn)
 H 	! H 	 X 	 X 	l No change (hold)

RC truth table

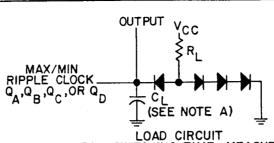
Inpu	ts	Outputs				
Enable G	CK	Max/min	Ripple clock outputs			
 L 	 T	Н	T			
 H 	X	X	l H			
X	X	L I	 H 			

Max/min is generated internally.

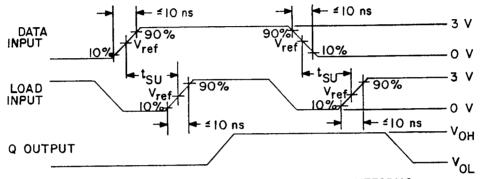
L = LOW voltage level
H = HIGH voltage level
X = Don't care
____ = LOW-to-HIGH clock transition
U = LOW pulse

FIGURE 3. Truth table.

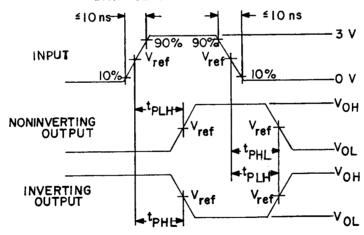
DWG NO. SIZE 76035 **MILITARY DRAWING** Α DEFENSE ELECTRONICS SUPPLY CENTER REV C DAYTON, OHIO PAGE 12



LOAD CIRCUIT
FOR SWITCHING TIME MEASUREMENT



DATA SETUP TIME VOLTAGE WAVEFORMS



GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

NOTE: CL includes probe and jig capacitance.

V_{REF} = 1.3 V.

FIGURE 4. Waveforms.

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Typical load, count, and inhibit sequences

Illustrated below is the following sequence:

- 1. Load (preset) to BCD seven.
- 2. Count up to eight, nine (maximum), zero, one, and two.
- 3. Inhibit.
- 4. Count down to one, zero (minimum), nine, eight, and seven.

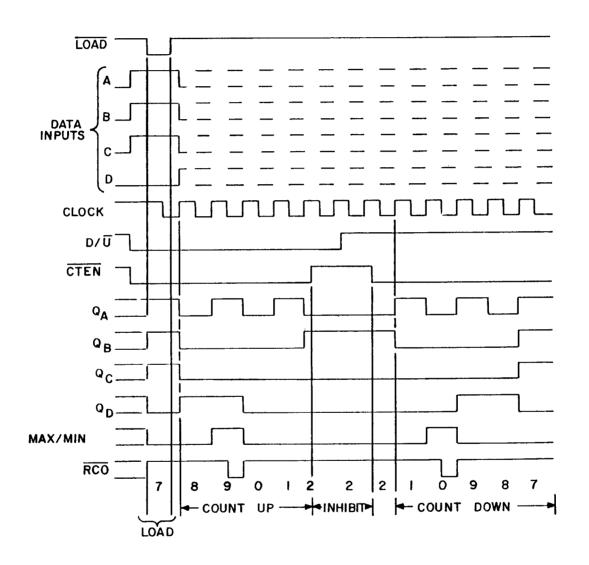
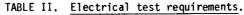


FIGURE 4. Waveforms - Continued.

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MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 9
[Group A test requirements (method 5005)	1, 2, 3, 7, 9, 1 10, 11
[Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

^{*} PDA applies to subgroup 1.

5. PACKAGING

- 5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.
- 6. NOTES
- 6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.
 - 6.2 Replaceability. Replaceability is determined as follows:
 - a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
 - b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/31513B--.
- 6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

MILITARY DRAWING

DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO

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6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawi part number	Vendor CAGE number	Vendor similar part number <u>1</u> /	Replacement military specification part number
7603501EX <u>2</u> ,	/ 04713 01295	54LS190/BEAJC SNJ54LS190J	M38510/31513BEX
7603501FX 2,	/ 04713 01295	54LS190/BFAJC SNJ54LS190W	M38510/31513BFX
76035012X <u>2</u>	/ 04713 01295	54LS190 M/B2AJC SNJ54LS190FK	M38510/31513B2X

 $[\]frac{1}{-}$ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Device 01 inactive for new design, use QPL product M38510/31513B--.

Vendor CAGE number	Vendor name and address				
01295	Texas Instruments, Incorporated P. O. Box 6448 Midland, TX 79701				
04713	Motorola, Incorporated 7402 South Price Road Tempe, AZ 85283				

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