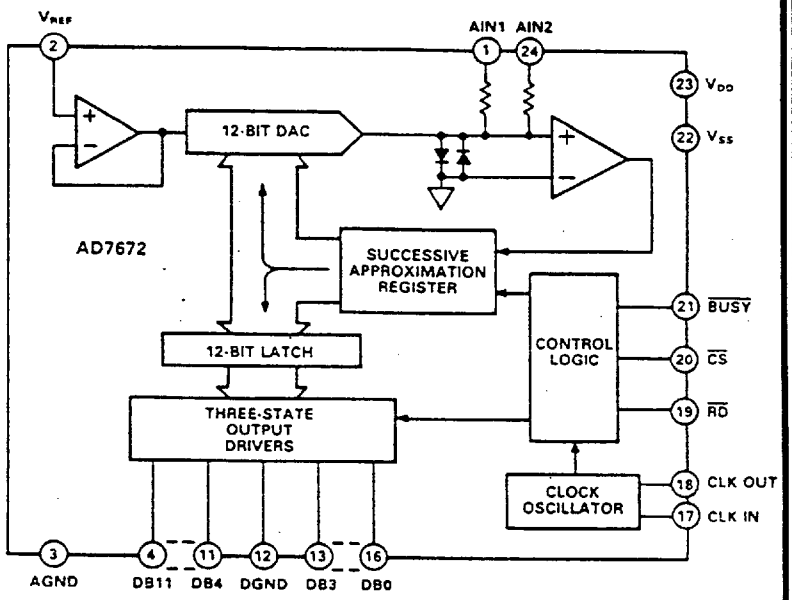
12 Bit A/D Converter - Radiation Hardened

7672RP

Class S Screening
High Speed BiCMOS

For Space Applications



SEI's 7672RP (RP for RAD-PAK®) high speed BiCMOS microcircuit features a minimum 100 kilorad (Si) total dose tolerance. Fully equivalent to the commercial 7672, the 7672RP combines Maxim's advanced BiCMOS, mixed technology process and SEI's radiation hardened RAD-PAK® packaging. The 7672RP uses an accurate high-speed DAC and comparator in an otherwise conventional successive-approximation loop to achieve conversion times as low as 3us while dissipating only 110 mW of power. The 7672RP is designed to be used with an external reference voltage. This allows the user to choose a reference whose performance suits the application or to drive a number of the 7672RPs from a single system reference, since the reference input is buffered and draws very little current. For digital signal processing applications where absolute accuracy and temperature coefficients may be unimportant, a low cost reference can be used. For optimal precision, a high accuracy reference where an absolute 12-bit accuracy can be obtained over a wide temperature range may be used. Capable of surviving space environments, the 7672RP is ideal for satellite, spacecraft, and space probe missions. RAD-PAK® incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. The 7672RP has a 100 krad (Si) total dose survivability.

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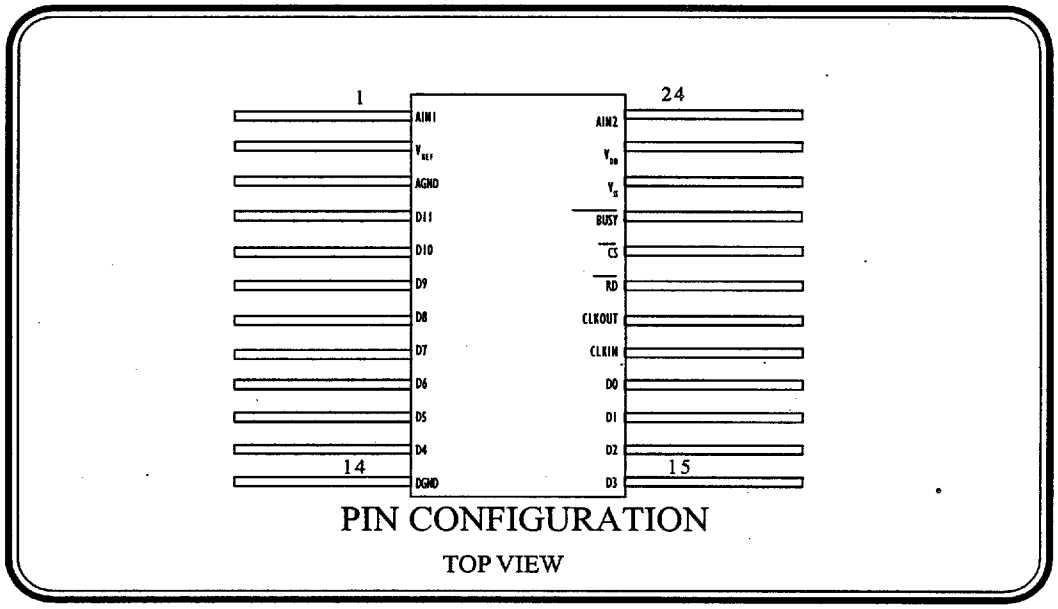
SEI 7672RP RADHARD 12 bit A to D CONVERTER

Radiation Hardened
7672RP

BiCMOS 12 Bit
Analog to Digital Converter



PIN CONFIGURATION

TOP VIEW

Features:

- 12 Bit Resolution and Accuracy
- Pin Compatible with MX7672, AD7672
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
  - Single Event Upset LET = 20 MeV(mg/cm²)
  - No Single Event Latchup
- Package:
  - 24 Pin RAD-PAK® flat pack (640 mils x 420 mils)
  - Weight – 4.8 grams
- Fast Conversion Times:
  - 7672RP-05: 5 usec
  - 7672RP-10: 10 usec
- Low 110 mW Typical Power Consumption
  - Corrects all single-bit errors
  - Detects all double and some triple-bit errors
- High Speed BiMOS Technology
  - Choice of +5V, +10V, or ±5V Input Ranges
  - Buffered Reference Input
  - Operates with +5V and -12V Power Supplies
  - Fast 125 ns Bus-Access Time
- Screening per TM 5004
- QCI per TM5005

TQM
Total Quality Management

January 1996

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7672RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Positive Supply Voltage	V_{dd}	-0.3	7.0	V
Negative Supply Voltage	V_{ss}	+0.3	-17	V
AGND to DGND		-0.3	V_{dd}+0.3	V
AIN1, AIN2 to AGND		-15	+15	V
Digital Input Voltage	V_{IN}	-0.3	V_{dd}+0.3	V
Digital Output Voltage	V_{OUT}	-0.3	V_{dd}+0.3	V
VREF to AGND		V_{SS}-0.3	V_{dd}+0.3	V
Power Dissipation to +75°C	P_d		1000	mW
Power Dissipation above +75°C (Derate)			10	mW/°C
Storage Temperature Range	T_S	-65	+150	°C
Operating Temperature Range	T_A	-55	+125	°C

7672RP RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Positive Supply voltage	V_{dd}	4.75	5.25	V
Negative Supply Voltage	V_{ss}	-13.2	-10.8	V
V_{REF} Input range		-5.05	-4.95	V
Power Dissipation V_{dd} = 5V, V_{ss} = -12V	P_d		179	mW

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7672RP ELECTRICAL CHARACTERISTICS[1]

PARAMETER	SYMBOL	MIN	MAX	UNIT
Integral Nonlinearity	INL	-3/4	+3/4	LSB
Differential Nonlinearity	DNL	-0.9	+0.9	LSB
Unipolar Offset Error T_A = +25 °C T_A = -55 to +125 °C		 -3 -4	 +3 +4	LSB
Unipolar Gain Error T_A = +25 °C T_A = -55 to +125 °C		 -4 -6	 +4 +6	LSB
Bipolar Zero Error T^A = +25 °C T_A = -55 to +125 °C		 -3 -4	 +3 +4	LSB
Bipolar Gain Error T_A = +25 $_O$C T_A = -55 to +125 °C		 -4 -6	 +4 +6	LSB

Notes:

1. V_{dd} = 5±5% Volts; V_{ss} = -12±10% Volts; V_{REF} = -5 Volts; T_A = -55 to +125 °C

7672RP DC ELECTRICAL CHARACTERISTICS[1]

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.4		V
Output Low Voltage: Isink = 1.6 mA	V_{OL}		0.4	V
Output High Voltage: Isource = 200 uA	V_{OH}	4.0		V
Input Leakage Current	I_{IN}			uA
Output Leakage Current	I_{CC}	-10	+10	uA
Input Capacitance[2]	C_{IN}		10	pF
Output Capacitance[2]	C_{OUT}		15	pF
Power Supply Rejection, V_{dd}		-2	+2	LSB
Power Supply Rejection, V_{ss}		-1	+1	LSB
Analog Input Current (AIN1 or AIN2)				uA
V_{REF} Input Current		-3	+3	uA

Notes:

1. V_{dd} = 5±5% Volts; V_{ss} = -12±10% Volts; V_{REF} = -5 Volts; T_A = -55 to +125 °C.
2. Guaranteed by design.

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7672RP TIMING CHARACTERISTICS[1,3]

PARAMETER	SYMBOL	MIN	MAX	UNIT
Conversion Time, -03 device Synchronous Clk, 12.5	t_{CONV}		3.125	us
Conversion Time, -05 device Synchronous Clk, 12.5	t_{CONV}		5.0	us
Conversion Time, -10 device Synchronous Clk, 12.5	t_{CONV}		10.0	us
Conversion Time, -03 device Asynchronous Clk, 12-13	t_{CONV}	3.0	3.25	us
Conversion Time, -05 device Asynchronous Clk, 12-13	t_{CONV}	4.8	5.2	us
Conversion Time, -10 device Asynchronous Clk, 12-13	t_{CONV}	9.6	10.4	us
CS\ to RD\ Setup Time[2]	t_1	0		ns
RD\ to BUSY\ Delay: C_L = 50 pF	t_2		270	ns
Data Access Time[4]: C_L = 50 pF	t_3		170	ns
RD\ Pulse Width[2]	t_4	t_3		ns
CS\ to RD\ Hold Time[2]	t_5	0		ns
Data Setup Time After BUSY\ [4]: C_L = 100 pF	t_6		100	ns
Bus Relinquish Time[5]	t_7		90	ns
Delay Between Read Operations	t_8	200		ns
CLKIN to BUSY\ Delay[2]	t_9		180	ns
RD\ to CLKIN Setup/Hold Time[2]	t_{10}	25	100	ns

Notes:

1. V_{dd} = +5 Volts; V_{ss} = -12 Volts; 1LSB = FS/4096; T_A = +25 °C; Performance over power supply tolerance is guaranteed by power supply rejection test.
2. Guaranteed by design.
3. All inputs are 0V to +5V swing with $t_r = t_f$ =5ns (10 to 90% of +5V) and timed from a voltage level of +1.6V.
4. t_3 and t_6 are measured with the load circuits of Figure 1 and are defined as the time required for an output to cross +0.8V or +2.4V.
5. t_7 is defined as the time required for the data linew to change 0.5V when

7672RP Package Ordering Guide

Package Style	Case Outline 1/	Description
D	D-24	24 Pin Dual In Line Package
F	F-24	24 Pin Flat Package

Note:

1/ For outline information, see Appendix A (Package Information - Outline Dimension)

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