REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Pgs. 10, 11 - added two package versions with same dimensions as original. Pg. 12 - modified par. 3.6.2. modified par. 4.2. Pg. 2 - decrease operation frequency. Pgs. 5, 6, 7 - decrease prop delay times.	9/22/77	M.A. Frank
B	Pg 1 - Document Inactive	1/25/78	M.A.F.

INACTIVE FOR NEW DESIGN AS OF
25 JAN 1978. USE M38510/42001B

Prepared in accordance with MIL-STD-100 — Selected item drawing

REV																																									
PAGE																																								
REV STATUS	REV	B	A			A	A	A		A	A	A	A																											
OF PAGES	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15																								

Original Date of Drawing
3 February 1977

PREPARED BY: A J Foley 2 Feb 77

CHECKED BY: C. R. Jackson 3 Feb 77

APPROVED BY: M.A. Frank 3 Feb 77

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO

TITLE: 8080A
Microprocessor, 8-Bit
N-Channel, Single Chip,
Microcircuit, Silicon Gate

SIZE	CODE IDENT. NO.	DWG NO.
A	14933	77002

REV B — PAGE 1 OF 15

DESC FORM 144
MAR 76

5962-E-129

1. SCOPE

1.1 Scope. This drawing describes the requirements for monolithic silicon, N-channel, 8-Bit Microprocessor microcircuit. This drawing provides for a level of microcircuit quality and reliability assurance for procurement of microcircuits in accordance with MIL-M-38510.

1.2 Part number. The complete part number shall be as shown in the following example:

77002	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish (3.3)

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit
01	8080A	8 bit fixed instruction microprocessor

1.2.2 Case outline. The case outline shall be as shown in figure 2.

Outline letter	Case outline
Q	(40 Pin Ceramic dual-in-line pack)

1.3 Absolute maximum ratings.

V_{CC} Supply Voltage, V_{DD} Supply Voltage, V_{SS} Supply Voltage, Input and Output Voltage (WITH RESPECT TO V_{BB})	-0.3 to +20 Vdc
Storage Temperature Range	-65 to +150°C
Power Dissipation	1.7 W
Lead Temperature (Soldering 5 seconds)	270°C
Maximum Junction Temperature	T_J = (150°C)
Thermal Resistance Junction to Case	(θ_{J-C} = 50°C/W)

1.4 Recommended Operating Conditions

Supply Voltage	V_{BB}	-4.5 V to -5.5 V
	V_{CC}	+4.5 V to +5.5 V
	V_{DD}	+10.8 V to +13.2 V
	V_{SS}	0 V
Minimum High Level Input Voltage	(logic inputs)	3.0 V
	(clock inputs)	8.5 V
Maximum Low Level Input Voltage (logic & clock inputs)		0.8 V
Maximum High Level Output Voltage		3.7 V
Maximum Low Level Output voltage		0.45 V
Frequency of Operation		0.5 MHz to 2.083 MHz
Ambient Operating Temperature Range		-55° to + 125°C

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Design documentation. The design documentation shall be in accordance with MIL-M-38510 and, unless otherwise specified in the contract or purchase order, shall be retained by the manufacturer but be available for review by the procuring activity or contractor upon request.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510.

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I and apply over the full recommended ambient operating temperature range, unless otherwise specified.

3.5 Marking. Marking shall be in accordance with MIL-M-38510 except the part number shall be in accordance with 1.2 herein, The M38510/XXX part number, and the "JAN" or "J" mark shall not be used.

3.6 Product assurance requirements. Microcircuits furnished under this drawing shall have been subjected to, and passed all the requirements, tests, and inspections detailed herein including screening, and quality conformance inspection requirements.

Table I. Electrical Characteristics.

Test	Symbol	Conditions	Device type	Limits Min	Limits Max	Units
High Level Output Voltage All Outputs	V_{OH}	V_{DD} = +10.8 V I_{OH} = -150 µA V_{BB} = -5.5 V, V_{CC} = +4.5 V	01	3.7	---	Volts
Low Level Output Voltage All Outputs	V_{OL}	V_{DD} = +10.8 V I_{OL} = 1.9 mA V_{BB} = -5.5 V, V_{CC} = 4.5 V	01	---	0.45	Volts
High Level High Impedance Output Current D_0-D_7, A_0-A_{15}	I_{ZH1}	V_O = +5.5 V T_A = +125°C, +25°C V_{BB} = -5.5 V, V_{CC} = +5.5 V V_{DD} = +10.8 V	01	---	10	µA
Low Level High Impedance Output Current D_0-D_7, A_0-A_{15}	I_{ZL1}	V_O = 0.45 V T_A = +125°C, +25°C V_{BB} = -4.5 V, V_{CC} = +5.5 V V_{DD} = 13.2 V	01	-10	-100	µA
High Level Input current; For Clock Inputs, Reset, Hold, Int, and Ready	I_{IH1}	Logic / Clock V_{IN} = 5.5 V / 13.2 V V_{BB} = -5.5 V / -5.5 V V_{CC} = +5.5 V / +4.5 V V_{DD} = 10.8 V / 13.2 V T_A = +125°C, / +25°C	01	---	10	µA
Low Level Input Current: For Clock Inputs, Reset, Hold, Int, and Ready	I_{IL1}	V_{IN} = 0 V V_{BB} = -4.5 V V_{CC} = +5.5 V V_{DD} = +13.2 V T_A = +125°C, +25°C	01	---	-10	µA
High Level Input Current; Data Bus in input mode D_0 - D_7	I_{IH2}	V_{IN} = 3.7 V V_{BB} = -4.5 V, V_{CC} = +5.5 V V_{DD} = +13.2 V T_A = +125°C, +25°C	01	-.4	-1.2	mA
Low Level Input Current; Data Bus in input mode D_0 - D_7	I_{IL2}	V_{IN} = 0 V V_{BB} = -4.5V, V_{CC} = +5.5 V V_{DD} = +13.2 V T_A = +125°C, +25°C	01	-10	-100	µA

TABLE I. Electrical Characteristics - Continued.

Test	Symbol	Conditions	Device type	Limits Min	Limits Max	Units
High Level Input Current Data Bus in Input Mode D_0 D_7	I_{IH3}	V_{BB} = -4.5 V, V_{CC} = +5.5 V V_{DD} = 13.2 V V_{IN} = 5.0 V, T_A = 125°C, 25°C	01	-10	-100	μA
Input High Threshold: All Inputs Except Clock	V_{IH1}	V_{BB} = -4.5 V -5.5 V V_{CC} = +4.5 V, 5.5 V V_{DD} = 10.8 V, 13.2 V	01	3.0	---	Volts
Input Low Threshold; All Inputs Including Clocks	V_{IL1}		01	---	0.8	Volts
Input High Threshold; Clock Inputs	V_{IH2}		01	8.5	---	Volts
Negative 5 V Power Supply Current	I_{BB}	f = 2.0 MHz V_{BB} = -5.5 V V_{CC} = +5.5 V V_{DD} = +13.2 V	01	.01	1.0	mA
Positive 5 V Power Supply Current	I_{CC}		01	10	100	mA
Positive 12 V Power Supply Current	I_{DD}		01	10	80	mA
Input Capacitance $\emptyset_1$, $\emptyset_2$	C_i	F = 1 MHz T_A = 25°C From Input pins to all other pins	01	17	25	pF
Input Capacitance Ready, Hold, int, D_0-D_7, Reset	C_i		01	6	10	pF
Output Capacitance A_0-A_{15}, Sync, DBIN, WAIT, WR, HLDA, INTE	C_O		01	10	20	pF
Clock Pulse Width Ø1	t_{WH1}	V_{BB} = -5V ±10% V_{CC} = +5V ±10% V_{DD} = +12 V ±10%	01	60	---	ns
Clock Pulse Width Ø2	t_{WH2}		01	220	---	ns
Delay Ø1 to Ø2 Leading Edges	t_{SLH7}		01	80	---	ns
Delay Ø1 to Ø2	T_{SLH6}		01	0	---	ns
Delay Ø2 to Ø1	t_{SHL8}		01	70	---	ns

TABLE I. Electrical Characteristics - Continued.

Test	Symbol	Conditions	Device type	Limits Min	Limits Max	Units
Ready Setup Time to Ø2	t_{SLH1}	V_{BB} = -5 V ±10% V_{CC} = +5 V ±10% V_{DD} = +12 V ±10%	01	120	---	ns
	t_{SHL1}		01	120	---	ns
Data Setup Time to Clock Ø1	t_{SLH2}		01	30	---	ns
	t_{SHL2}		01	30	---	ns
Data Setup Time to Clock Ø2	t_{SLH3}		01	150	---	ns
	t_{SHL3}		01	150	---	ns
INT Input Setup Time During Ø1 or Ø2. INT Not Valid	t_{SLH4}		01	120	---	ns
	t_{SHL4}		01	120	---	ns
Hold Input Setup Time to Ø2	t_{SHL5}		01	140	---	ns
	t_{SLH5}		01	140	---	ns
Data Hold Time From Ø2	t_{HHL2}		01	50	---	ns
	t_{HLH2}		01	50	---	ns
INT Input Hold Time During Ø1 or Ø2, INT Valid	t_{HHL1}		01	0	---	ns
	t_{HLH1}		01	0	---	ns
Clock Period	t_{CY}		01	0.32	2.0	μS
Data and Status Output Delay from Ø2: D_0-D_7 Data and Status Valid	t_{PLH1}	C = 50 pF all outputs T_A = +25°C	01	---	220	ns
	t_{PHL1}		01	---	220	ns
	t_{pZH1}		01	---	220	ns
	t_{pZL1}		01	---	220	ns
Delay for Data Bus to Enter Input Mode. D_0-D_7	t_{PHZ1}	R_L = 2.2KΩ R = 25KΩ C = 50 pF all outputs T_A = +25°C	01	---	140	ns
	t_{PLZ1}		01	---	140	ns

TABLE I. Electrical Characteristic - Continued.

Test	Symbol	Conditions	Device type	Limits Min	Limits Max	Units
Delay to Float During Hold From Ø2 A_0-A_{15}: D_0-D_7	t_{PLZ2}	R_L = 2.2KΩ R = 25KΩ C = 50 pF all outputs T_A = +25°C	01	---	120	ns
	t_{PHZ2}		01	---	120	ns
DBIN Output Delay From Ø2	t_{PLH3}		01	25	140	ns
	t_{PHL3}		01	25	140	ns
Delay to Float During Hold From HLDA A_0-A_{15}, D_0-D_7	t_{PHZ3}		01	1/		
	t_{PLZ3}		01	1/		
SYNC, $\overline{WR}$, WAIT, $\overline{HLDA}$ Output Delay	t_{PLH4}		01	---	120	ns
	t_{PHL4}		01	---	120	ns
Address and Data Delay to Float During Hold From $\overline{WR}$, A_0-A_{15}, D_0-D_7	t_{PHZ4}		01	2/		ns
	t_{PLZ4}			2/		ns
INTE Output Delay from Ø2	t_{PHL5}		01	---	200	ns
	t_{PLH5}		01	---	200	ns
Address Valid after DBIN During HLDA	t_{PHZ5}		01	-20	---	ns
	t_{PLZ5}		01	-20	---	ns
Address Output Delay from Ø2 Address Valid A_0-A_{15}	t_{PLH6}		01	---	200	ns
	t_{PHL6}		01	---	200	ns
Output Data Stable Prior to $\overline{WR}$ 1 D_0-D_7	t_{PLH7}		01	3/		ns
	t_{PHL7}		01	3/		ns
Address Stable Prior to $\overline{WR}$ A_0-A_{15}	t_{PLH8}		01	4/		ns
	t_{PHL8}		01	4/		ns
Output Data, Address Stable From $\overline{WR}$ (Not HLDA). D_0-D_7, A_0-A_{15}	t_{PHL9}		01	5/		ns
	t_{PLH9}		01	5/		ns

/ See notes on page 8

TABLE I. Electrical Characteristics - Continued.

Table Notes:

The following equations determine the minimum limits for the noted Table I delay measurements.

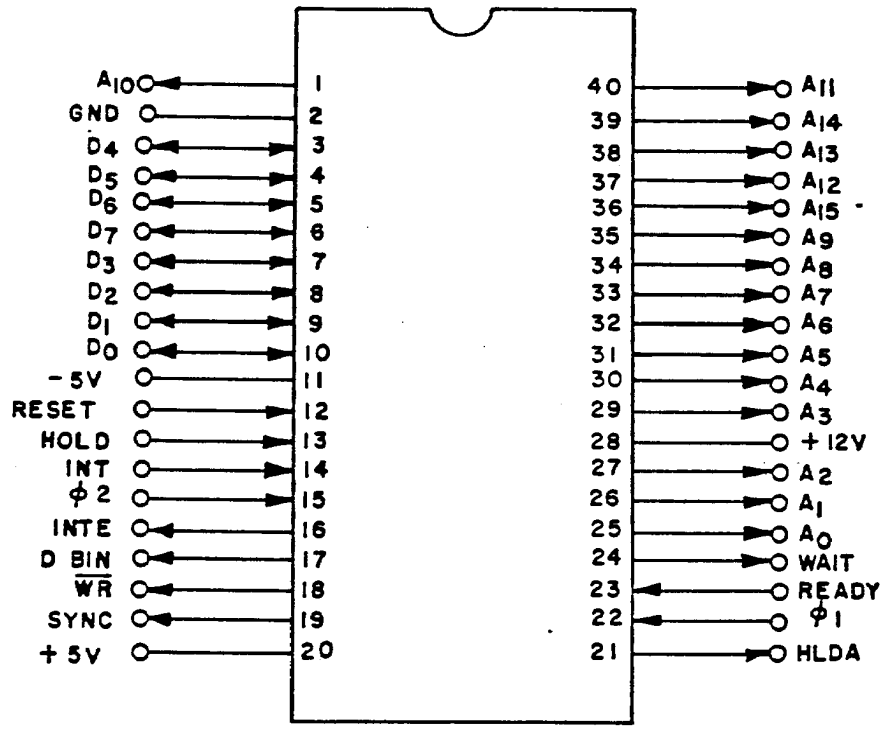
1/ t_{PHZ_3} and $t_{PLZ_3} = t_{SLH_7} + t_{TLH_{\emptyset 2}} - 50$ ns

2/ t_{PHZ_4} and $t_{PLZ_4} = t_{SLH_7} + t_{TLH_{\emptyset 2}} - 10$ ns

3/ t_{PHL_7} and $t_{PLH_7} = t_{period_{(clock)}} - t_{SLH_7} - t_{TLH_{\emptyset 2}} - 170$ ns

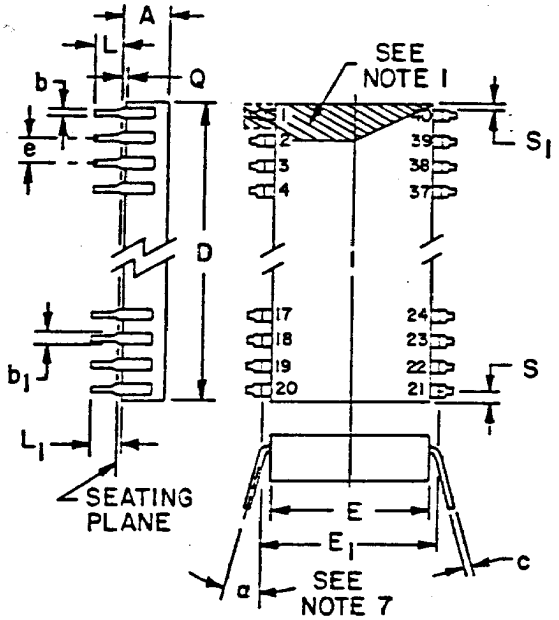
4/ t_{PHL_8} and $t_{PLH_8} = 2t_{period_{(clock)}} - t_{SLH_7} - t_{TLH_{\emptyset 2}} - 140$ ns

5/ t_{PHL_9} and $t_{PLH_9} = t_{SLH_9} + t_{TLH_{\emptyset 2}} + 10$ ns

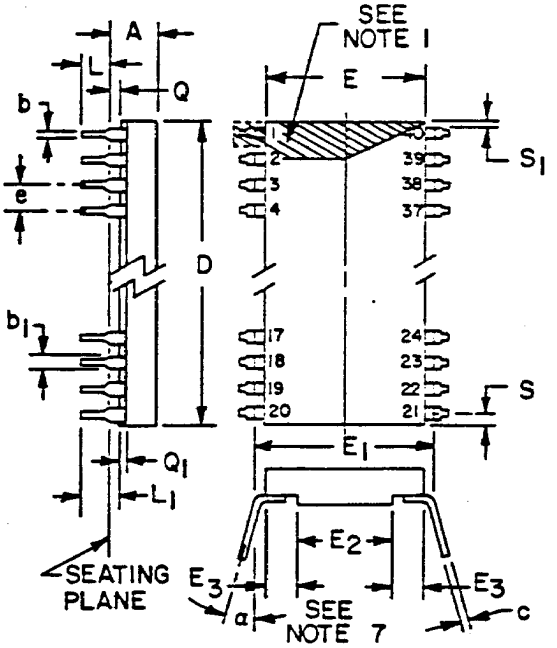


Device type 01

FIGURE 1. Terminal connections.



CONFIGURATION 1



CONFIGURATION 2 (SEE NOTE 10)

FIGURE 2. Case outline Q (40-lead, 5/16" x 2-1/16" dual-in-line pack).

DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 14933	DWG NO. 77002
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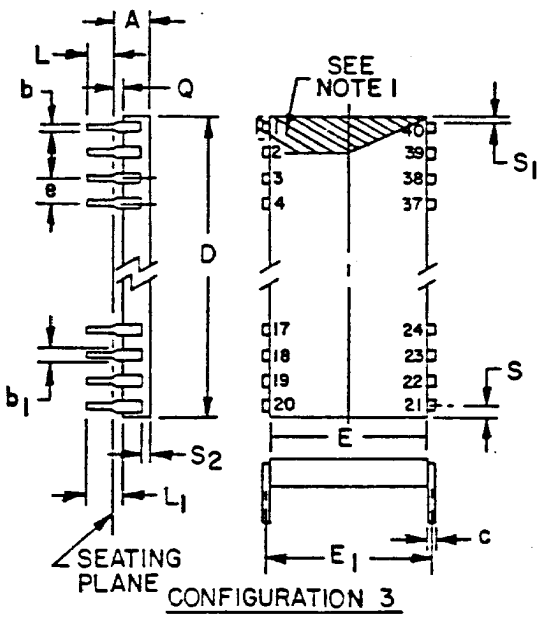

CONFIGURATION 3

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	---	.225	---	5.72	
b	.014	.023	.36	.58	8
b_1	.030	.070	.76	1.78	2,8
c	.008	.015	.20	.38	8
D	---	2.080	---	52.83	4
E	.510	.615	12.95	15.62	4
E_1	.520	.625	13.21	15.88	7
E_2	.280	---	7.11	---	
E_3	.050	---	1.27	---	
e	.100 BSC		2.54 BSC		5,9
L	.120	.200	3.05	5.08	
L_1	.150	---	3.81	---	
Q	.020	.060	.51	1.52	3
Q_1	.020	---	.51	---	
S	---	.080	---	2.03	6
S_1	.005	---	.13	---	6
S_2	.005	---	.13	---	
α	0°	15°	0°	15°	

NOTES:
1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be .020 (.51 mm) for leads number 1, 20, 21, and 40 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact logitudinal position relative to pins 1 and 40.
6. Applies to all four corners (leads number 1, 20, 21, and 40), and 40.5 shall apply.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads (see 40.4 of this appendix).
8. All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
9. Thirty eight spaces.
10. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

FIGURE 2. Case outline Q (40-lead, 5/16" x 2-1/16" dual-in-line pack) - Continued.

3.6.1 Screening. Screening shall be in accordance with method 5004, class B, of MIL-STD-883 and 4.3 herein. The 100 percent final electrical screening for off the shelf devices shall consist of the normal 100 percent DC tests at 25°C with 10 percent PDA, high and low temperature DC tests, and 25°C AC tests followed by normal sampling and LTPD's at group A lot acceptance.

3.6.2 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and 4.4 herein.

3.7 Manufacturer eligibility. To be eligible to supply microcircuits to this drawing, a manufacturer must have manufacturer certification in accordance with MIL-M-38510 for at least one line. Any suppliers not listed on 6.6 herein shall submit Group A variables data on 22 devices in accordance with 4.4.1. This data is to be submitted to DESC-EQE.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection to this device type shall not be required.

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).
   (1) Test condition D or E, each circuit must be driven with an appropriate signal to simulate circuit applications and each circuit shall have maximum load applied.
   (2) T_A = 125°C minimum.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Percent defective allowable (PDA) - The PDA is specified as 10 percent based on failures from group A, subgroup 1, test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for the lot.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Groups A and B inspections shall be performed on each lot. Quality assurance shall keep lot records for 3 years (minimum), monitor for compliance to the prescribed procedures, and observe that satisfactory manufacturing conditions and records on lots are maintained for these devices. The records, including as a minimum an attributes summary of all screening and quality conformance inspections conducted on each lot, shall be available for review by the customer at all times.

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in table I of method 5005 of MIL-STD-883 (class B) and as follows:

a. Tests shall be as specified in table II.
b. Subgroups 4, 5, 6, and 8 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. In group B inspection, each inspection lot shall be subjected to the test subgroups and LTPD values shown in table IIb of method 5005 of MIL-STD-883, class B.

4.4.3 Group C and group D inspection. Group C and group D inspections shall be as specified in method 5005 of MIL-STD-883, class B. The frequency of testing and the sample size shall be in accordance with MIL-M-38510. Generic test data (6.5) may be used to satisfy the requirements for group C and group D inspection.

a. End point electrical parameters shall be as specified in table II.
b. Operating life test (method 1005 of MIL-STD-883) conditions:
   (1) Test condition D or E, each circuit must be driven with an appropriate signal to simulate circuit applications and each circuit shall have maximum load applied.
   (2) T_A = 125°C, minimum.
   (3) Test duration: 1,000 hours.
c. Subgroups 3 and 4 shall be added to the group C inspection requirements and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.

4.5 Inspection of preparation for delivery. Inspection of preparation for delivery shall be in accordance with MIL-M-38510, except that the rough handling test shall not apply.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups
Interim electrical parameters (pre burn-in) (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9
Groups C and D end point electrical parameters (method 5005)	1, 2, 3
Additional electrical subgroups for group C periodic inspections	10, 11

* PDA applies to subgroup 1 (see 4.3c).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. Only 6.4 of the notes specified in MIL-M-38510 shall apply to this drawing.

6.2 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. This drawing is intended exclusively to prevent the proliferation of unnecessary duplicate specifications, drawings and stock catalog listings. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, this drawing becomes obsolete and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.3 Ordering data. The contract or order should specify the following:

a. Complete part number (see 1.2).
b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
c. Requirement for certificate of compliance, if applicable.
d. Requirements for notification of change of product or process to procuring activity, if applicable.
e. Requirements for packaging and packing.
f. Requirements for carrier, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct shipment to the Government.

6.4 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by contractor prepared specification or drawing.
b. When Military Specification MIL-M-38510/420 is issued, the part numbered devices specified in this drawing will be replaced by the microcircuit identified as part number M38510/42001B---.

6.5 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Generic test data is defined as test data from devices manufactured during the same time period, by means of the same production technique, materials, controls and design, and in the same microcircuit group (see 3.1.3(h) of MIL-M-38510) as the deliverable devices. The same time period shall be interpreted as covering a maximum span of 180 days between the generic test sample fabrication and the fabrication of deliverable devices. The vendor is required to retain generic data for a period of not less than 36 months from the date of shipment.

6.6 Suggested source(s) of supply. 2/

DESC DRAWING PART NUMBER	VENDOR FSCM NUMBER	SIMILAR 1/ VENDOR TYPE	REPLACEMENT MILITARY SPECIFICATION PART NUMBER
7700201QX	34335 34649 27014 01295	AM9080A MC8080A/B INS8080A TMS8080A	M38510/42001BQX

VENDOR FSCM NUMBER	VENDOR NAME AND ADDRESS
34335	Advanced Micro Devices, Inc. 901 Thompson Place Sunnyvale, CA 94086
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051
27014	National Semiconductor Corp. 2900 Semiconductor Drive Santa Clara, CA 95051
01295	Texas Instruments, Inc. P. O. Box 5012 Dallas, TX 75222

1/ CAUTION. DO NOT USE THIS NUMBER FOR ITEM PROCUREMENT. ITEMS PROCURED TO THE SIMILAR VENDOR TYPE ONLY MAY NOT SATISFY THE PERFORMANCE REQUIREMENTS OF THIS DRAWING.

2/ For additional suggested sources of supply or assistance in the use of this drawing, contact DESC-EC, 1507 Wilmington Pike, Dayton, Ohio 45444 or telephone 513 -296-5375.