REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Convert to SMD format. Editorial changes throughout. Redrawn.	92-11-18	M. L. POELKING
B	Add device type 02. Add cage 34371 as source of supply. Technical changes in 1.3 and 1.4 and table I. Boilerplate update. Editorial changes throughout.	93-11-19	M. L. POELKING

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

CURRENT CAGE CODE 67268

REV																		
SHEET																		
REV	B	B	B															
SHEET	14	15	16															

REV STATUS OF SHEETS	REV	B	B	B	A	A	A	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE 77-08-18

REVISION LEVEL B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, STROBED HEX INVERTER/BUFFER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	77020

SHEET 1 OF 16

DESC FORM 193-1
JUL 91

5962-E302-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	4502B	Strobed hex inverter/buffer
02	4502B	Strobed hex inverter/buffer

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	dual-in-line package
F	GDFP2-F16 or CDFP3-F16	16	flat package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specification when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range (V_{DD}) (01)	-0.5 V dc to +18 V dc
Supply voltage range (V_{DD}) (02)	-0.5 V dc to +20 V dc
(voltages referenced to V_{SS} terminal)	
Input voltage range	-0.5 V dc to V_{DD} + 0.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation, P_D	500 mW 1/
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}) (01)	+3.0 V dc minimum to +15 V dc maximum
Supply voltage range (V_{DD}) (02)	+3.0 V dc minimum to +18 V dc maximum
Minimum high level input voltage (V_{IH})	+3.5 V dc at V_{DD} = 5 V dc
Maximum low level input voltage (V_{IL})	+1.5 V dc at V_{DD} = 5 V dc
Case operating temperature range	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Intergrated circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing) (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching time waveforms. The switching time waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High-level output voltage	V_{OH}	V_{DD} = 5.0 V V_{DD} = 10 V V_{DD} = 15 V	V_{IN} = 0 V or V_{DD}	1,2,3	01	4.95 9.95 14.95		V
Low-level output voltage	V_{OL}	V_{DD} = 5.0 V V_{DD} = 10 V V_{DD} = 15 V	V_{IN} = V_{DD} or 0 V	1,2,3	01		0.05 0.05 0.05	V
Low-level input voltage	V_{IL} 1/	V_O = 4.5 V or 0.5 V	V_{DD} = 5.0 V	1,2,3	01		1.5	V
		V_O = 9.0 V or 1.0 V	V_{DD} = 10 V				3.0	
		V_O = 13.5 V or 1.5 V	V_{DD} = 15 V				4.0	
High-level input voltage	V_{IH} 1/	V_O = 4.5 V or 0.5 V	V_{DD} = 5.0 V	1,2,3	01	3.5		V
		V_O = 9.0 V or 1.0 V	V_{DD} = 10 V			7.0		
		V_O = 13.5 V or 1.5 V	V_{DD} = 15 V			11.0		
High-level output current	I_{OH}	V_O = 2.5 V	V_{DD} = 5.0 V	1,2,3	01	-0.7		mA
		V_O = 4.6 V	V_{DD} = 5.0 V			-0.14		
		V_O = 9.5 V	V_{DD} = 10 V			-0.35		
		V_O = 13.5 V	V_{DD} = 15 V			-1.1		
Low-level output current	I_{OL}	V_{OL} = 0.4 V	V_{DD} = 5.0 V	1,2,3	01	2.0		mA
		V_{OL} = 0.5 V	V_{DD} = 10 V			4.4		
		V_{OL} = 1.5 V	V_{DD} = 15 V			16		
Input current	I_{IN}	V_{DD} = 15 V		1,2,3	01		± 1.0	µA
Three-state leakage current	I_{TL}	V_{DD} = 15 V		1,2,3	01		± 3.0	µA
Input capacitance	C_{IN}	V_{IN} = 0 V	See 4.3.1b	4	01		7.5	pF
Quiescent current	I_{DD}	V_{DD} = 5.0 V V_{DD} = 10 V V_{DD} = 15 V		1,2,3	01		30 60 120	µA
Functional tests		See 4.3.1c		7,8	01			

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Propagation delay time, data to output	t_{PHL1}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	01		270 110 80	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			340 145 105	
Propagation delay time, data or inhibit to output	t_{PLH1}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	01		590 260 190	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			740 340 245	
Propagation delay time, inhibit to output	t_{PHL2}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	01		670 290 190	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			840 375 245	
Transition time	t_{THL}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	01		100 50 40	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			150 75 60	
	t_{TLH}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	01		200 100 80	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			300 150 120	
Propagation delay time, output high to high impedance	t_{PHZ}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	01		130 60 50	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			165 80 65	
Propagation delay time, high impedance to output high	t_{PZH}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	01		520 210 160	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			650 275 210	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Propagation delay time, output low to high impedance	t_{PLZ}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	01		300 140 110	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			375 180 145	
Propagation delay time, high impedance to output low	t_{PZL}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	01		320 130 100	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			400 170 130	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.-continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High-level output voltage	V_{OH}	V_{DD} = 5.0 V 2/ V_{DD} = 10 V 2/ V_{DD} = 15 V	V_{IN} = 0 V or V_{DD}	1,2,3	02	4.95 9.95 14.95		V
Low-level output voltage	V_{OL}	V_{DD} = 5.0 V 2/ V_{DD} = 10 V 2/ V_{DD} = 15 V	V_{IN} = V_{DD} or 0 V	1,2,3	02		0.05 0.05 0.05	V
Low-level input voltage	V_{IL} 1/	V_O = 4.5 V or 0.5 V	V_{DD} = 5.0 V	1,2,3	02		1.5	V
		V_O = 9.0 V or 1.0 V	V_{DD} = 10 V				3.0	
		V_O = 13.5 V or 1.5 V	V_{DD} = 15 V				4.0	
High-level input voltage	V_{IH} 1/	V_O = 4.5 V or 0.5 V	V_{DD} = 5.0 V	1,2,3	02	3.5		V
		V_O = 9.0 V or 1.0 V	V_{DD} = 10 V			7.0		
		V_O = 13.5 V or 1.5 V	V_{DD} = 15 V			11.0		
High-level output current 4/	I_{OH}	V_O = 2.5 V	V_{DD} = 5.0 V	1,2,3	02	-1.15		mA
		V_O = 4.6 V	V_{DD} = 5.0 V			-0.36		
		V_O = 9.5 V	V_{DD} = 10 V			-0.9		
		V_O = 13.5 V	V_{DD} = 15 V			-2.4		
Low-level output current 4/	I_{OL}	V_{OL} = 0.4 V	V_{DD} = 5.0 V	1,2,3	02	2.16		mA
		V_{OL} = 0.5 V	V_{DD} = 10 V			5.4		
		V_{OL} = 1.5 V	V_{DD} = 15 V			14.4		
Input current	I_{IN}	V_{DD} = 20 V 5/		1,2,3	02		± 1.0	µA
Three-state leakage current	I_{TL}	V_{DD} = 20 V 5/		1,2,3	02		± 12.0	µA
Input capacitance	C_{IN}	V_{IN} = 0 V	See 4.3.1b	4	02		7.5	pF
Quiescent current	I_{DD}	V_{DD} = 5.0 V 2/ V_{DD} = 10 V 2/ V_{DD} = 15 V 2/ V_{DD} = 20 V 5/		1,2,3	02		30 60 120 600	µA
Functional tests		See 4.3.1c		7,8	02			

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, data or inhibit to output	t_{PHL1}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	02		270 120 80	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			340 150 105	
Propagation delay time, data or inhibit to output	t_{PLH1}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	02		380 180 130	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			570 270 195	
Transition time	t_{THL}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	02		120 60 40	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			180 90 60	
	t_{TLH}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	02		200 100 80	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 200 kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			300 150 120	
Propagation delay time, output high to high impedance	t_{PHZ}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 1kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	02		120 80 60	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 1kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			180 120 90	
Propagation delay time, high impedance to output high	t_{PZH}	C_L = 50 pF Min V_{DD} = 5.0 V R_L = 1kΩ 2/ V_{DD} = 10 V 3/ 2/ V_{DD} = 15 V	9	02		220 100 80	ns
		C_L = 50 pF Min V_{DD} = 5.0 V R_L = 1kΩ V_{DD} = 10 V 2/ 3/ V_{DD} = 15 V	10,11			330 150 120	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Propagation delay time, output low to high impedance	t_{PLZ}	C_L = 50 pF Min, R_L = 1kΩ, 3/		02			ns
		V_{DD} = 5.0 V	9			250	
		2/ V_{DD} = 10 V	9			130	
		2/ V_{DD} = 15 V	9			110	
		C_L = 50 pF Min, R_L = 1kΩ, 2/ 3/					
		V_{DD} = 5.0 V	10,11			375	
		V_{DD} = 10 V	10,11			195	
		V_{DD} = 15 V	10,11			165	
Propagation delay time, high impedance to output low	t_{PZL}	C_L = 50 pF Min, R_L = 1kΩ, 3/		02			ns
		V_{DD} = 5.0 V	9			250	
		2/ V_{DD} = 10 V	9			110	
		2/ V_{DD} = 15 V	9			80	
		C_L = 50 pF Min, R_L = 1kΩ, 2/ 3/					
		V_{DD} = 5.0 V	10,11			375	
		V_{DD} = 10 V	10,11			165	
		V_{DD} = 15 V	10,11			120	

1/ V_{IH} and V_{IL} tests are not required if applied as forcing functions for the V_{OH} and V_{OL} tests.

2/ This condition is guaranteed, if not tested, to the specification limits in table I.

3/ See figure 4 for switching time waveforms.

4/ Subgroups 2 and 3 may be guaranteed, if not tested, to the specification limits in table I.

5/ At -55°C test is performed with V_{DD} = 18 V.

Device type	All
Case outline	E and F
Terminal number	Terminal symbol
1	D3
2	Q3
3	D1
4	DIS
5	Q1
6	D2
7	Q2
8	V_{SS}
9	Q4
10	D4
11	Q5
12	INH
13	D5
14	Q6
15	D6
16	V_{DD}

FIGURE 1. Terminal connections.

Dn	INHIBIT	DISABLE	Qn
L	L	L	H
H	L	L	L
X	H	L	L
X	X	H	Z

H = logic high voltage level
L = logic low voltage level
X = irrelevant
Z = high impedance state

FIGURE 2. Truth table.

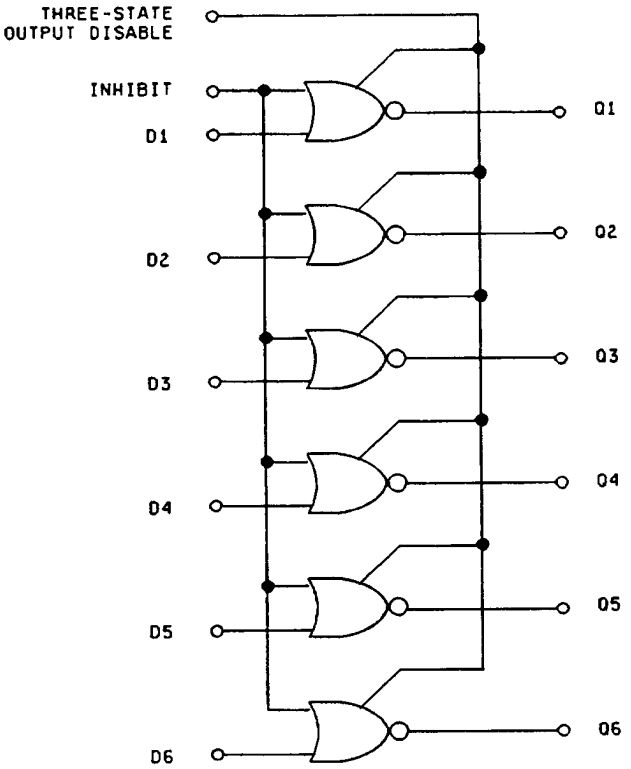
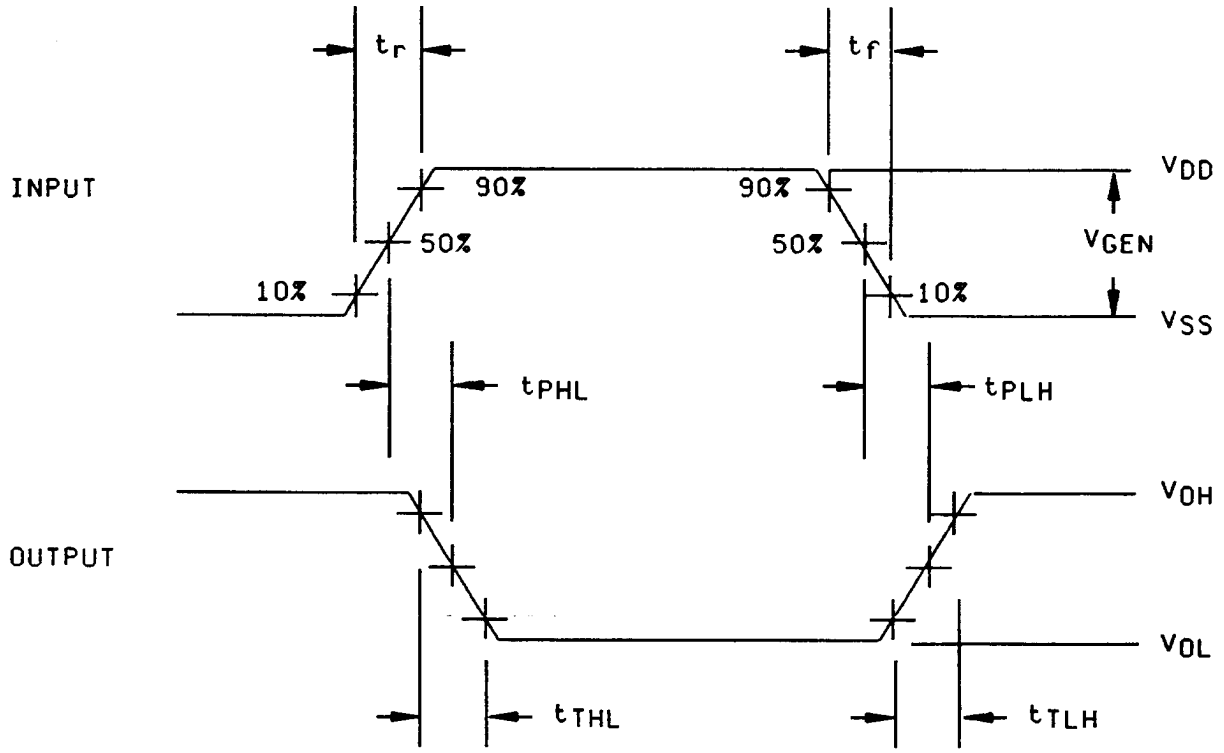


FIGURE 3. Logic diagram.



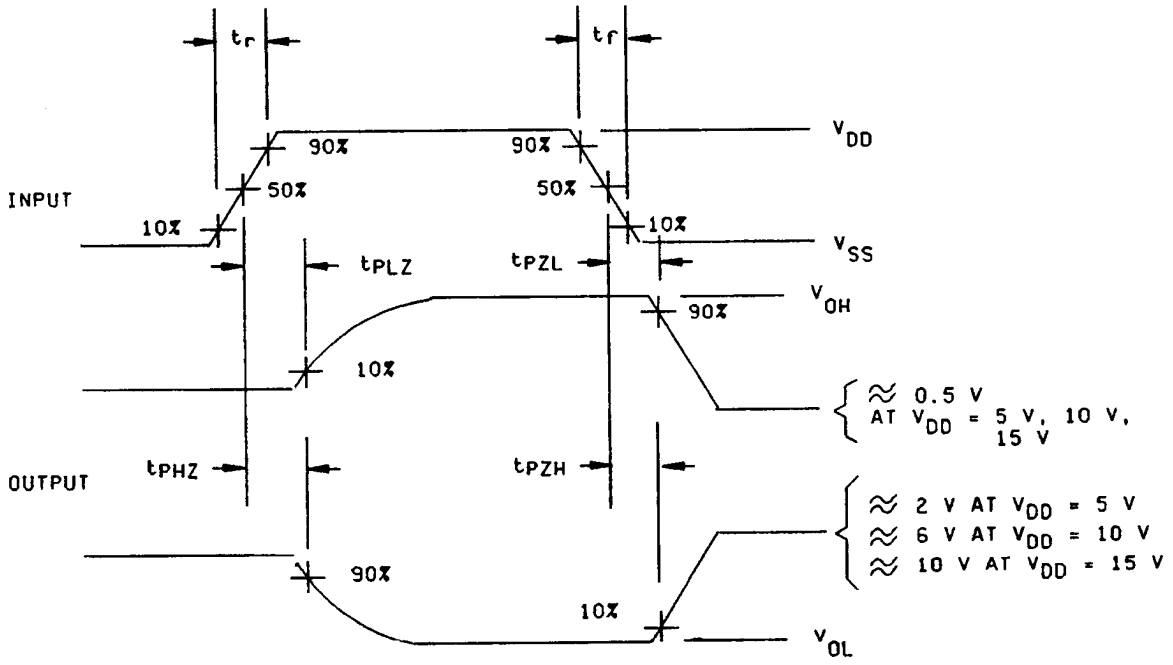
DYNAMIC TEST WAVEFORMS-01

Input pulse
$V_{GEN} = V_{DD} \pm 1.0\%$
$t_{PH} = 1.0 \pm 0.1$ µs
$t_r = t_f = 20 \pm 2$ ns
PRR = 200 kHz

DYNAMIC TEST WAVEFORMS-02

Input pulse
$V_{GEN} = V_{DD}$
$t_r = t_f = 20$ ns
PRR = 200 kHZ

FIGURE 4. Switching time waveforms.



DYNAMIC TEST WAVEFORMS-01

Input pulse
$V_{GEN} = V_{DD} \pm 1.0\%$
$t_{PH} = 1.0 \pm 0.1$ µs
$t_r = t_f = 20 \pm 2$ ns
PRR = 200 kHz

DYNAMIC TEST WAVEFORMS-02

Input pulse
$V_{GEN} = V_{DD}$
$t_r = t_f = 20$ ns
PRR = 200 kHZ

FIGURE 4. Switching time waveforms - Continued.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	----
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. Test all applicable pins on 5 devices with zero failures.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistic purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.