LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVE
F	Change to military drawing format. Add device type 03. Device 01, case E, inactive for new design. Table I (device 01) change test condition for $I_{\rm IL}$ . Table I (device 02): Delete test $R_{\rm DS2}$ and $V_{\rm CT}$ ; add test $\Delta R_{\rm DS1}$ ; change test conditions and limits for: $R_{\rm DS1}$ , $C_{\rm IS}$ ,	87-01-30	M.A. Frye
G	Add case outline 2. Electrical changes in table I, 1.3, and 1.4. Editorial changes throughout. Change vendor CAGE 34371 vendor PINs and add vendor CAGE 24355. Delete vendor CAGE 32293 and add vendor CAGE 1ES66.	94-03-24	M.A. Frye

The original first page of this drawing has been replaced.

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PMIC N/A PREPARED BY Donald R. Osborne				DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444															
****					CHECKED BY D.A. DiCenzo				MICROCIRCUIT, CMOS, POSITIVE LOGIC								GIC		
DRAWING  THIS DRAWING IS AVAILABLE				APPROVED BY N.A. Hauck				8-CHANNEL ANALOG MULTIPLEXERS,											
FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DRAWING APPRI DEPARTMENT OF DEFENSE 77-10-26			PROVA	L DATE			MONOLITHIC SILICON												
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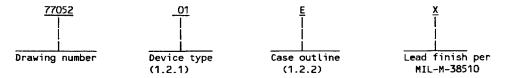
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9004708 0000755 T95 **=** 

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-SID-883, "Provisions for the use of MIL-SID-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	<u>Circuit function</u>
01	DG508A, HI-508, ADG508A	CMOS, positive logic, 8-channel analog MUX/DENUX
02	HI-508A, HI-548	CMOS, positive logic, 8-channel analog MUX/DEMUX with overvoltage protection
03	MAX358	CMOS, positive logic, 8-channel analog MUX/DEMUX with overvoltage protection

1.2.2 <u>Case outline(s)</u>. The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	cqcc1-N2O	20	Square leadless chip carrier

1.2.3 <u>Lead finish</u>. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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    1.3 Absolute maximum ratings.

    Supply voltage between V+ and V-:
      Device type 01 - - - - - - - - +44 V dc
      Device types 02 and 03 - - - - - - - +40 V dc
    V+ to ground:
      Device type 01 - - - - - - - - - +22 V dc
      Device types 02 and 03 - - - - - - - - +20 V dc
    V- to ground:
      Device types 02 and 03 - - - - - - - - - - - - - - - - 20 V dc
    Digital input overvoltage range
      Device types 02 and 0\overline{3} - - - - - - - - - (V-) - 4.0 V dc to (V+) + 4.0 V dc
    Analog input overvoltage range
                                       ---- (V-) - 3.0 V dc to (V+)
      Device type 01 - - - - -
    Analog input voltage (V<sub>S</sub>):

Device type 01 - - - - - - - - - - - (V-) - 2 V dc to (V+) + 2 V dc
      Device types 02 and 03 - - - - - - - - (V-) - 20 V dc to (V+) + 20 V dc
    Storage temperature range - - - - - - - - - - - - - - - - - -65°C to +150°C
    Power dissipation (PD):
      Case E - - - - 470 mW at T<sub>A</sub> = +75°C
      Case F - - - - - 725 mW at T_A^A = +75°C Case 2 - - - - - - - 1.23 W at T_A^A = +75°C
    Derating factor:
      Case E - - - - - - - - - - - - - - 12.0 mW/°C above T_A = +75^{\circ}C Case F - - - - - - - - 8.0 mW/°C above T_A = +25^{\circ}C Case 2 - - - - - - - - - - - - - 12.3 mW/°C above T_A = +75^{\circ}C
    Thermal resistance, junction-to-case (\theta_{JC}) - - - - See MIL-STD-1835 Lead temperature (soldering, 10 seconds) - - - - - +300°C
     Junction temperature (T<sub>J</sub>)
 1.4 Recommended operating conditions.
      Positive supply voltage (V+) - - - - - - - - - +15 V dc
     Logic low level address input voltage (V_{\rm IL})- - - - 0 V dc to 0.8 V dc Logic high level address input voltage (V_{\rm IH}):

Device types 01 and 03 - - - - - - - - 2.4 V dc to (V+) -
                                                   _ - - - - 2.4 V dc to (V+) - 0.7 V dc
        Device type 02 - - - - - - - - - - - - 4.0 V dc to V+
      Enable voltage (V<sub>EN</sub>):
        Device type 01 \frac{e^{N}}{1} - - - - - - - - - - - - 4.5 V dc to (V+) - 0.7 V dc Device type 02 - - - - - - - - - - - - - 4.0 V dc to (V+) - 0.7 V dc
        Device type 03 - - - - - - - - - - 2.4 V dc to (V+) - 0.7 V dc
      Ambient operating temperature range (T_A) - - - - - -55°C to +125°C
 2. APPLICABLE DOCUMENTS
 2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification,
standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and
Standards specified in the solicitation, form a part of this drawing to the extent specified herein.
  SPECIFICATION
    MILITARY
        MIL-M-38510

    Microcircuits, General Specification for.

  STANDARDS
     MILITARY
                         - Test Methods and Procedures for Microelectronics.
        MIL-STD-883

    Microcircuit Case Outlines.

        MIL-STD-1835
                                                                                                               77052
                     STANDARDIZED
                                                                   SIZE
                 MILITARY DRAWING
                                                                    A
     DEFENSE ELECTRONICS SUPPLY CENTER
                DAYTON, OHIO 45444
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BULLETIN

Mail ITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

#### REQUIREMENTS

- 3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.
  - 3.2.1 <u>Case outline(s)</u>. The case outline(s) shall be in accordance with 1.2.2 herein.
  - 3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 1.
  - 3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.
- 3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.
- 3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).
- 3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.
- 3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.
- 3.8 <u>Notification of change</u>. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).
- 3.9 <u>Verification and review</u>. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
  - 4. QUALITY ASSURANCE PROVISIONS
- 4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

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TABLE I.	Electrical performance characteristics.
	(Device type O1)

Test	   Symbol	Conditions $1/\sqrt{V_{en}} = -15 \text{ V}, \text{ V} = +15 \text{ V}, \text{ V}_{en} = 4.5 \text{ V}$	Group A	Lin	Unit		
		-55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	subgroups	Min	Max		
Irout Leak <b>age</b> current <u>2</u> /	IH	Measure address inputs sequentially,   connect all unused address inputs   to 5.0 V	1, 2		+0.8	μΑ	
	IIL	Measure address inputs sequentially,   connect all unused address inputs   to 5.0 V			-0.8		
Leakage current into the source terminal of an "OFF"	<sup>+I</sup> s(off)	V <sub>S</sub> = +10 V, V <sub>EN</sub> = 0.8 V All unused inputs = -10 V	1, 2, 3	-50	+50	пA	
switch	-Is(off)	V <sub>S</sub> = -10 V, V <sub>EN</sub> = 0.8 V All unused sources = +10 V					
Leakage current into the drain terminal	<sup>+I</sup> D(OFF)	V <sub>D</sub> = 10 V, V <sub>EN</sub> = 0.8 V All unused inputs = -10 V	1, 2, 3	-250	  +250 	n <b>A</b>	
of an "OFF" switch	-I <sub>D</sub> (OFF)	V <sub>D</sub> = -10 V, V <sub>EN</sub> = 0.8 V All unused inputs = +10 V					
Leakage current from an "ON" driver	+I <sub>D</sub> (ON)	v <sub>p</sub> = 10 V, V <sub>S</sub> = -10 V All unused inputs = -10 V	1, 2, 3	-250	+250	nA	
into the switch (drain)	-ID(ON)	V <sub>D</sub> = -10 V, V <sub>S</sub> = 10 V All unused inputs = +10 V		<u> </u>		-	
Positive supply current	I(+)	V <sub>A</sub> = 0 V, V <sub>EN</sub> = 5 V	1, 2, 3		12	mA	
Negative supply current	I(-)	v <sub>A</sub> = 0 v, v <sub>EN</sub> = 5 v	1, 2, 3	-12			
Standby positive supply current	<sup>+I</sup> SBY	V <sub>A</sub> = 0 V, V <sub>EN</sub> = 0 V	1, 2, 3		3.5	mA	
Standby negative supply current	-I <sub>SBY</sub>	v <sub>A</sub> = 0 v, v <sub>EN</sub> = 0 v		-3.5		mA	
Switch "ON" resistance	R <sub>DS1</sub>	V <sub>S</sub> = +10 V I <sub>D</sub> = +1 mA	1, 3	1	400	Ω	
			2		500	_	
		$V_S = -10 V$ $I_D = -1 mA$	1, 3	   	400	  -	
			2		500		

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TABLE I		Electrical	performance	characteristics	-	Continued.		
(Device type 01)								

	<del></del>	Conditions 1/		<u> </u>		T II-iA
Test	Symbol 	$(V- = -15 \text{ V}, V+ = +15 \text{ V}, V_{EN} = 4.5 \text{ V})$ -55°C \le T_A \le +125°C	Group A subgroups	<u>Lin</u>	mits	_  Unit 
Switch "ON" resistance	R <sub>DS2</sub>	unless otherwise specified  V+ = +10 V, V- = -10 V, V <sub>S</sub> = +7.5 V  I <sub>D</sub> = -1 mA	1, 2, 3	Min	Max    1000	Ω
		V+ = +10 V, V- = +10 V, V <sub>S</sub> = -7.5 V I <sub>D</sub> = -1 mA			1000	-    
Capacitance: Address	c <sub>A</sub>	V+ = V- = 0 V <u>3</u> / f = 1 MHz T <sub>A</sub> = +25°C	4		10	pF
Capacitance: Output switch	c <sub>os</sub>	V+ = V- = 0 V <u>3</u> / f = 1 MHz T <sub>A</sub> = +25°C	4		45 	pF
Capacitance: Input switch	c <sub>IS</sub>	V+ = V- = 0 V <u>3</u> / f = 1 MHz T <sub>A</sub> = +25°C	4		10	pF
Charge transfer error	V <sub>СТЕ</sub>	V <sub>S</sub> = GND 3/ V <sub>GEN</sub> = 0 V to 5 V, f = 500 kHz T <sub>A</sub> = +25°C, C <sub>L</sub> = 100 pF	4		10	mV
Single channel isolation	v <sub>ISO</sub>	V <sub>GEN</sub> = 1 V <sub>p-p</sub> , f = 200 kHz <u>3</u> / T <sub>A</sub> = +25°c	4	50		dB
Crosstalk between channels	V <sub>CT</sub>	V <sub>GEN</sub> = 1 V <sub>p-p</sub> , f = 200 kHz <u>3</u> /  T <sub>A</sub> = +25°C		50		
Break-before- make time delay	t <sub>D</sub>	T <sub>A</sub> = +25°C  See figure 3	9	5		ns
Propagation delay times:	t <sub>ON(A)</sub>	  R <sub>L</sub> = 1kΩ, c <sub>L</sub> = 100pF  See figures 4 and 5	9, 11		1000	   ns
Address inputs to I/O channels	<sup>t</sup> OFF(A)	Joee Trigules 4 and 5	10		1500	_
Enable to I/O	t <sub>ON(EN)</sub>	$R_L = 1 k\Omega$ , $C_L = 100 pF$ See figures 4 and 5	9, 11		1000	ļ
	<sup>t</sup> off(EN)		10		1500	

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TABLE	I.	Electrical	performance	characteristics	_	Continued.
			(Device ty	pe 02)		

Test	Symbol	Conditions $\frac{1}{2}$ $(V = -15 \text{ V}, V = +15 \text{ V}, V_{EN} = 4.0 \text{ V})$	Group A	Limits		Unit
		-55°C ≤ T <sub>A</sub> ≤ +125 <sup>U</sup> C unless otherwise specified	subgroups	   Min	Max	
Positive input clamping voltage	V <sub>IC(POS)</sub>	I <sub>IN</sub> = 1 mA, V+ = V- = 0 V <u>3</u> / T <sub>A</sub> = +25°C	1		+1.5	V
Negative input clamping voltage	V <sub>IC(NEG)</sub>	I IN = -1 mA, V+ = V- = 0 V 3/   TA = +25°C	1	   -1.5 	   	V   
Input leakage current <u>2</u> /	IIH	Measure inputs sequentially, connect all unused inputs to GND	1, 2	-1.0	+1.0	μΑ
	IIL	Measure inputs sequentially, connect all unused inputs to GND	1, 2	+1.0	-1.0	
Leakage current into the source terminal of an "OFF" switch	+Is(off)	V <sub>S</sub> = 10 V, V <sub>EN</sub> = 0.8 V, V <sub>D</sub> = -10 V All unused inputs = -10 V	1, 2	-50	+50	nA
	-Is(off)	V <sub>S</sub> = -10 V, V <sub>EN</sub> = 0.8 V, V <sub>D</sub> = +10 V   All unused inputs = +10 V	 			
Leakage current into the drain terminal of an	<sup>+I</sup> D(OFF)	V <sub>D</sub> = +10 V, V <sub>EN</sub> = 0.8 V All unused inputs = -10 V	1, 2	-250	+250	nA
"OFF" switch	-I <sub>D</sub> (OFF)	  V <sub>D</sub> = -10 V, V <sub>EN</sub> = 0.8 V  All unused inputs = +10 V				
Leakage current from an "ON" driver the	+I <sub>D</sub> (ON)	V <sub>S</sub> = +10 V, V <sub>D</sub> = +10 V   All unused inputs = -10 V	1, 2, 3	-250	+250	nA
switch (drain)	-ID(ON)	V <sub>S</sub> = - 10 V, V <sub>D</sub> = - 10 V All unused inputs = +10 V				
Overvoltage protected, leakage current	+ID(OFF) over- voltage	v <sub>S</sub> = 33 v, v <sub>D</sub> = 0 v, v <sub>EN</sub> = 0.8 v	1, 2, 3	-2.0	+2.0	μΑ
into the drain terminal of an "OFF" switch	-ID(OFF) over- voltage	$v_S = -33 \text{ v, } v_D = 0 \text{ v, } v_{EN} = 0.8 \text{ v}$				

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TABLE I.	Electrical	performance	characteristics	-	Continued.	
(Device type 02)						

īest	Conditions $\frac{1}{2}$   Symbol   $(V- = -15 \text{ V}, V+ = +15 \text{ V}, V_{EN} = 4.0 \text{ V})$		Group A	Limits		Unit
		(V- = -15 V, V+ = +15 V, V <sub>EN</sub> = 4.0 V) -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	subgroups	Min	Max	<u> </u>
Positive supply current	I(+)	v <sub>A</sub> = 0 v, v <sub>EN</sub> = 4 v	1, 2, 3		+2.0	mA
degative supply	1(-)	v <sub>A</sub> = 0 v, v <sub>EN</sub> = 4 v	1, 2, 3	-1.0		mA
Standby positive supply current	+I <sub>SBY</sub>	v <sub>A</sub> = 0 v, v <sub>EN</sub> = 0 v	1, 2, 3		+2.0	mA
Standby negative supply current	-I <sub>SBY</sub>	v <sub>A</sub> = 0 v, v <sub>EN</sub> = 0 v	1, 2, 3	-1.0		mA
Switch "ON" resistance	+R <sub>DS1</sub>	$ V_{S}  = +10 V$ $ I_{D}  = -100 \mu A$	1		1500	   Ω -
			2, 3		1800	
	-R <sub>DS1</sub>	  V <sub>S</sub> = -10 V  I <sub>D</sub> = -100 μA	1		1500	Ω
		٠ ،	2, 3		1800	
Difference in switch "ON" resistance	+∆R <sub>DS1</sub>	(+R <sub>DS1</sub> max) - (+R <sub>DS1</sub> min) X 100/+R <sub>DS1</sub> AVE, T <sub>A</sub> = +25°c	1		7	%
between channels	-∆R <sub>DS1</sub>	(-R <sub>DS1</sub> max) - (-R <sub>DS1</sub> min) x 100/-R <sub>DS1</sub> AVE, T <sub>A</sub> = +25°c	1		7	
Capacitance: Address	C <sub>A</sub>	V+ = V- = 0 V	4		10	pF
Capacitance: Output switch	cos				45	

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER	SIZE A		77052
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	I.A.	BLE I. Electrical performance characters (Device type 02)	31103			
Test	Conditions $\frac{1}{2}$   Symbol   $(V - = -15 \text{ V}, V + = +15 \text{ V}, V_{FN} = 4.0 \text{ V})$		Group A	Limits		Unit
		-55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	subgroups	Min	Max	
Capacitance: Input switch	c <sub>IS</sub>		_	     	15	pF
Charge transfer error	V <sub>CTE</sub>	V <sub>S</sub> = GND,   V <sub>GEN</sub> = 0 V to 5 V, T <sub>A</sub> = +25°C			10	mV
Off isolation	VISO	V <sub>GEN</sub> = 0.8 V <sub>p-p'</sub> f = 100 kHz <u>3</u> /  T <sub>A</sub> = +25°C, V <sub>S</sub> = 7 V rms  R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 15 pF	4	50		dB
Break-before- make time delay	t <sub>D</sub>	$T_A = +25$ °C, See figure 3 $3/$ $R_L = 1 kΩ$ , $C_L = 12.5 pF$	9	5		ns
Propagation delay times:	t <sub>ON(A)</sub>	$R_{L} = 10 \text{ M}\Omega$ $3/$ $C_{L} = 14 \text{ pF}$	9		500	-  -
Address inputs to I/O channels	t <sub>OFF(A)</sub>	See figures 4 and 5	10, 11		1000	_
Enable to I/O	<sup>t</sup> on(EN)	$ R_L = 1 k\Omega \qquad 3/$ $ C_L = 12.5 pF$	9	ļ 	500	_
	toff(EN)	See figures 4   and 5	10, 11		1000	

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**9004708 0000763 06%** 

TABLE I.	Electrical performance characteristics - Continued.					
(Device type 03)						

Test	Symbol	Conditions $\frac{1}{1}$ $ (V-=-15 \text{ V}, V+=+15 \text{ V}, V_{FN}=2.4 \text{ V})$	Group A	Limits		Unit	
		-55°C ≤ T <sub>A</sub> ≤ +12 <sup>50</sup> C unless otherwise specified	subgroups	Min	Max		
Input Leakage	IIH	Measure inputs sequentially, connect	11	-1.0	1.0	<u> </u> µа	
current <u>2</u> /	ļ	all unused inputs to ground	2	<u> </u>	10		
	IIL		1	-1.0	1.0	μΑ	
	ļ		2		10		
Leakage current into the source terminal of an "OFF" switch	I <sub>S(OFF)</sub>	V <sub>S</sub> = 10 V, V <sub>EN</sub> = 0.8 V, All unused inputs = -10 V, V <sub>D</sub> = -10 V	1, 2 -	-50	50	nA	
"Uff" switch		V <sub>S</sub> = -10 V, V <sub>EN</sub> = 0.8 V, All unused inputs = +10 V, V <sub>D</sub> = +10 V					
Leakage current into the drain terminal of an "OFF" switch	I <sub>D</sub> (OFF)	V <sub>D</sub> = +10 V, V <sub>EN</sub> = 0.8 V, All unused inputs = -10 V	1, 2	-250	250	nA	
	-I <sub>D</sub> (OFF)	V <sub>D</sub> = -10 V, V <sub>EN</sub> = 0.8 V,  All unused inputs = +10 V		j			
Leakage current from an "ON" driver into the	ID(ON)	V <sub>S</sub> = +10 V, V <sub>D</sub> = +10 V, All unused inputs = -10 V	1, 2, 3	  -250 	250	nA	
switch (drain)		V <sub>S</sub> = -10 V, V <sub>D</sub> = -10 V, All unused inputs = +10 V					
Overvoltage protected,	ID(OFF)	$v_S = +25 \text{ v}, v_D = 0 \text{ v}, v_{EN} = 0.8 \text{ v}$	1, 3	-2.0	2.0	μA	
leakage current into the drain terminal of an	voltage)		2	-5.0	5.0		
"OFF" switch		v <sub>S</sub> = -25 v, v <sub>D</sub> = 0 v, v <sub>EN</sub> = 0.8 v	1, 3	-2.0	2.0		
			2	-5.0	5.0		
Positive supply current	I(+)	V <sub>A</sub> = 5.0 V	1, 2, 3		2.0	mA	

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TABLE I.	Electrical	performance	characteristics	-	Continued.
		(Device ty			

Test	Symbol	Conditions $\frac{1}{1}$ $(V- = -15 \text{ V}, V+ = +15 \text{ V}, V_{EN} = 2.4 \text{ V})$	Group A	Lim	mits	_ Unit
		-55°C ≤ T <sub>A</sub> ≤ +125 <sup>9</sup> C unless otherwise specified	subgroups	Min	Max	1
(egative supply current	I(-)	v <sub>A</sub> = 5.0 v	1, 2, 3		-1.4	mA
Standby positive supply current	<sup>+I</sup> SBY	V <sub>A</sub> = 0 V, V <sub>EN</sub> = 0.8 V	1, 2, 3	<u> </u>	2.0	mA
Standby negative supply current	-I <sub>SBY</sub>	v <sub>A</sub> = 0 v, v <sub>EN</sub> = 0.8 v	1, 2, 3	1	-1.0	mA
Switch "ON" resistance	R <sub>DS1</sub>	$ V_S  = +10 V,$ $ I_D  = 100 \mu A$	1, 3		1500	Ω
			2		1800	
		V <sub>S</sub> = -10 V   I <sub>D</sub> = -100 \( \mu \text{A} \)	1, 3		1500	Ω
			2		1800	
Switch "ON" resistance	R <sub>DS2</sub>	$V+ = +10 \text{ V}, V- = -10 \text{ V}, V_S = +5 \text{ V},$ $I_D = 100 \mu\text{A}$	1, 2, 3		2200	Ω
		$V+ = +10 \text{ V}, V- = -10 \text{ V}, V_S = -5 \text{ V},$ $I_D = -100 \mu\text{A}$		1		
Capacitance: Address	C <sub>A</sub>	V+ = V- = 0 V, 3/ f = 1 MHz, T <sub>A</sub> = +25°C	4		10	pF
Capacitance: Output switch	Cos	V+ = V- = 0 V, 3/ If = 1 MHz, T <sub>A</sub> = +25°C			45	
Capacitance: Input switch	c <sub>IS</sub>	V+ = V- = 0 V, 3/ f = 1 MHz, T <sub>A</sub> = +25°C	4		10	pF
Charge transfer error	V <sub>CTE</sub>	V <sub>S</sub> = GND, V <sub>GEN</sub> = 0 V to 5 V, T <sub>A</sub> = +25°C	4		10	mV

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TABLE I.	Electrical performance characteristics	_	Continued.
	(Device type 03)		

Test	Symbol	Conditions $\frac{1}{2}$ $(V = -15 V, V = +15 V, V_{EN} = 2.4 V)$	Group A	Lin	nits	_  Unit
		$(V- = -15 \text{ V, } V+ = +15 \text{ V, } V_{-}^{-} = 2.4 \text{ V})$ -55°C $\leq T_{A} \leq +125^{\circ}C$ unless otherwise specified	subgroups	Min	Max	<u> </u>
Single channel isolation	V <sub>ISO</sub>	V <sub>GEN</sub> = 1 V <sub>P-p</sub> , f = 200 kHz, 3/ T <sub>A</sub> = +25°C	4	50		dB
Crosstalk between channels	v <sub>cτ</sub>	V <sub>GEN</sub> = 1 V <sub>p-p</sub> , f = 200 kHz, <u>3</u> / T <sub>A</sub> = +25°C		50		
Break-befo <b>re</b> - make time delay	t <sub>D</sub>	T <sub>A</sub> = +25°C <u>3</u> / See figure 3	9	5		ns
Propagation delay times:	<sup>t</sup> ON(A)	$R_{L} = 10 \text{ k}\Omega, \qquad \underline{3}/$ $C_{L} = 100 \text{ pF},$	9	<u> </u> 	1000	ns -
Address inputs to I/O channels	toff(A)	See figures 4 and 5	10, 11		1500	_
Enable to I/O	ton(EN)	$\begin{vmatrix} R_L = 1 & k\Omega, & \underline{3}/\\ C_L = 100 & pF, & \underline{3}/2 \end{vmatrix}$	9	<u> </u>	1000	_
	t <sub>OFF(EN)</sub>	See figures 4	10, 11	   	1500	

 $<sup>\</sup>frac{1}{2}$ / Unless otherwise specified, V+ = +15 V and V- = -15 V.  $\frac{1}{2}$ / Input current of one input node.  $\frac{1}{2}$ / Guaranteed, if not tested, to the limits specified.

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Case outline	E	F	2			
Device type	01,02,03,04	01,04	01,02,03			
Terminal number	Terminal symbol					
1 2 3 4 5 6 7 8 9 10 11 12	AO ENABLE V- IN 1 IN 2 IN 3 IN 4 OUT IN 8 IN 7 IN 6 IN 5	AO ENABLE V- IN 1 IN 2 IN 3 IN 4 OUT IN 8 IN 7 IN 6 IN 5	NC AD ENABLE V- IN 1 NC IN 2 IN 3 IN 4 OUT NC IN 8			
13 14 15 16 17 18 19 20	V+ GND A2 A1	V+ GND A2 A1  	IN 7 IN 6 IN 5 NC V+ GND A2			

FIGURE 1. Terminal connections.

## Device types 01, 02, and 03

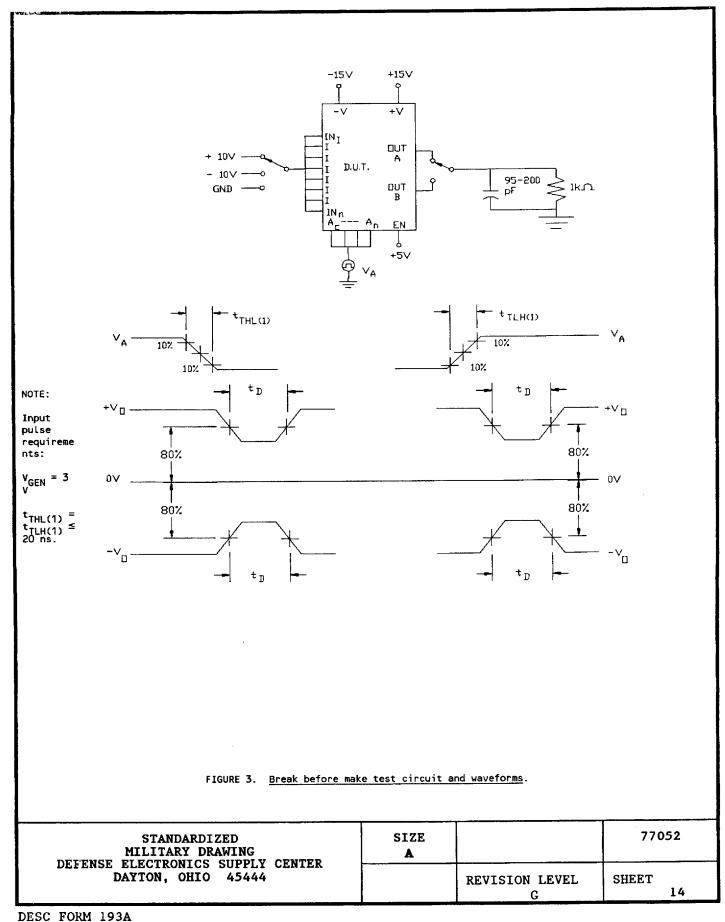
A2	A1	AO	EN	Channel selected
Х	Х	Х	L	None
L	L	L	Н	1
L	L	н	Н	2
L	Н	L	Н	3 4
L	н	н	Н	4
Н	L	Ĺ	н	5
н	Ĺ	н	н	6
н	ĺН	Ĺ	н	7
Н	н	Н	Н	8

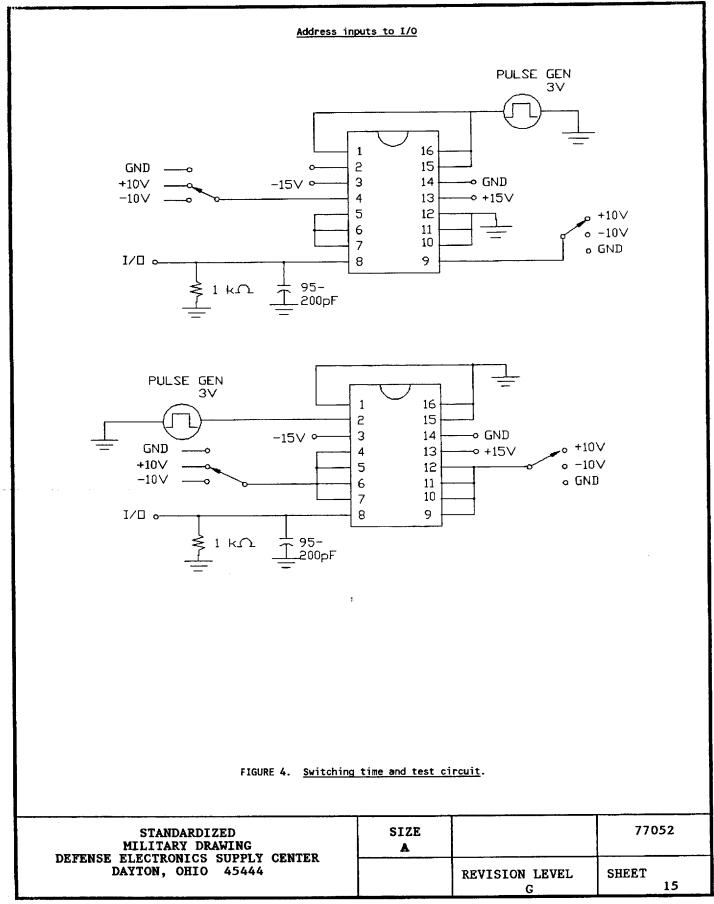
FIGURE 2. Truth table.

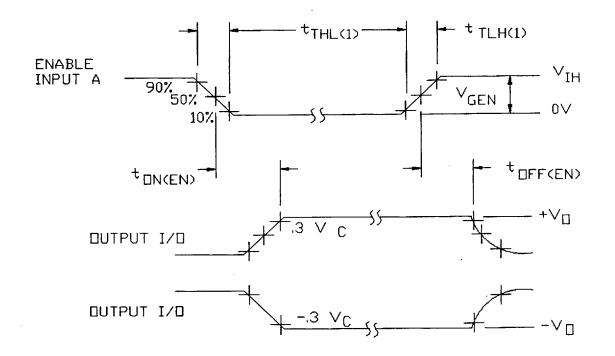
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# **9004708 0000767 707**







NOTE:

Input pulse requirements:

 $V_{GEN} = 3 V$   $t_{THL(1)} = t_{TLH(1)} \le 20 \text{ ns.}$ 

FIGURE 5. Switching time and waveforms.

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## 9004708 0000770 2T1 **=**

- 4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:
  - a. Burn-in test, method 1015 of MIL-STD-883.
    - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
    - (2)  $T_A = +125$ °C, minimum.
  - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- 4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

#### 4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (capacitance measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

### 4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883:
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
  - (2)  $T_A = +125$ °C, minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. <u>Electrical test requirements</u>.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1

<sup>\*</sup> PDA applies to subgroup 1.

<sup>\*\*</sup> Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

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- PACKAGING
- 5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).
  - 6. NOTES
- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.
  - 6.2 Replaceability. Replaceability is determined as follows:
    - a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
    - b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the wicrocircuit identified as part number M38510/1900XB\*X.
- 6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.
- 6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.
- 6.5 <u>Comments</u>. Comments on this drawing should be directed to DESC-EC, Dayton, OH 45444, or telephone (513) 296-5377.
- 6.6 <u>Approved sources of supply</u>. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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