T-52-33-17

OAK TECHNOLOGY, INC.

VCEP

May 1992

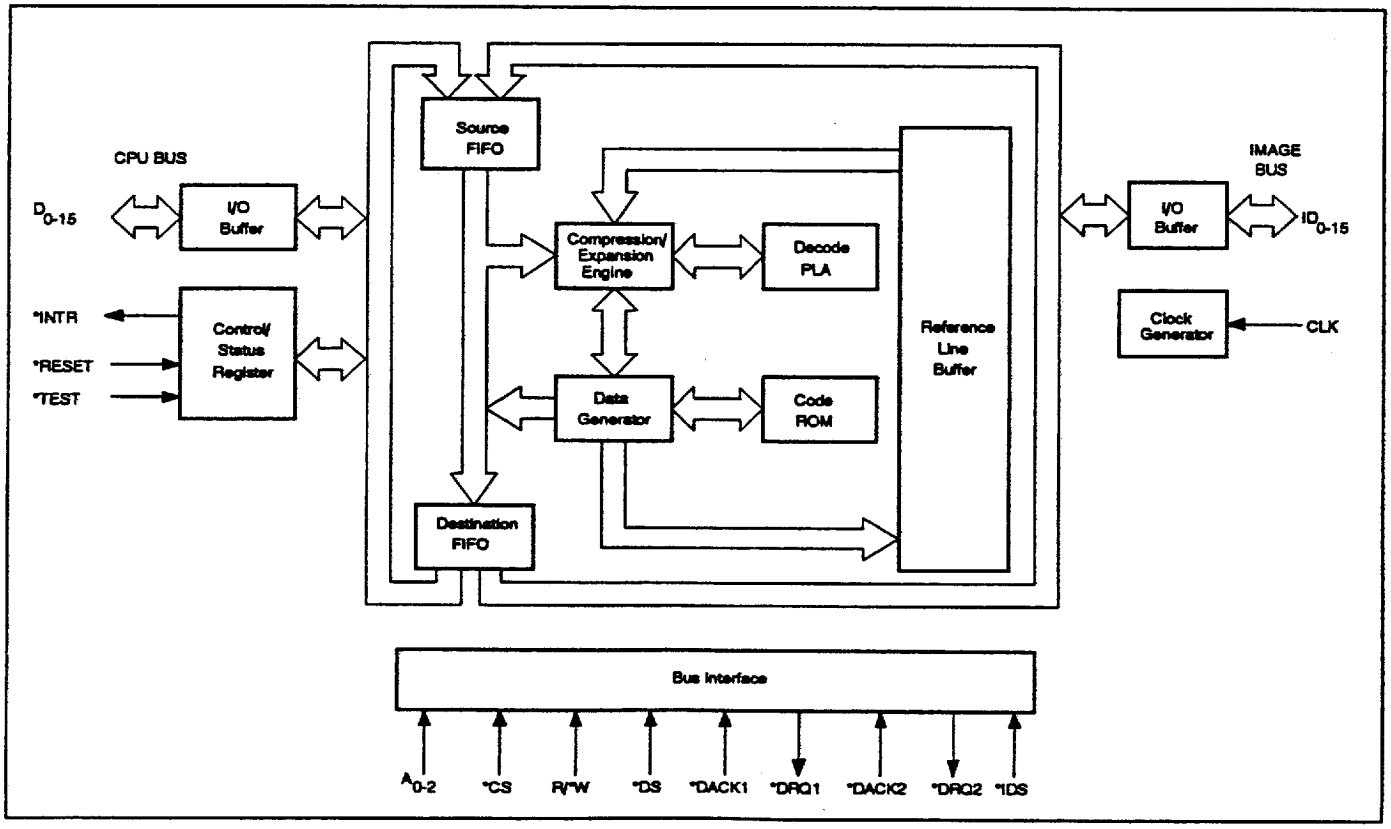
OTI-95C71

Video Compression/Expansion Processor

DISTINCTIVE CHARACTERISTICS

- Bitonal image compression or expansion at data rates in excess of 50 Mb/s
- Fully compatible with CCITT standards for Group 3 and Group 4 encoding
- Dual-bus architecture with single-bus option
- Supports bit-boundary image widths up to 8191 pixels without tiling in all modes
- 68-pin PLCC package
- On-chip 8191 pixel reference-line buffer for high-performance 2D coding
- Provides error detection and recovery capability
- Supports programmable k-Parameter for 2D coding
- 16-word FIFOs on input and output with status flag register
- Fully asynchronous bus interfaces

BLOCK DIAGRAM



Oak Technology, Inc. 139 Kifer Ct. Sunnyvale, CA 94086 TEL: (408)737-0888 FAX: (408)737-3838

GENERAL DESCRIPTION

The OTI-95C71 Video Compression/Expansion Processor (VCEP) is a high-performance CMOS processor which compresses and expands binary image data using the internationally standardized CCITT Group 3 and Group 4 algorithms.

The VCEP supports the Modified Huffman (MH), Modified Read or Modified Relative (MR), and Modified-Modified Read (MMR) coding schemes. MH coding is a one-dimensional technique which identifies and then codes run-lengths of black or white pixels for each scan line. Two-dimensional MR coding compresses each block of k scan lines using MH coding for the first line, followed by k-1 scan lines coded to reflect only differences from the pixel patterns of the previous scan line. The value of the k-Parameter is defined by the user and will generally be set to a larger number on communications links with lower bit-error rates. MMR coding uses an all-white imaginary reference line when coding the first scan line, and then two-dimensional coding for all remaining lines of a page. For a typical black and white image, MMR coding offers the best compression, followed by MR and then MH.

The CCITT Recommendation T.4 refers to MH and MR coding as Group 3 techniques and Recommendation T.6 refers to MMR coding as a Group 4 technique. Compressed data may be corrupted during transmission or storage. Group 3 error detection is provided by the VCEP to allow recovery on a line or block boundary (MH or MR). Detection of an error in Group 4 (MMR) requires retransmission of a page since recovery on less than a page boundary is not possible.

The extent of image data compression provided by Group 3 and Group 4 compression techniques depends heavily on the specific data patterns contained in the image. Typically, an originally black and white (binary) image will yield compression ratios between 5:1 and 50:1 depending on the mode and the runlengths encountered. The compression ratio improves as image resolution increases because the average runlength is greater. A binary image produced from a gray scale or color original using dithered or half-toned regions may compress poorly or even result in negative compression where the encoded data is greater than the raw image data in the regions with very short runlengths. Alternatively, the user may program the VCEP for transparent mode where data is simply passed from the Source FIFO to the Destination FIFO without compressing or modifying the data.

When 2D (MR or MMR) coding is performed the previous scan line is used as a reference to code the current line. To significantly increase performance the VCEP stores the reference line in an on-chip buffer of up to 8191 pixels.

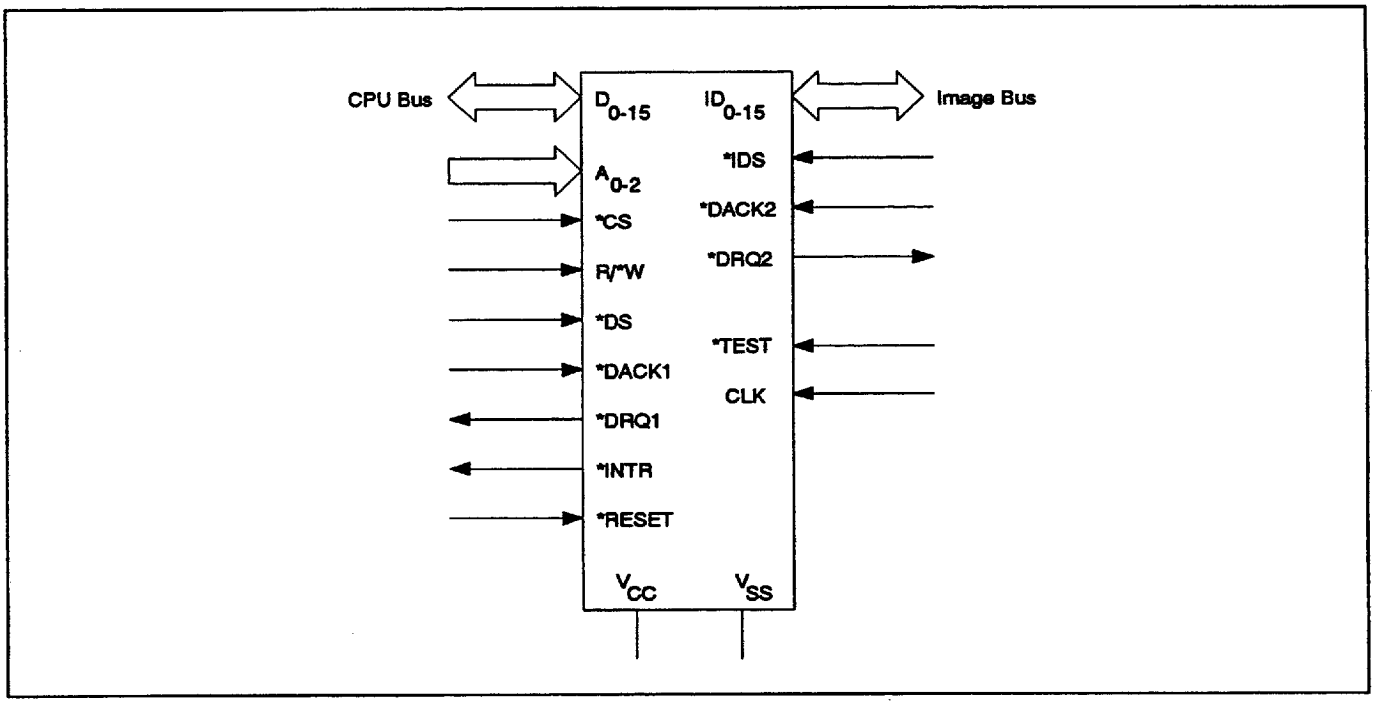
The VCEP is a slave-mode device with two, 16-bit asynchronous bus interfaces. The user may select either bus to be the source, the destination, or both. This allows single-bus or dual-bus system designs. Data is buffered on input and output by internal 16-word FIFOs. The VCEP may be set to either compress, expand or pass through data in transparent mode. It cannot do these operations simultaneously.

The VCEP has several mechanisms to detect data errors during expansion. For MH and MR modes, if the expanded scan line is longer or shorter than the user-programmed line length, the VCEP sets a flag and generates an interrupt for the host. (MMR code does not contain End-of-line codes to support this.) In all modes, illegal codes and other invalid fields are also detected as data errors. Upon a data error interrupt, the host CPU is responsible for error recovery by, for example, replicating the previous scan line, when an error is found in the current scan line. In MH and MR modes, when the VCEP suspends operation due to a data error, it can be restarted and will automatically search for the beginning of a new line before resuming expansion.

The VCEP has programmable burst and dwell counters for each bus to allow the user to restrict the duration of the VCEP's data requests and to extend the time between requests. If burst and dwell are programmed to zero, the VCEP will request and retain the bus as much as needed.

All registers on the VCEP are programmed by the host via the CPU bus, by selecting specific registers with the three address lines. The control registers should not be reprogrammed while an operation is active but may be read at any time. During an operation, the CPU bus FIFO data port may be accessed by either the address lines or a single data transfer acknowledge line. These types of accesses are referred to as flow-through and fly-by modes respectively. Data is always accessed on the Image bus by a fly-by cycle.

LOGIC SYMBOL



ORDERING INFORMATION

The VCEP is available in a 68-pin Plastic Leaded Chip Carrier (PLCC) and in two operating frequencies. Select the speed version by attaching the proper suffix as shown below.

OTI95C71 /20

Speed Option
/20 = 20 MHz
/16 = 16 MHz

Device Number/Description
OTI95C71
Video Compression/Expansion Processor (VCEP)

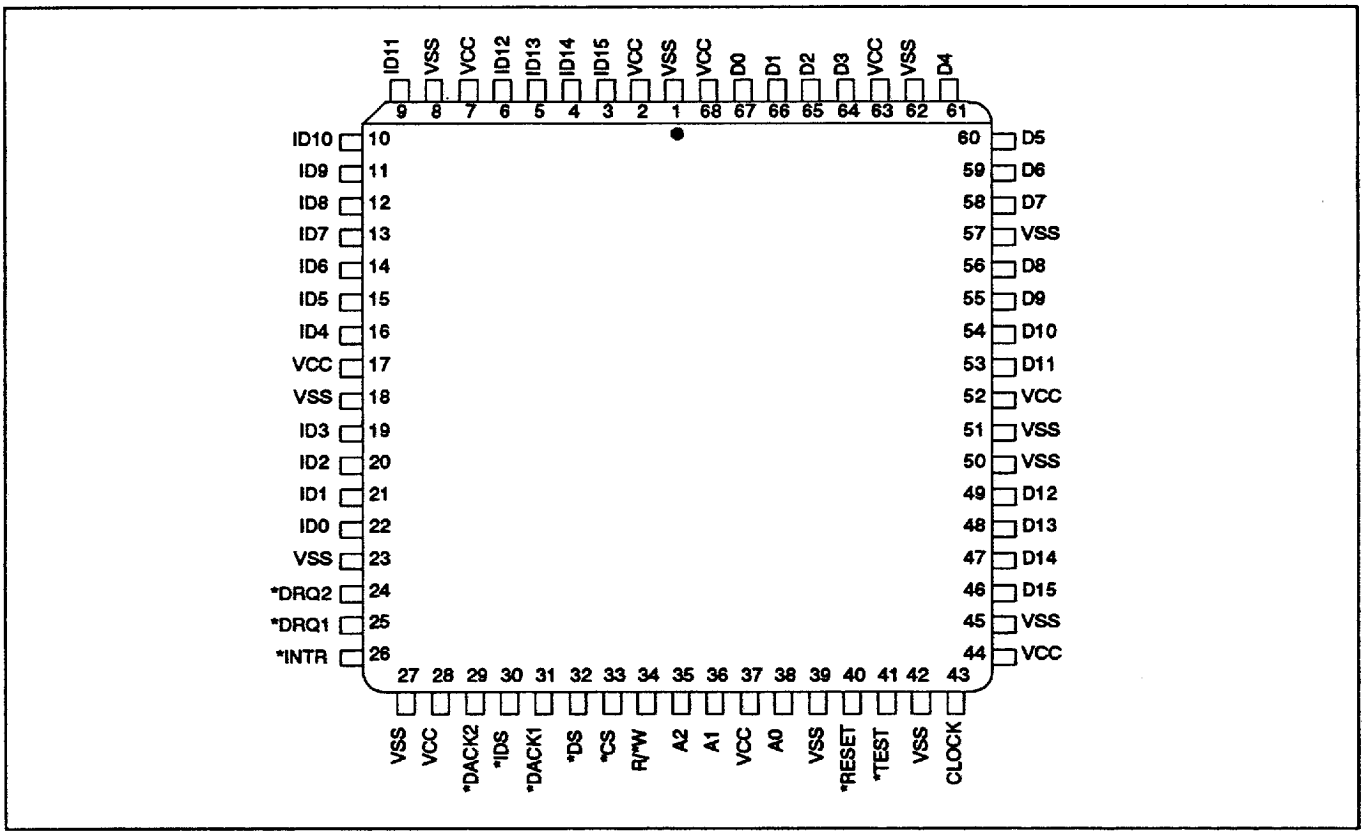
PIN DESCRIPTION

Pin Name	Direction	Description
A0-2	Input	**Address Bus** A 3-bit address used to select one of eight internal registers or the FIFO data port. These inputs are valid only when *CS is active for a flow-through access on the CPU bus.
*CS	Input	**Chip Select** An active-low input that qualifies *DS when performing a flow-through access on the CPU bus. *CS must be inactive when *DACKn is active for a fly-by access on the CPU bus. *CS may be held active for multiple access cycles.
*DS	Input	**Data Strobe** An active-low input that strobes all data transfers on the CPU bus. For CPU write cycles, data is latched on the rising edge of *DS.
R/*W	Input	**Read/*Write** An input that controls the direction of transfer on the CPU bus. R/*W must be high for a read cycle and low for a write cycle. This input is relevant only when *CS is active for a flow-through access on the CPU bus.
D0-15	I/O	**CPU Data Bus** A 16-bit, bidirectional, three-state data bus used for all accesses to the control registers and available for accesses to the input and output FIFOs during an operation.
*DRQ1, 2	Output	**Data Transfer Request 1 and 2** Active-low outputs that indicate the input or output FIFOs are requesting service. (See Table 1 for source and destination control assignments.)
*DACK1, 2	Input	**Data Transfer Acknowledge 1 and 2** Active-low inputs that qualify *DS or *IDS when performing a fly-by access on the CPU bus or Image bus. *DACK1 is asserted in response to a service request on *DRQ1 and *DACK2 is asserted in response to *DRQ2. (See Table 1 for control assignments.) *DACKn should not be asserted for a CPU bus access if *CS is active for a flow-through access of the CPU bus. *DACKn may be held active for multiple access cycles.
*IDS	Input	**Image Data Strobe** An active-low input that strobes fly-by data transfers on the Image bus. For write cycles, data is latched on the rising edge of *IDS. The direction of Image bus transfers is automatically determined by the source and destination control bits. (See Table 1.)
ID0-15	I/O	**Image Data Bus** A 16-bit, bidirectional, three-state data bus available for accesses to the input and output FIFOs during an operation.
*INTR	Output	**Interrupt Request** An active-low ouput that is asserted when an exception or termination condition occurs and the user has previously set the Interrupt Enable bit in the Command/Status Register. *INTR goes inactive when the Command/Status Register is read or when the VCEP is reset.

PIN DESCRIPTION

Pin Name	Direction	Description
*RESET	Input	**Reset** An active-low, asynchronous input which initializes the VCEP to an idle state. *RESET must be driven LOW for at least four clock cycles to execute a complete internal reset sequence.
*TEST	Input	**Test** An active-low input that, when held LOW, forces all VCEP outputs to three-state level. In normal use, this pin should be tied to a VCC pullup resistor or held at a TTL-HIGH level.
CLK	Input	**Clock** An input that provides the timing reference for all internal operations of the VCEP. CLK must be driven by an external source before initiating any VCEP operation. CLK may be stopped while the VCEP is idle.

CONNECTION DIAGRAM



Top View - Pin 1 is marked for orientation.

REGISTER DESCRIPTION

The VCEP has eight internal locations that are directly addressable for CPU bus flow-through accesses, using the three address inputs. Port location 0 accesses the FIFO Data Port and the other seven locations access the control and status registers needed to perform VCEP operations. See Figure 1 for the organization of control fields in these registers. *Note that all reserved bits should be programmed to zero.

FIFO DATA PORT 0

The FIFO Data Port allows flow-through accesses to write to the Source (input) FIFO or read from the Destination (output) FIFO. These accesses should only be made when the appropriate data request signal or flag is active. A FIFO access made when a request is inactive will cause the internal FIFO pointer to be shifted incorrectly. It is possible to mix flow-through and fly-by mode accesses on the CPU bus as long as *CS and the *DACKn are mutually exclusive.

COMMAND/STATUS REGISTER (CSR) PORT 1

The Command/Status Register contains command, control and status bit fields. It is normally written to initiate a VCEP operation and read to determine status. Writing to the CSR while a VCEP operation is in progress (GO = 1) will cause an Abort condition and the operation will be suspended. The CSR may be read at any time and this always clears the status flag bits. See Figure 2 for CSR bit assignments.

GO - CSR bit 15

The GO bit is used to start a VCEP operation in the mode indicated by the OM field. All control parameters in the other registers must be valid before writing the CSR with the GO bit set to 1. When GO is set, the VCEP will clear the status bits and start the selected operation. When the operation is complete, the VCEP will halt, wait for the Destination FIFO to be emptied, and then reset the GO bit. If the CSR is written while the VCEP is busy, the current operation will be aborted. In this case, *INTR will be activated to interrupt the CPU if the IE bit is set. A hardware or software reset should be issued to clear an abort condition.

When GO = 0, the VCEP is idle and may be reset or reprogrammed, but the FIFO Data Port should not be accessed. The GO bit should not be set when writing a Software Reset command. A hardware or software reset will always clear the GO bit.

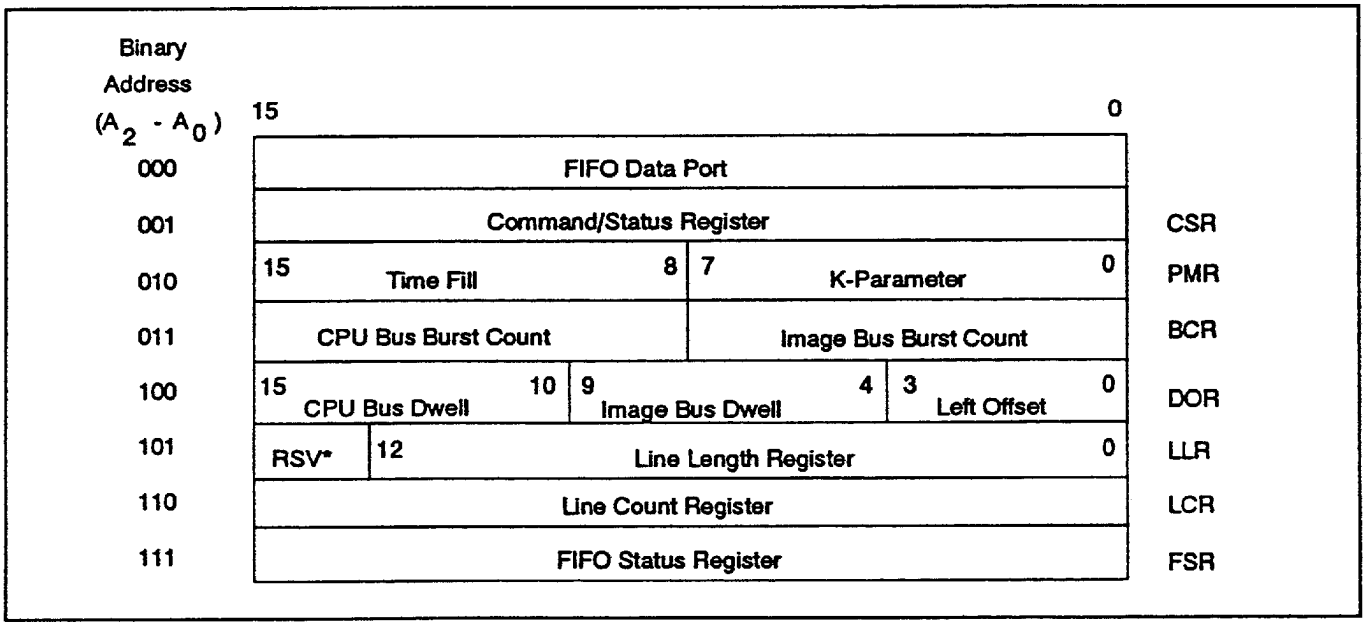


Figure 1. VCEP Register Set

COMMAND/STATUS REGISTER CONTINUED

Operational Mode (OM) - CSR 14:11

The OM field defines the type of operation to be performed as shown in Figure 2. Only the valid combinations of compression or expansion, transparent mode, or Software Reset should be programmed in this field. See the Operating Modes section for a detailed description of each type of operation.

A Software Reset command has the same effect as activating the hardware *RESET input pin. A software or hardware reset must be issued between each page of VCEP operations.

Page Mode (PM) - CSR bit 10

When PM is set, the VCEP will attempt to process an entire page of information before stopping and setting the PC flag. When PM = 0, referred to as Line Mode, the VCEP will stop after each scan line of the image is processed and indicate this by setting the LC flag. Line Mode allows greater control over the progress of an operation and is useful during the error recovery process. To restart a Line Mode operation, a command with the GO bit set should be issued. The VCEP may be switched between page and line mode when restarting. In all cases when halting, the GO bit is not cleared and the flags are not set until the Destination FIFO has been emptied.

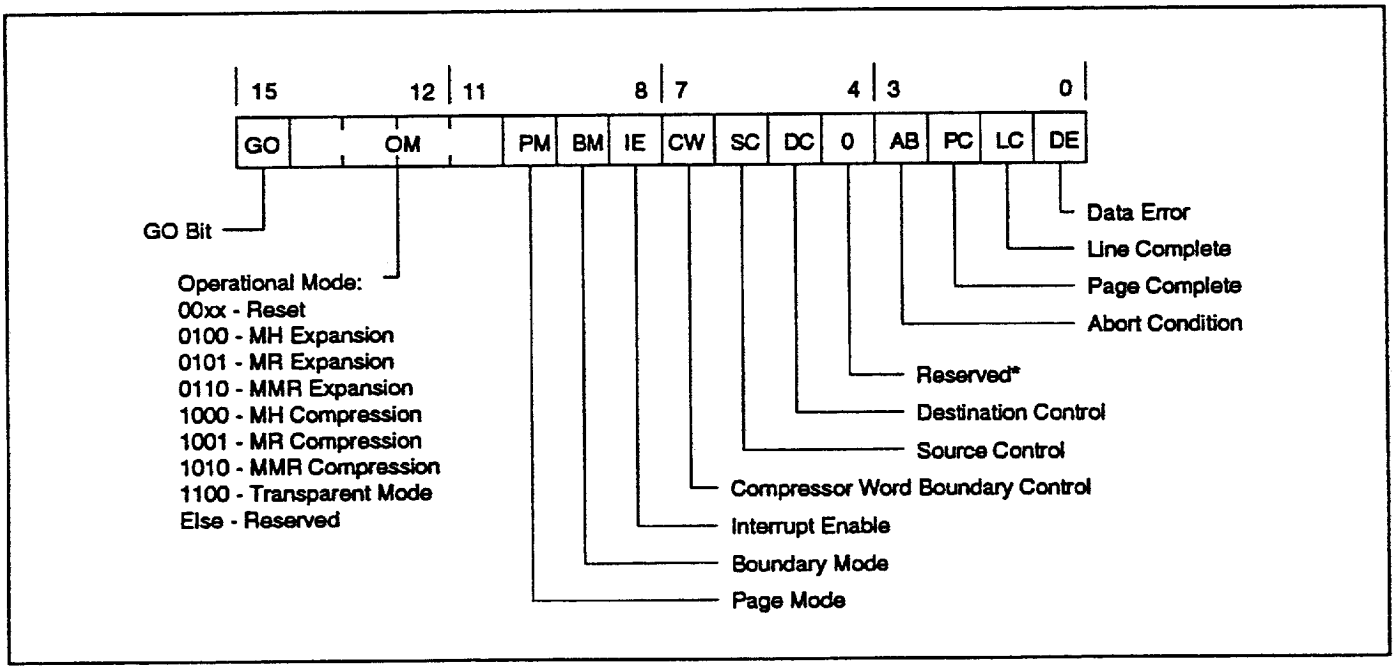


Figure 2. Command/Status Register

REGISTER DESCRIPTION

COMMAND/STATUS REGISTER CONTINUED

Boundary Mode (BM) - CSR bit 9

This bit defines whether the first code data word of a page is on a word boundary (BM = 0) or on an odd-byte boundary (BM = 1). For compression, if BM = 1, the VCEP inserts eight zeros before the first code word of a page so that the code begins on an odd-byte boundary, ie. bit 8 of the word. If BM = 0, no zeros are inserted and the code word begins on bit 0. For expansion, if BM = 1, the VCEP ignores the first eight bits (0-7) of the first code data word of the page and begins expanding from the second byte (bit 8). If BM = 0, the VCEP begins expansion from bit 0 of the first code data word.

Interrupt Enable (IE) - CSR bit 8

When IE is set, the *INTR output is activated whenever the VCEP encounters an exception or termination condition (AB, PC, LC or DE). However, *INTR does not go active until the Destination FIFO has been emptied. When IE = 0, *INTR is never activated.

Compressor Word (CW) - CSR bit 7

The Compressor Word boundary control bit is used to ensure that the compressed code for each scan line ends on a word boundary. In MH or MR compression mode, if CW is set, the VCEP will insert 0 to 15 pad bits (zeros) at the end of each line of code data to ensure that the line ends on a word boundary. If CW = 0, the variable length code words are packed sequentially without regard to data word boundaries as compression progresses from line to line. In MMR compression mode, this bit is ignored.

Source Control (SC) - CSR bit 6

If SC = 0, the CPU bus is selected as the input for data to the Source FIFO. When SC = 1, the Image bus is selected as the input source. See Table 1.

Destination Control (DC) - CSR bit 5

If DC = 0, the CPU bus is selected as the output for data from the Destination FIFO. When DC = 1, the Image bus is selected as the output destination.

(reserved) - CSR bit 4

Abort (AB) - CSR bit 3

If the Command/Status Register is written while an operation is in progress, the VCEP will abort processing and set the AB flag. To recover, a software or hardware reset must be issued and a delay of at

CSR Bits		SOURCE (Input)		DESTINATION (Output)	
SC	DC	Bus	Control Pins	Bus	Control Pins
0	0	CPU D0-15	*DRQ1/*DACK1	CPU D0-15	*DRQ2/*DACK2
0	1	CPU D0-15	*DRQ1/*DACK1	Image ID0-15	*DRQ2/*DACK2
1	0	Image ID0-15	*DRQ2/*DACK2	CPU D0-15	*DRQ1/*DACK1
1	1	Image ID0-15	*DRQ1/*DACK1	Image ID0-15	*DRQ2 /*DACK2

Table 1. VCEP Bus Assignment

least eight clock cycles must occur before issuing a command with the GO bit set to start a new operation. An abort is considered a non-recoverable condition and all data in process is lost.

Page Complete (PC) - CSR bit 2

When the VCEP detects the RTC/EOP code in expansion mode, it sets this flag. In compression or transparent mode, this flag is set when the Line Count Register has been decremented to zero. Either way, this Status flag indicates that the VCEP has processed a page of data.

Line Complete (LC) - CSR bit 1

When the Page Mode bit is reset, (PM = 0), the VCEP is in single-line mode and the Line Complete flag will be set when the VCEP has processed one line of data. The VCEP must be restarted to resume processing of the next line.

Data Error (DE) - CSR bit 0

When the VCEP detects a data error during expansion, this flag is set. Data error conditions are described in the section on Error Detection and Recovery.

See Table 2 for a summary of status information.

PARAMETER REGISTER (PMR) PORT 2

The Parameter Register contains the 8-bit Time-Fill value in the high byte and the 8-bit k-Parameter in the low byte.

Time-Fill (TF) - PMR 15:8

Time-Fill is an option for MH and MR compression modes and it's value specifies the minimum length of a coded line in words. This value may vary from 0 to 255 words. If zero is programmed, no fill bits are added to the code data. For any non-zero value, the VCEP will pad all coded lines of fewer words than the value specified by inserting zeros after the end of the coded data and before the next EOL code, with the Time-Fill bits always ending on a word boundary. Minimum line length is calculated as the sum of the lengths of the leading EOL code, the code words for the scan line, and the pad bits. An example of Time-Fill in the coded data stream is shown in Figure 5.

PMR bit 15 is the most-significant bit of the TF value and bit 8 is the least-significant bit.

AB	PC	LC	DE	Explanation
1	x	x	x	Operation Aborted due to CSR write while VCEP was Busy
0	1	0	0	Page Complete without Error
0	0	1	0	Line Complete without Error in Line Mode
0	0	0	1	Expansion Data Error detected due to illegal code or the expanded line length exceeded the programmed LLR value
0	0	1	1	Expansion Data Error detected due to illegal code or expanded line length less than LLR value, followed by an EOL code, or: MH or MR: Two EOLs followed by a non-EOL MMR: One EOL followed by a non-EOL (in EOP)
0	1	0	1	Expansion Data Error detected due to incorrect line length followed by an EOP code

Table 2. Summary of Status Information

REGISTER DESCRIPTION

PARAMETER REGISTER CONTINUED

K-Parameter (k) - PMR 7:0

The k-Parameter specifies for MR compression mode how many lines (k-1) will be compressed using two-dimensional coding after a one-dimensionally coded reference line. k may vary from 0 to 255. When k = 0, the first scan line of a page is 1D-coded and all remaining lines of the page are 2D-coded. When k = 1, all scan lines of the page are 1D-coded.

In single Line Mode (PM = 0), the value of k may be changed when the VCEP is idle. PMR bit 7 is the most-significant bit of k and bit 0 is the least-significant bit. The k-Parameter is valid only in MR compression and is ignored in all other modes.

BURST COUNT REGISTER (BCR) PORT 3

The Burst Count Register contains the 8-bit CPU bus Burst Count in the high byte and the 8-bit Image bus Burst Count in the low byte. Non-zero values may be programmed in the BCR in order to restrict the duration of active Data Request (*DRQ1,2) outputs. This feature may be used to prevent the VCEP from dominating the bus during an operation. Programming the Burst Count values to zero allows the VCEP to assert and hold the *DRQn outputs active as long as necessary to keep the FIFOs serviced. Since the VCEP is capable of processing a word every three clocks, a system with a longer bus cycle may see the *DRQn outputs stay active for an entire page of operation when BCR = 0. The Burst Counts may be programmed with values of 0 to 255. This provides for burst durations of unlimited, single-cycle, and a range of 4 to 1016 clock cycles. See the section on Burst and Dwell Control for a detailed description of the BCR.

DWELL/OFFSET REGISTER (DOR) PORT 4

The Dwell/Offset Register contains the 6-bit CPU bus Dwell Count field in bits 15:10, the 6-bit Image bus Dwell Count field in bits 9:4, and a 4-bit Left Offset Register (LOR) field in bits 3:0.

Dwell Count Register (DCR) - DOR 15:4

The Dwell Counts may be programmed with non-zero values in order to extend the time when the *DRQn outputs are held inactive. This feature may be used to prevent the VCEP from re-requesting the bus too quickly to allow other bus transactions to execute as desired. A Dwell Count of zero allows the VCEP to re-activate a *DRQn output as soon as a FIFO needs service. The Dwell Counts may be programmed with values of 0 to 63. This provides for dwell durations of unrestricted, and 8 to 504 clock cycles. See the section on Burst and Dwell Control for a detailed description of Dwell Count operation.

Left Offset Register (LOR) - DOR 3:0

The Left Offset Register field may be programmed with a non-zero value to force the VCEP to ignore the first 1 to 15 pixels at the beginning of each scan line of image data input during a compression operation, or to insert 1 to 15 zeros at the beginning of each scan line of image data output during an expansion operation. This feature is used to support bit-boundary image files where the left edge of an image may not be word-aligned. Note that the left-most pixel of an image word corresponds to bit 0 of the data word, and that bit 15 is the right-most pixel of a word. Setting the LOR to zero indicates that the left edge of an image is word-aligned and that no pixels should be ignored.

LINE LENGTH REGISTER (LLR) PORT 5

The Line Length Register specifies the number of pixels contained in one scan line of image data. The maximum image width is 8191 pixels and the minimum image width is 17 pixels. The three most significant bits of the LLR must be loaded with zeros. Note that if a non-zero Left Offset value has been programmed, the sum of LOR and LLR is limited to the minimum and maximum width values. The LLR may be read at any time and will always return the original programmed value. It does not have to be reprogrammed between operations for pages of the same width.

When the image width is not a multiple of 16, indicating that the right edge of an image file is not word-aligned, the VCEP ignores the last (most-significant) bits of the last image word of each scan line during compression and inserts zeros in the last image word of each scan line during expansion. This feature, combined with the LOR, supports true bit-boundary image files.

LINE COUNT REGISTER (LCR) PORT 6

The Line Count Register specifies the number of scan lines of an image for compression or transparent mode operations. In these modes the LCR will be decremented each time the VCEP processes one line. It may be read at any time to determine the progress of

an operation. When the LCR reaches zero, the VCEP terminates the page. The original programmed value is saved internally and restored each time the GO bit is set to allow multiple pages of the same size to be processed without reprogramming the control registers.

Expansion operations do not require a Line Count to execute properly because the correct number of lines is assumed when the EOP code is detected. The LCR should be initialized to zero and it is incremented each time the VCEP expands a line and may be read to determine progress or, at the end of a page, to determine the total number of lines in the image.

FIFO STATUS REGISTER (FSR) PORT 7

The FIFO Status Register contains five flag bits that may be used to monitor a VCEP operation and determine the condition of the internal Data Request lines and the Source and Destination FIFOs. This allows software to determine when FIFO accesses are appropriate without the use of external hardware to monitor the *DRQn outputs. Use of the FSR FIFO flags may be more efficient in some systems because burst transfers of 8 words can be supported.

Busy (B) - FSR bit 15

The Busy flag is active as long as the GO bit in the Command/Status Register is active. This flag is duplicated to allow software control of data transfers without having to read both the CSR and FSR.

(reserved) - FSR bits 14:4

Source Request (SR) - FSR bit 3

The Source Request flag is active if the *DRQn output pin for the Source FIFO is active. The Source FIFO is assigned to either the CPU bus or the Image bus depending on the setting of the SC and DC bits in the CSR. (See Table 1.)

Source Half-empty (SH) - FSR bit 2

The Source Half-empty flag is active if there is space for 8 or more words in the Source FIFO.

Destination Request (DR) - FSR bit 1

The Destination Request flag is active if the *DRQn output pin for the Destination FIFO is active. The Destination FIFO is assigned to either the CPU bus or the Image bus depending on the setting of the SC and DC bits in the CSR. (See Table 1.)

Destination Half-full (DH)-FSR bit 0

The Destination Half-full flag is active if there are 8 or more words available in the Destination FIFO.

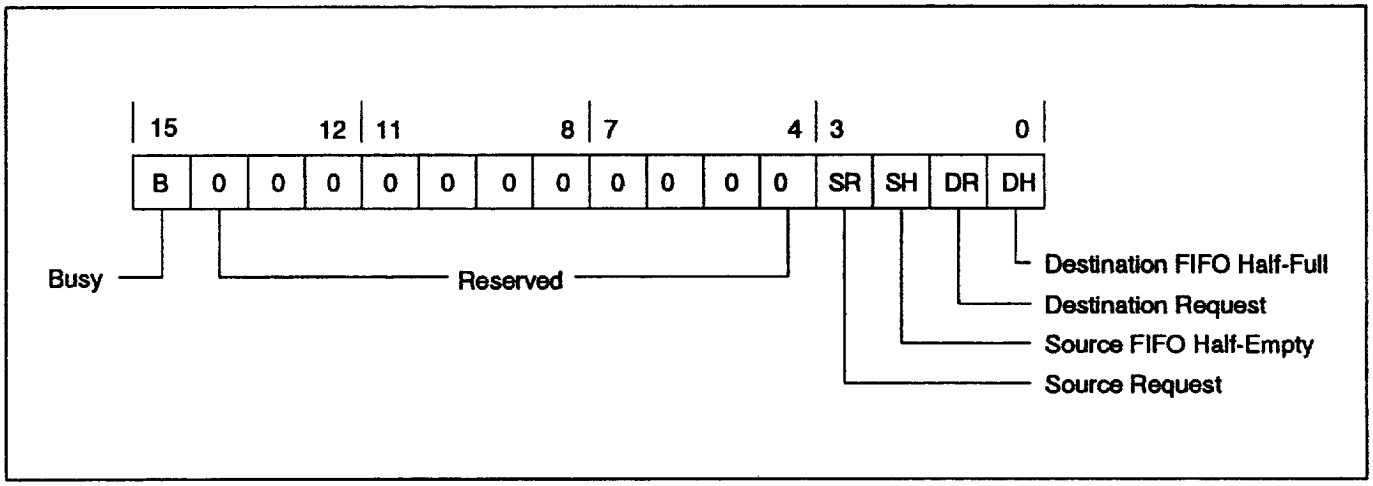


Figure 3. FIFO Status Register

FUNCTIONAL DESCRIPTION

The VCEP performs compression and expansion of bitonal (black and white or 1 bit/pixel) bit-mapped images using the CCITT standards T.4 and T.6. This is commonly referred to as "image compression" and is not to be confused with "data compression" that may be used on ASCII or binary data files. For clarity, the following terminology conventions are used:

Uncompressed files are referred to as image data, organized as image words that correspond to the 16-bit data words residing in a file or memory. Image words are arranged as a raster that starts at the upper left corner of the image with bit 0 of the first word and progresses along horizontal scan lines. The last word of each scan line of image data may be padded with zeros to ensure that each line ends on a word boundary. The VCEP's programmable left offset and line length serve to support bit-boundary image sizes.

Compressed files are referred to as code files, comprised of code words. A code word, or sequence of words, identifies a run length of black or white pixels. It is important to understand that code words, as defined in the CCITT code table, are variable length and may have no correspondence to data words in a file or memory. Code words are packed sequentially and fall on arbitrary word boundaries. There is an option (CW) to force the code for each image scan line to end on a data word boundary. Otherwise, only the end of a page will end on a word boundary and the EOP code may be padded with zeros to accomplish this.

The VCEP may be thought of as simply a conversion pump that receives image data at the input and generates code data at the output for compression, or receives code data at the input and generates image data at the output for expansion. Internally the compression/ expansion engine always takes input from the Source FIFO and sends output to the Destination FIFO via the Data Generator. Both FIFOs are 16 words deep.

As shown in the Block Diagram, an external bus master may use either the CPU bus or the Image bus to load the Source FIFO and either bus may be similarly used to unload the Destination FIFO. All internal operations are clocked by the CLK timing input, and all external bus operations are asynchronous. The FIFOs serve to decouple these operations and smooth the flow of data through the part. The VCEP engine will wait whenever the Source FIFO becomes empty or the Destination FIFO becomes full.

The CPU or DMA controller and VCEP clock rates may differ significantly within the following limitations:

If the VCEP clock is slower than the CPU clock, a lower limit is reached when more than one complete data transfer cycle occurs in one VCEP clock cycle. (Two transfer cycles cannot be recognized on the same clock). One data transfer per VCEP clock may occur on each bus of a dual-bus system since the buses are fully independent.

If the VCEP clock is faster than the CPU clock, or in the case of long data strobe widths, a limit is defined by the maximum low pulse width of *DS or *IDS. This limit is 15 VCEP clock cycles.

BUS INTERFACE CONTROL

The VCEP supports two types of accesses on the CPU bus: fly-by and flow-through. (These names relate to types of DMA controller cycles.) Flow-through accesses use the A_{0-2} inputs to address an internal location and *CS, R/*W, and *DS to control the transfer. All programmable control registers must be accessed in this manner and the FIFO Data Port may be accessed this way. Fly-by accesses on the CPU bus use *DACKn and *DS to control a transfer to or from the FIFOs. The Image bus supports only fly-by accesses to or from the FIFOs using the *IDS and *DACKn inputs. A fly-by write always goes to the Source FIFO and a fly-by read always comes from the Destination FIFO.

The *DRQ1/*DACK1 and *DRQ2/*DACK2 pins are assigned as pairs to the CPU and Image busses, depending on the setting of the Source Control (SC) and Destination Control (DC) bits in the Command/Status Register (CSR). Generally, the *DRQ1/*DACK1 pair is used for the CPU bus and *DRQ2/*DACK2 is used for the Image bus, unless one bus is used for both the Source and Destination. In these single-bus cases, the *DRQ1/*DACK1 pair is used for the Source and *DRQ2/*DACK2 is used for the Destination. (See Table 1.) Since the *DACKn input for the CPU bus enables a FIFO access, it must not coincide with an active *CS. The *DACK2 input for the Image bus may be tied to *IDS if the VCEP is never used in a single-bus mode.

The *DRQn outputs go active when the associated FIFO needs service and go inactive when the FIFO cannot be accessed. They are intended to work in a "demand mode". It is not possible to sample a *DRQn pin and do an eight word burst transfer, since a FIFO

may become full or empty at any time. If burst DMA transfers are desired, the FIFO Status Register (FSR) should be polled.

The *DRQn for the Destination FIFO will not go active until there are eight words in the FIFO (except at the end of a page or the end of a line in Line Mode) and will always go inactive when the FIFO is emptied. Empty may only occur at the end of a page. The *DRQn for the Source FIFO will not go active unless there are eight spaces available and will go inactive when the FIFO is full. Full may not happen during an entire page and the Source *DRQn will stay active until a reset is performed.

BUS BURST AND DWELL CONTROL

The VCEP is capable of processing one code word during expansion or one image word during compression every three clock cycles. (Average throughput will be less, depending on image complexity.) This data rate is frequently higher than the bus transfer rate of some systems, and a full page may be processed without ever filling the Source FIFO or emptying the Destination FIFO. In this case, the *DRQn outputs may stay active for the entire page. Consequently, it may be desirable to restrict the duration and delay between active request outputs to prevent the VCEP service from dominating the bus(ses). The programmable Burst and Dwell counters serve this purpose, but it should be noted that loading them with non-zero values will generally degrade overall VCEP performance.

The Burst Count Register (BCR) holds the 8-bit Burst Count values for the CPU bus and the Image bus. These values are completely independent and define the actual Burst Count of clock cycles that is given by:

Burst Clocks = (Burst Count Value - 1) X 4

This provides for Burst Counts of 4 to 1,016 clock cycles, during which a *DRQn output can remain active. Loading the BCR with zero disables the counter and allows the VCEP to hold the *DRQn output active for an unlimited time. Loading the BCR with a value of one causes the Burst Count to expire immediately on the first access allowing the *DRQn output to go inactive. This supports a single transfer for each *DRQn.

Programming the BCR with values greater than one enables the Burst Counter to begin decrementing the count, once per clock, starting from the beginning of the first FIFO access, until the Burst Count expires. After the count expires, the *DRQn output will go inactive at the beginning of the next FIFO access. The rising edge of a *DRQn output always conforms to the parameter #10 delay from the falling edge of *DS or *IDS, except in the case of reset. Also, regardless of the BCR value, a *DRQn output will always go inactive on the current access, if that access makes a FIFO go empty or full. The next request will begin a new burst period of the full count value.

In the boundary case where the Burst Count for the Source bus expires and the VCEP is waiting for the next access to make the *DRQn output inactive, but the last word of a page has already been transferred, the *DRQn output will stay active until a reset. Alternatively, sixteen null words can be written to the Source FIFO to force it to be full and force the *DRQn inactive.

The Dwell/Offset Register (DOR) holds the 6-bit Dwell Count values for the CPU bus and the Image bus. These values are completely independent and define the actual Dwell Count of clock cycles that is given by:

Dwell Clocks = (Dwell Count Value) X 8

This provides for a Dwell Count range of 0 to 504 clock cycles, during which the *DRQn output is prevented from going active to re-request service for a FIFO. Loading the Dwell Count with zero disables the counter and enables the VCEP to activate the *DRQn output without delay when the FIFO requires service or after a burst period.

Loading the Dwell Count with a non-zero value enables the counter to begin decrementing the count, once per clock, starting from the end of the last FIFO access of a burst period, until the count expires. After the count expires, the VCEP may activate the *DRQn output if the FIFO currently requires service.

The actual timing for the falling edge of the *DRQn outputs may vary since, in all cases, requests are triggered by external accesses but the rising edges of *DS or *IDS must be internally synchronized to the VCEP clock to start an operation.

When the VCEP is used in dual-bus operations, the effects of the Burst and Dwell control are completely independent for the CPU bus and the Image bus. However, in single-bus operations, the Burst/Dwell values for the bus used will affect both the *DRQ1 and *DRQ2 outputs. This means that both will go inactive on the last access of a burst period and the VCEP does not distinguish between read and write accesses.

FUNCTIONAL DESCRIPTION

PROGRAMMING OPERATIONS

The VCEP should be reset after power up and must be programmed to initiate the desired operation. A software reset operation has the same affect as activating the hardware *RESET input pin and either or both may be used after power up. The typical setup sequence after reset would be to program each of the control registers (PMR, BCR, DOR, LLR and LCR) in any order, and then write a command to the CSR that selects the Operational Mode (OM) and the desired control bit settings (PM, BM, IE, CW, SC and DC), and at the same time sets the GO bit to start the operation. All of the registers may be read at any time, but modifying parameters while the VCEP is active could produce unpredictable results. Writing to the CSR while an operation is active will always cause an abort condition.

Restarting an operation, such as a Line Mode operation or after handling an error, may require only rewriting the original command word to the CSR. While the GO bit is zero, any parameters or control bits may be changed if desired. It is also possible to change the control registers (not the CSR) while the VCEP is active for an operation (GO = 1), but idle due to an empty Source FIFO or a full Destination FIFO. To do this, a delay of up to 1,000 clocks may be required to ensure that the VCEP engine is waiting.

After each page operation, a software or hardware reset should be issued to the VCEP. This does not clear the values previously programmed in the control registers and the current value in the Line Count Register is replaced by the originally programmed value. This allows a series of pages of the same size to be processed with only a reset and a GO command between pages. A minimum of eight clocks of delay must occur after a reset before the next commmand is issued.

OPERATING MODES

Each type of operation is initiated by writing a command to the CSR with the desired mode and control bits selected and the GO bit set. A software reset command should not have the GO bit set and the control bits are not significant.

Compression

For compression, the VCEP engine takes image data from the Source FIFO and puts the compressed code data into the Destination FIFO. The values in the LLR and LCR are used to determine where the End-of-Line (EOL) codes and End-of-Page (EOP) code should be inserted. When the LCR specified number of lines are complete and all code words have been read from the Destination FIFO, the Page Complete (PC) flag in the CSR will be set. The *INTR output will be activated if the IE bit in the CSR was set when the GO command for the operation was issued.

The maximum line length value that can be loaded in the LLR is 8191 pixels. If the left offset value in the LOR is non-zero, the VCEP will ignore the first 1 to 15 bits, starting from bit 0 of the first image word of each scan line, according to the value programmed, and begin compression with the remainder of the first word. In this case, the value of LLR + LOR cannot exceed the maximum of 8191. Wider images can be divided into tiles for separate operations. Depending on the values of LLR and LOR, the last pixel of an image line may not end on a word boundary. The unused bits of this last word will be ignored by the VCEP and the next line must begin in the next word.

Several options may be selected with compression by use of the control bits in the CSR. If PM = 0, Line Mode is selected and the VCEP will halt after each image line is compressed and set the Line Complete (LC) flag and reset GO when the Destination FIFO is emptied. Since only whole 16-bit words of code stream are placed in the Destination FIFO, a partial word of code for the line may be retained internally until the beginning code of the next line is available. If the Compressor Word Boundary control bit (CW) is set, the final code for a line is padded with zeros, if necessary, to ensure that each line of code ends on a data word boundary. In this case, the Destination FIFO will always receive a complete line of code before halting in Line Mode. The padding is added to the last runlength code word and before the EOL code. This means that all lines actually start with an EOL code, as specified by the CCITT standard.

The Time-Fill value, programmed in the high byte (bits 15:8) of the Parameter Register, may be used to add padding to the end of a code line in a way similar to the CW option, except the TF value specifies the minimum length of a coded line in words. This means that the padding may be a partial word plus additional whole words to reach the TF minimum. Code lines that are longer than TF will not be padded unless CW is also set and the line needs to be padded to end on a word boundary.

If the Boundary Mode (BM) bit in the CSR is set for a compression operation, the VCEP will insert eight zeros in bits 0:7 of the first code word of a page and begin the compressed code (an EOL code) on an odd byte boundary or bits 8:15. The code will progress normally from that point.

MH Compression

For MH compression (OM = 1000) each scan line is one-dimensionally encoded, so the k-Parameter is ignored. The compressed code for each image line begins with an EOL code and the end of the last line of code is appended with six EOL codes. This EOP is referred to as a Return-to-Control (RTC) code by the CCITT standard.

MR Compression

In MR mode (OM = 1001), the first image line in each block of k scan lines is compressed one-dimensionally (1D) and then k-1 lines are compressed using the previous line as a reference for the current line (2D). (The VCEP's on-chip reference line buffer serves to drastically enhance performance for 2D modes.) The EOL code that precedes a 1D line is appended with a Tag bit that is set to a one. The EOL codes that precede 2D lines have a Tag bit of zero. All EOL codes that make up the RTC code have a Tag bit of one.

The k-Parameter is valid only in MR mode and ignored in all other modes. The range of k is 1 to 255. If k is set to 1, all lines of the page are 1D coded. If k is set to zero, the first line of the page is 1D coded and all remaining lines of the page are 2D coded. In Line Mode (PM = 0), the value of the k-Parameter may be changed while the VCEP is halted between lines. Otherwise, the k-Parameter value does not change and does not have to be reloaded after a reset.

MMR Compression

In MMR mode (OM = 1010), also known as Group 4, the VCEP will compress all image scan lines two-dimensionally using an all-zero (white) imaginary reference line for the first scan line, and the previous line as a reference for all remaining lines of the page. The CW, Time-Fill and k-Parameter options are not valid in MMR mode and the code stream does not contain EOL codes for each line. The EOP code, which consists of two 12-bit EOL codes, is the only overhead for a compressed file. Consequently, MMR provides the best compression ratio when compared to MH and MR modes. However, it is not possible to recover from an illegal or invalid code error, mid-page, during MMR expansion. A corrupted code file for a page must be retransmitted to the system to be correctly expanded. The PM and BM options in the CSR may be used in this mode.

Expansion

For expansion, the VCEP takes compressed code data from the Source FIFO and puts the expanded image data into the Destination FIFO. The value in the Line Length Register (LLR) is used to verify that each expanded line matches the expected length. If not, a Data Error (DE) is generated and processing halts. Error checking is also performed to detect illegal or invalid codes. The Line Count Register (LCR) is incremented after each line is correctly expanded and may be read by the CPU to monitor progress or to determine the total number of lines after a page is completed. The LCR should be initialized to zero prior to the first expansion operation and it will be automatically restored to the last programmed value each time the GO bit is set for a new page.

The options for expansion are more limited than for compression. If PM = 0, Line Mode is selected and the VCEP will suspend processing after each line is expanded and set the LC flag when the Destination FIFO is emptied. If the Boundary Mode (BM) bit is set, expansion of a page will begin with the code starting at bit 8, or the high byte of the first code word and the low byte (bits 0:7) will be ignored. If BM = 0, the code is assumed to begin on bit 0 of the first word. The CW bit and the Time-Fill and k-Parameter in the PMR are not used for expansion.

The Left Offset value in the DOR will be used to insert the programmed number of zeros into the first image word of each expanded line. The VCEP will automatically insert zeros in the last word of each image line if the programmed LOR and LLR does not result in lines that end on a data word boundary. Note that an expanded image would not match the original image in a file compare, if the original contained bits set to one in the Left Offset and right-most positions that are ignored during compression.

MH Expansion

In MH mode (OM = 0100), the VCEP will expand the code for each line one-dimensionally and ignore the k-Parameter. If an error in the code causes a Data Error (DE) to occur, the VCEP will halt and set the DE flag when the Destination FIFO is emptied. This allows

FUNCTIONAL DESCRIPTION

OPERATING MODES CONTINUED

the system to discard and replace the corrupted line. Restarting the operation will cause the VCEP to search for the next EOL code before resuming the expansion. Normally only a single line is lost in this recovery process.

MR Expansion

In MR mode (OM = 0101), the VCEP expands a 1D line if the Tag bit appended to the preceding EOL code is a one, and expands a 2D line if the Tag bit of the preceding EOL code is a zero. This implies that the error recovery upon a Data Error may require replacing multiple lines since a single error could corrupt an entire block of k lines.

MMR Expansion

In MMR mode (OM = 0110), the VCEP expands each line two-dimensionally using an imaginary all zero (white) reference line for the first line of code, and the previously expanded line as a reference for each remaining line of the page. Since line boundaries are not distinguished by EOL codes and all lines are 2D coded, it is not possible to recover from a Data Error mid-page.

Transparent Mode

In Transparent mode (OM = 1100), the VCEP transfers data directly from the Source FIFO to the Destination FIFO without modification. Control of the operation is similar to compression in that the LLR and LCR values are used to determine when the operation should be halted for Line Complete (LC) and/or Page Complete (PC) conditions, depending on the setting of the PM bit in the CSR. There is no error checking on the data being transferred. The Time-Fill and k-Parameter are ignored and the BM, CW and LOR bits should be programmed to zero.

Transparent mode is a simple operation normally used to transfer blocks of a programmed size through the VCEP to provide a data path between the CPU and Image busses. It should not be confused with the "uncompressed mode" that is an optional extension of the CCITT standards. The VCEP does not support uncompressed mode or automatically detect lines that result in negative compression.

Reset

A Reset command (OM = 00xx) has the same effect as activating the hardware *RESET input pin and these two may be used interchangeably. Reset causes the GO bit and the AB, PC, LC and DE flags in the CSR to be cleared. All of the flags in the FSR are cleared. The *DRQ1, *DRQ2 and *INTR output pins are driven inactive. The location pointers for reading and writing the Source and Destination FIFOs are moved to the "top" location but the data stored in the FIFOs is not cleared. The contents of the other control registers are not changed by a reset.

Reset must be internally synchronized by the VCEP in order to suspend the current operation and move the internal engine to an idle state. For this reason, it is necessary for a delay of eight VCEP clocks to occur after a reset, before issuing a command to start the next operation.

IMAGE DATA FORMAT

Image files are processed by the VCEP in such a way that the original image may be compresssed to a code file that may be expanded to produce an image that is identical to the original. The image data for this process must conform to the following conditions:

- An image is represented by an array of black and white pixels where white = 0 and black = 1.
- Images are transferred in 16-bit words by progressing along horizontal scan lines starting from the upper left corner.
- The top line of the image page is processed first, progressing from left to right, and each lower line is similarly processed until the bottom line is completed.
- The least significant bit 0 of each image data word is considered the left-most pixel of that word and bit 15 is the right-most.
- Each scan line is contained in a sequence of image data words that begin and end on word boundaries.
- During compression, any unused bits in the first and last words of each line, depending on LOR and LLR values, are ignored.
- During expansion, any unused bits in the first and last words of each line, depending on LOR and LLR values, are filled with zeros.

Note that if any of the unused bits mentioned above are set to one in the original image file, they will be zeros in the expanded image file. See Figure 4 for details on the image data format.

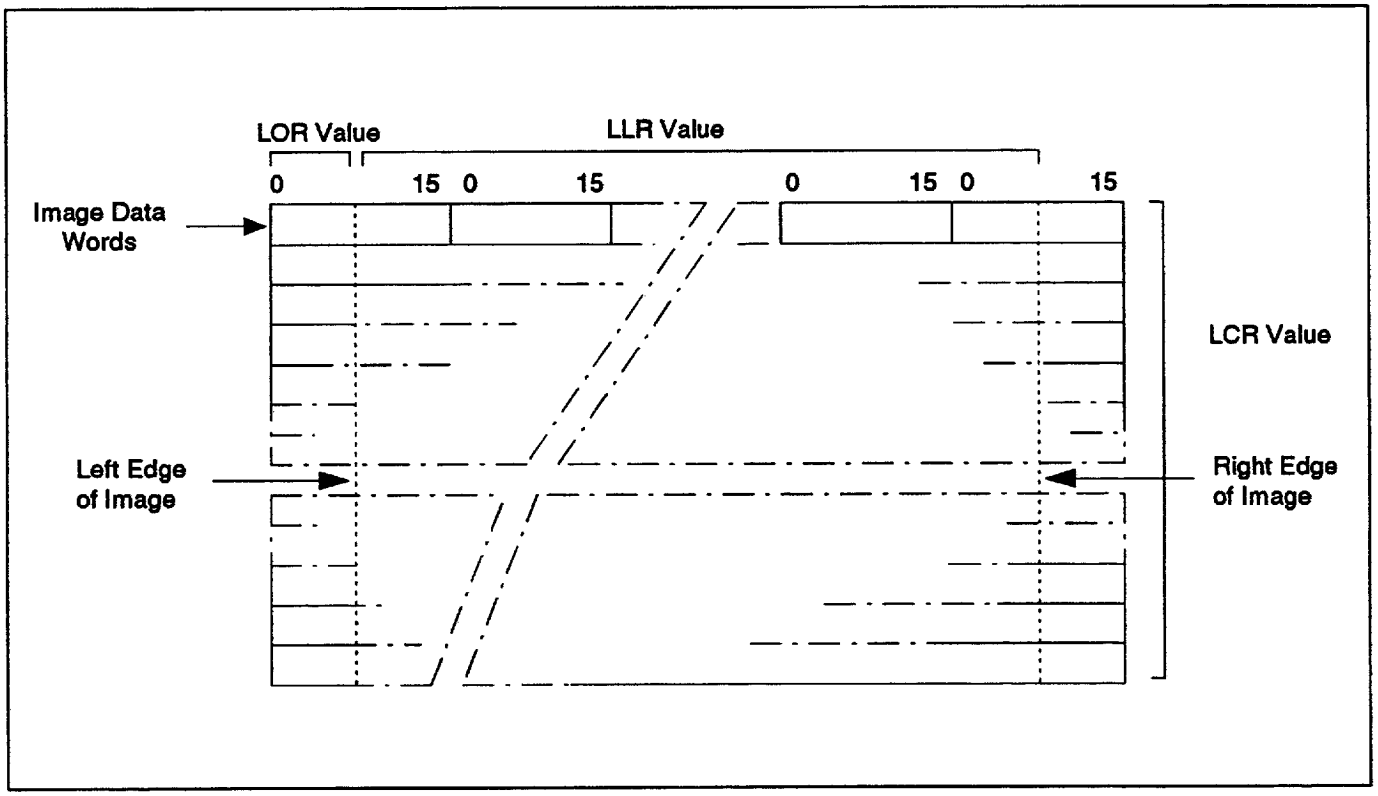


Figure 4. Image Data Format

DATA FORMATS

COMPRESSED CODE FORMAT

The format of compressed code streams conforms to the CCITT standard to ensure that files from all sources are compatible. The VCEP packs the variable length code word stream into data words using the following conventions:

- Code words are 1 to 13 bits as they appear in the CCITT code tables.
- Code words are packed into 16-bit data words without regard to word boundaries.
- The left-most bit of a code word comes first in the code stream and the right-most bit comes last.
- The code stream progresses from bit 0 of a data word to bit 15 and fills as many data words as necessary.

As the above conventions indicate, individual code words in the code stream are only recognizable when a sequence of data words is displayed in binary form with bit 0 on the left and bit 15 on the right. For additional details on the format of the compressed code, see Figure 5.

END-OF-LINE AND END-OF-PAGE CODES

The EOL code defined by the CCITT standard for Group 3 is a 12-bit code word:

000000000001

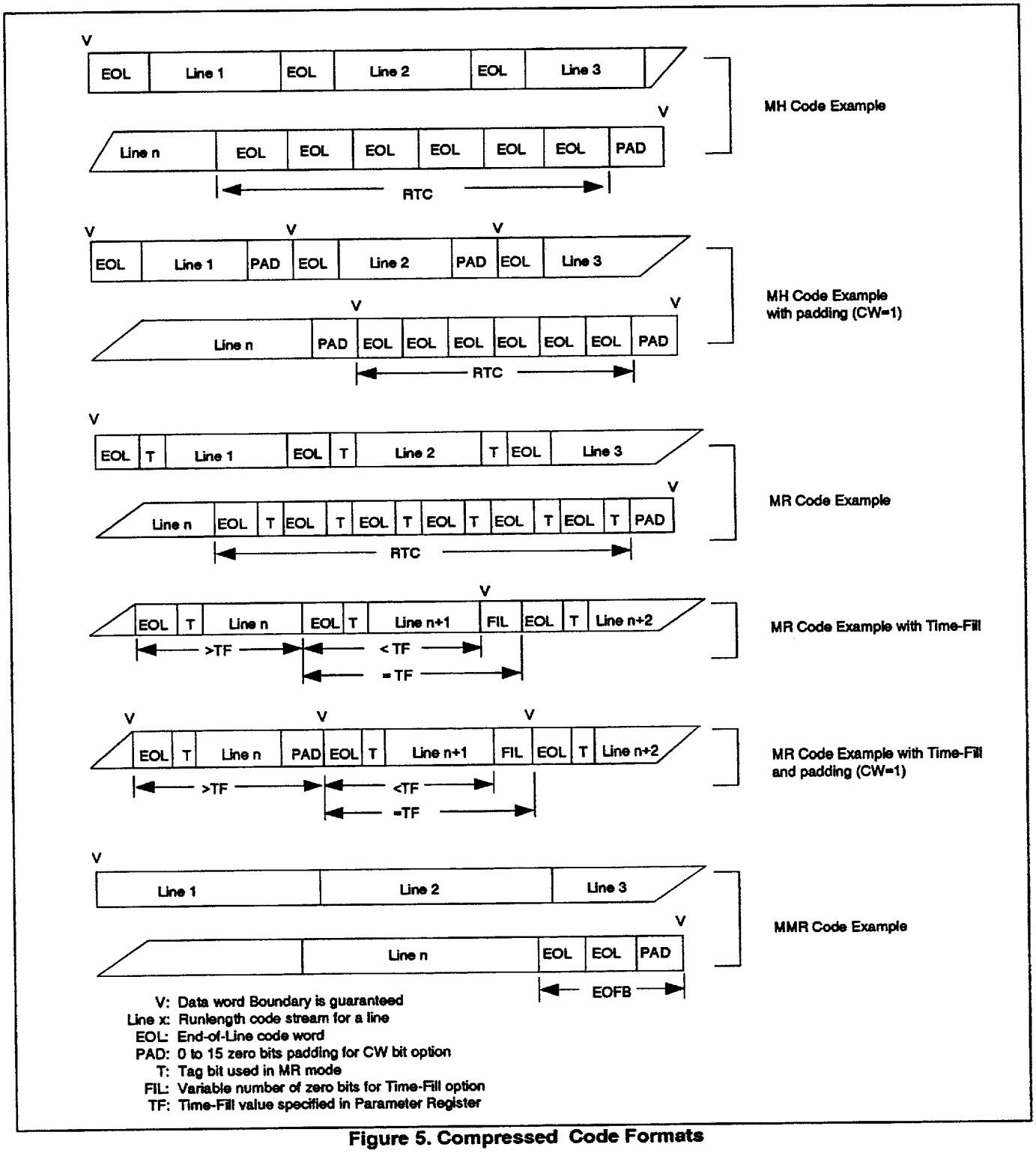
In MH mode, this word precedes the stream of runlength codes for each line. The code stream for the last line is followed by six consecutive EOL codes to indicate the End-of-Page (EOP).

In MR mode, every EOL code is appended with one Tag bit:

000000000001T

Where T is a one if the following line is a 1D-encoded line and T is a zero if the following line is 2D-encoded. The Tag bits of the six EOL codes that make up the EOP for MR mode are all set to one. The EOP code for Group 3 is referred to as a Return-to-Control (RTC) code in the CCITT specification.

For MMR mode, there are no EOL codes inserted in the code stream for each line. The EOP is indicated by two consecutive 12-bit "EOL" codes to form a 24-bit word that is referred to as the End-of-Facsimile Block (EOFB) code in the Group 4 specification.



V: Data word Boundary is guaranteed
Line x: Runlength code stream for a line
EOL: End-of-Line code word
PAD: 0 to 15 zero bits padding for CW bit option
T: Tag bit used in MR mode
FIL: Variable number of zero bits for Time-Fill option
TF: Time-Fill value specified in Parameter Register

Figure 5. Compressed Code Formats

SYSTEM INFORMATION

ERROR DETECTION AND RECOVERY

The VCEP detects certain error conditions during expansion operations which cause processing to halt. As soon as the Destination FIFO is emptied, one or two Status flags will be set and the GO bit will be reset. The *INTR output will be activated if the IE bit was set. The following error conditions are detected:

1. The expanded line length is longer than the LLR value.
2. The expanded line length is shorter than the LLR value when an EOL is detected (MH/MR only).
3. The expanded line length is shorter than the LLR value when an EOP is detected.
4. The codes indicate that a runlength is negative.
5. One of the following illegal codes is encountered:

   0000001
   00000001
   000000001
   0000000001
   00000000001
6. Two consecutive EOL codes followed by a non-EOL code (MH/MR only.)
7. One EOL code followed by a non-EOL code (MMR only).

In the above cases where an error and an EOL code is detected (#2, 6 and 7), the LC flag will be set in addition to the DE flag. In the case where an error and an EOP code is detected (#3), the PC flag will be set in addition to the DE flag.

In MH and MR modes, the system may accomplish error recovery by replacing the current image line containing the error, with the last correctly expanded image line. The VCEP may then be restarted by writing a command to the CSR with the GO bit set. If desired, the VCEP may be restarted in Line Mode to simplify recovery when an error affects multiple lines, as is frequently the case in MR mode where a single error could affect a block of k lines. When an error is indicated only by the DE flag, restarting will cause the VCEP to search for the next EOL code before resuming expansion. When both DE and LC are set, expansion will resume immediately upon restarting because an EOL code has already been detected. The Status flags are always cleared by restarting.

IMAGE PROCESSING TIME

The VCEP's performance, in terms of data throughput, is dependent on the complexity of the image and the bus bandwidth available to transfer image data. An average throughput of 50 Mb/s is obtained on 200 dpi documents #4 and #7, which are the most complex of the eight standard CCITT test documents. The other six test documents achieve higher throughput, as would documents scanned at higher resolutions, since they will achieve better compression ratios.

During expansion, the VCEP can process one code word (1 to 13 bits) in three clock cycles. During compression, the VCEP can process one runlength of up to 16 bits in three clock cycles. If the maximum clock rate of 20 MHz is used, one runlength will be processed every 150 ns. This means that if an image consisting of alternating black and white pixels is compressed by the VCEP, it will be processed at one bit per 150 ns, or 6.67 Mb/s. At the other extreme, an all-white image will be processed at 16 bits per 150 ns, or 106.7 Mb/s. While each document is unique, analysis shows that the worst image regions of the CCITT test documents contain five runlengths per 16 bits. In this practical worst-case condition, the VCEP would still throughput data in excess of 20 Mb/s. Note that throughput in Transparent mode will always be 16 bits per three clocks.

The transfer of image data to or from the VCEP will often affect performance. During expansion for example, image data must be removed by the system from the Destination FIFO at a rate at least equal to the engine speed to provide maximum system throughput. A dual-bus system provides the better opportunity for optimum performance since all available bus bandwidth on one bus may be used for transferring image data. However, assuming a document has a 10:1 compression ratio, a single-bus system would have to transfer only 10% more data to achieve the same performance.

Optimum* 20 Mhz VCEP Throughput

200 dpi CCITT Test Documents 1-8

	Compression						Expansion					
DOC	MH		MR		MMR		MH		MR		MMR	
#	ms	Mbit/s	ms	Mbit/s	ms	Mbit/s	ms	Mbit/s	ms	Mbit/s	ms	Mbit/s
1	44.4	89.9	45.8	86.7	46.0	86.7	43.6	91.5	46.8	85.3	47.0	84.9
2	42.4	94.1	43.9	92.8	42.8	93.2	41.0	97.3	44.0	90.7	44.4	89.9
3	48.2	82.8	50.6	78.9	50.4	79.1	46.4	86.0	51.2	77.9	52.2	76.4
4	58.2	68.6	64.8	61.6	64.6	61.8	56.6	70.5	65.2	61.2	67.7	59.0
5	49.4	80.8	52.0	76.7	76.7	51.8	48.0	83.1	52.8	75.6	53.8	74.2
6	45.2	88.3	46.2	86.4	46.0	86.7	43.6	91.5	46.8	85.3	47.7	84.2
7	56.8	70.2	64.0	62.3	64.0	62.3	54.6	73.1	65.2	61.2	68.4	58.3
8	44.6	89.5	45.6	87.5	45.8	86.7	42.6	93.7	46.0	86.7	46.8	85.3

* These values were obtained on an evaluation board setup to ensure that throughput is not limited by delays in servicing the VCEP FIFOs.

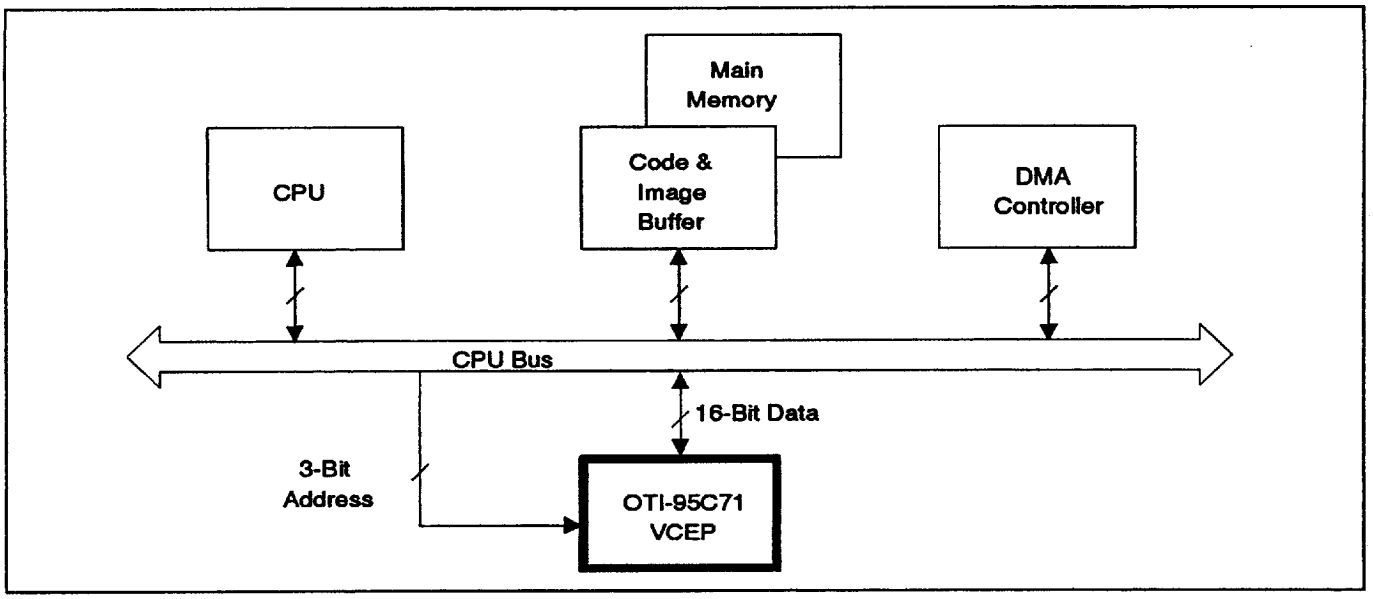
Example* 20 Mhz VCEP Throughput

200 dpi CCITT Test Documents

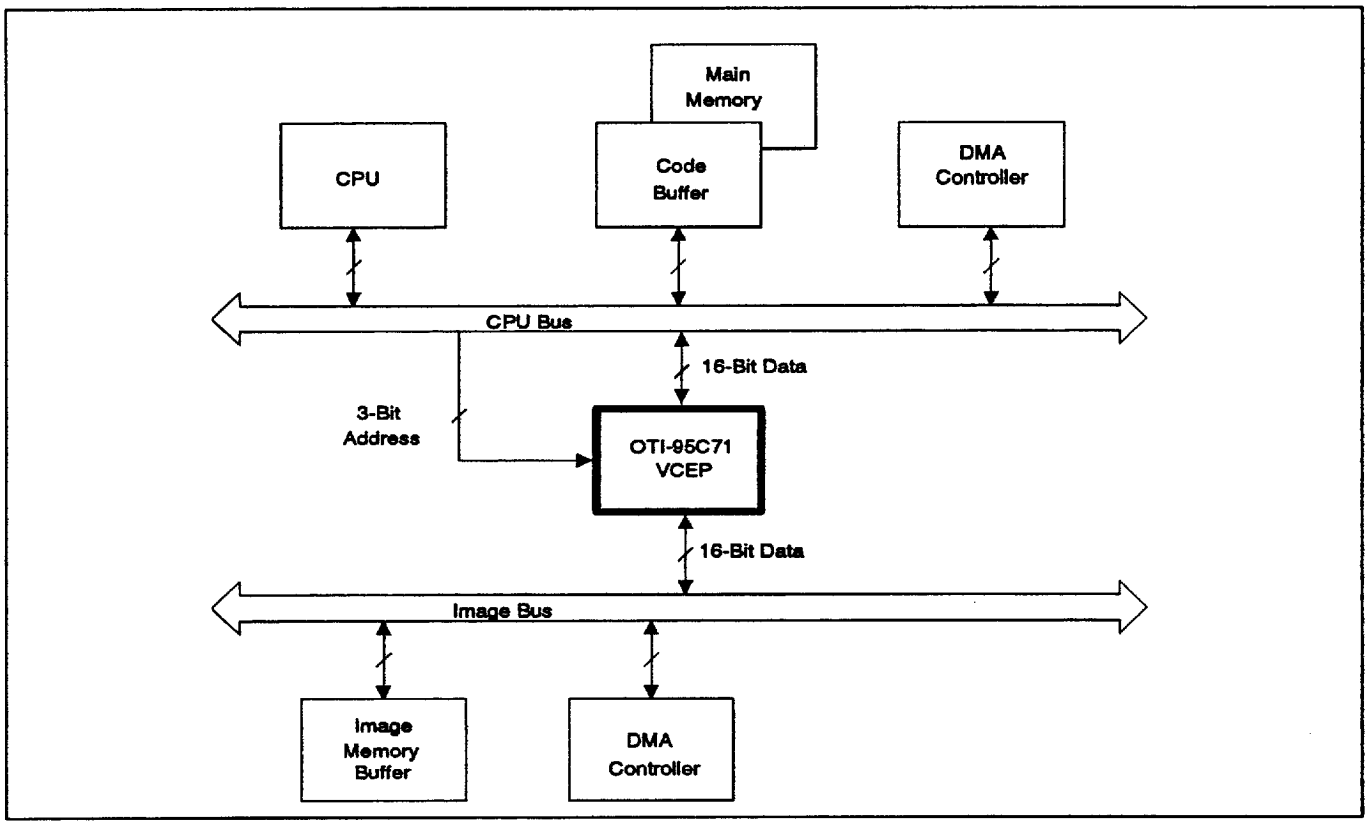
	Compression						Expansion					
DOC	MH		MR		MMR		MR		MH		MMR	
#	ms	Mbit/s	ms	Mbit/s	ms	Mbit/s	ms	Mbit/s	ms	Mbit/s	ms	Mbit/s
1	64.8	61.6	65.9	60.6	65.9	60.6	52.2	76.4	53.8	74.2	54.4	73.4
2	64.3	62.1	64.3	62.1	64.3	62.1	50.6	78.9	51.1	78.1	50.5	79.0
3	64.8	61.6	66.5	60.0	66.4	60.1	52.7	75.7	56.0	71.3	57.1	69.9
4	72.0	55.4	77.4	51.6	77.4	51.6	62.6	63.7	69.7	57.3	71.4	55.9
5	65.9	60.6	68.1	58.6	68.1	58.6	54.4	73.4	57.1	69.9	58.8	67.9
6	64.3	62.1	64.3	62.1	64.9	61.5	50.5	79.0	51.6	77.3	51.7	77.2
7	65.4	61.0	70.9	56.3	70.8	56.4	57.7	69.2	67.6	59.0	70.8	56.4
8	64.3	62.1	63.7	62.6	64.2	62.2	50.5	79.0	50.5	79.0	51.1	78.2

* These values were obtained on an evaluation board using bus transfer cycles that are 4 or 5 clocks long and may limit throughput .

SYSTEM INFORMATION



Single-Bus Configuration



Dual-Bus Configuration

ABSOLUTE MAXIMUM RATINGS

Storage Temperature.....-65 to +150°C

Maximum V_{CC} Relative to V_{SS}.....-0.3 to +7.0 V

DC Voltage Applied to Any Pin

Relative to V_{SS}.....-0.5 to V_{CC}+ 0.3 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A).....0 to +70°C

Supply Voltage (V_{CC}).....+4.75 to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage		-0.5	+0.8	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} +0.5	V
V_{OL}	Output LOW Voltage	I_{OL}= 2.0 mA		+0.4	V
V_{OH}	Output HIGH Voltage	I_{OH}= 250 µA	2.4		V
I_{LI}	Input Leakage Current	0 < V_{IN} < V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0.45 < V_{OUT} < V_{CC}		±10	µA
I_{CC}	Power Supply Current			80	mA

CAPACITANCE

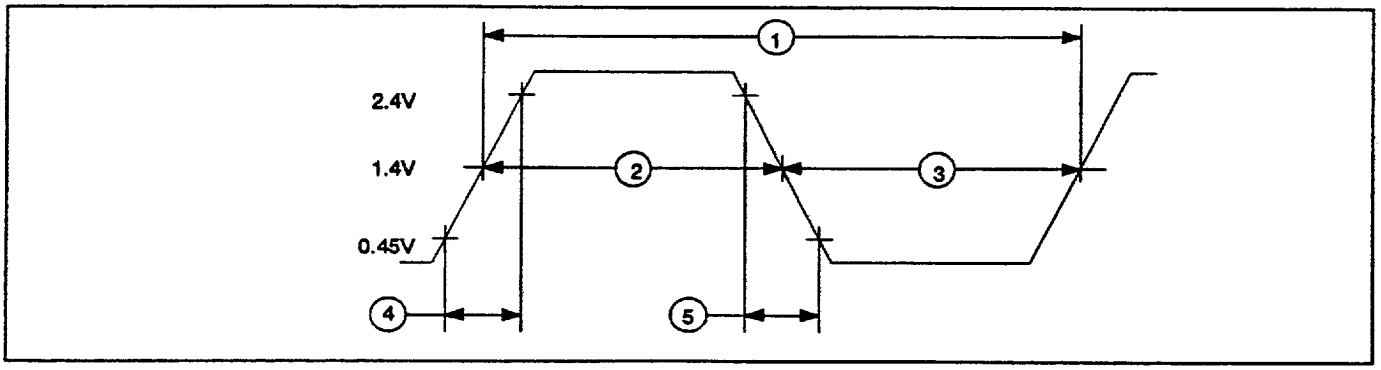
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Pin Capacitance			10	pF
C_{OUT}	Output Pin Capacitance	f_C = 1 MHz		15	pF
$C_{I/O}$	I/O Buffer Capacitance			20	pF

SWITCHING CHARACTERISTICS

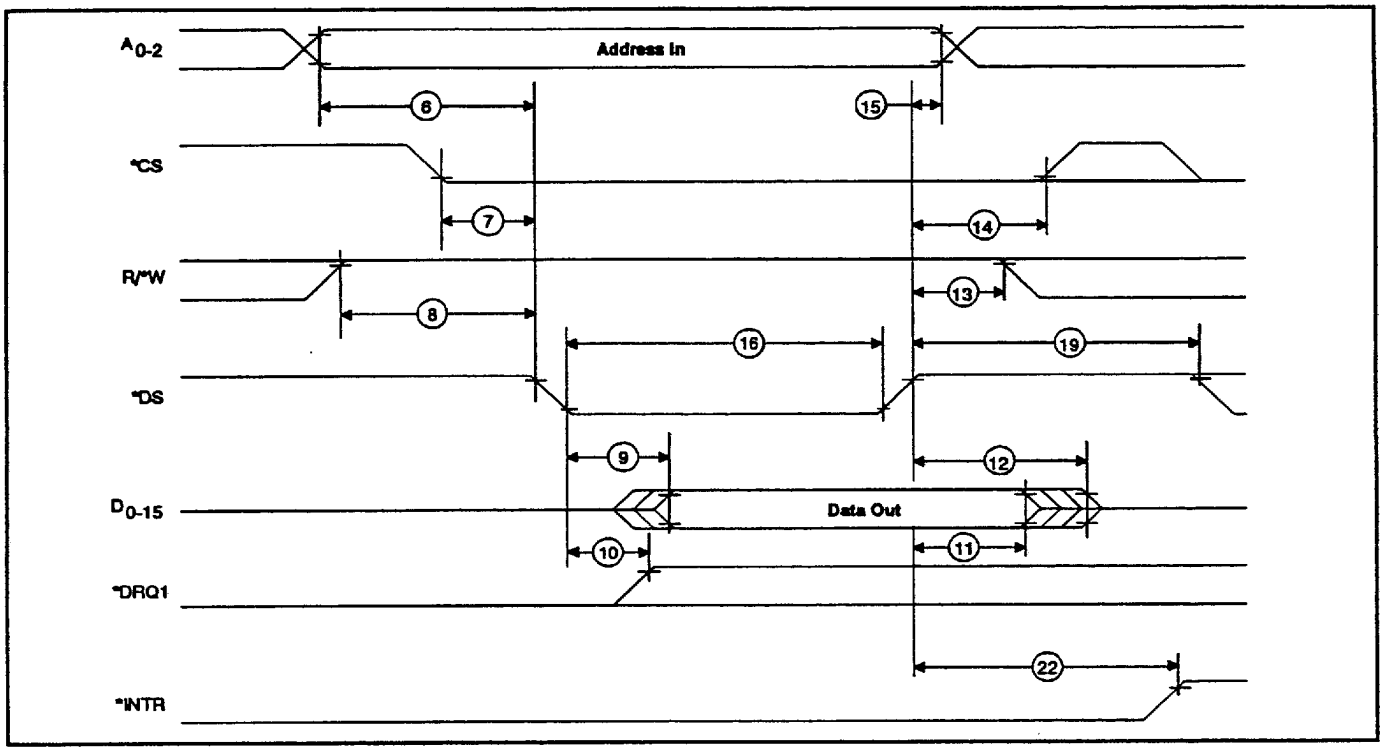
Guaranteed over operating range (T_A = 0 to 70°C, V_{CC} = 5V ±5%)

Parameter		Parameter	95C71-20		95C71-16		
No.	Type	Description	Min.	Max.	Min.	Max.	Unit
1	t_{PD}	Clock Period	50	500	62	500	ns
2	t_{PWH}	Clock HIGH Time	23		28		ns
3	t_{PWL}	Clock LOW Time	23		28		ns
4	t_R	Clock Rise Time		5		5	ns
5	t_F	Clock Fall Time		5		5	ns
6	t_S	Address Valid to *DS FE Setup Time	10		10		ns
7	t_S	*CS Valid *DS FE Setup Time	0		0		ns
8	t_S	R/*W Valid to *DS FE Setup Time	10		10		ns
9	t_D	*DS/*IDS FE to Data Output Valid Delay		50		55	ns
10	t_D	*DS/*IDS FE to *DRQ RE Delay	0	40		45	ns
11	t_H	*DS/*IDS RE to Data Output Hold Time	0		0		ns
12	t_D	*DS/*IDS RE to Data Out Float Delay		40		45	ns
13	t_H	*DS RE to R/*W Valid Hold Time	0		0		ns
14	t_H	*DS RE to *CS Valid Hold Time	0		0		ns
15	t_H	*DS RE to Address Valid Hold Time	0		0		ns
16	t_{PWL}	*DS/*IDS LOW Width	65	(Note 2)	75	(Note 2)	ns
17	t_S	Data In Valid to *DS RE Setup Time	35		40		ns
18	t_H	*DS RE to Data In Valid Hold Time	0		0		ns
19	t_{PWH}	*DS/*IDS HIGH Width	45		55		ns
20	t_S	*DACK FE to *DS/*IDS Setup Time	0		0		ns
21	t_H	*DS/*IDS RE to *DACK RE Hold Time	0		0		ns
22	t_D	*DS RE to *INTR RE Delay Time		40		45	ns
23	t_{PWL}	*RESET LOW Width	(Note 1)		(Note 1)		ns

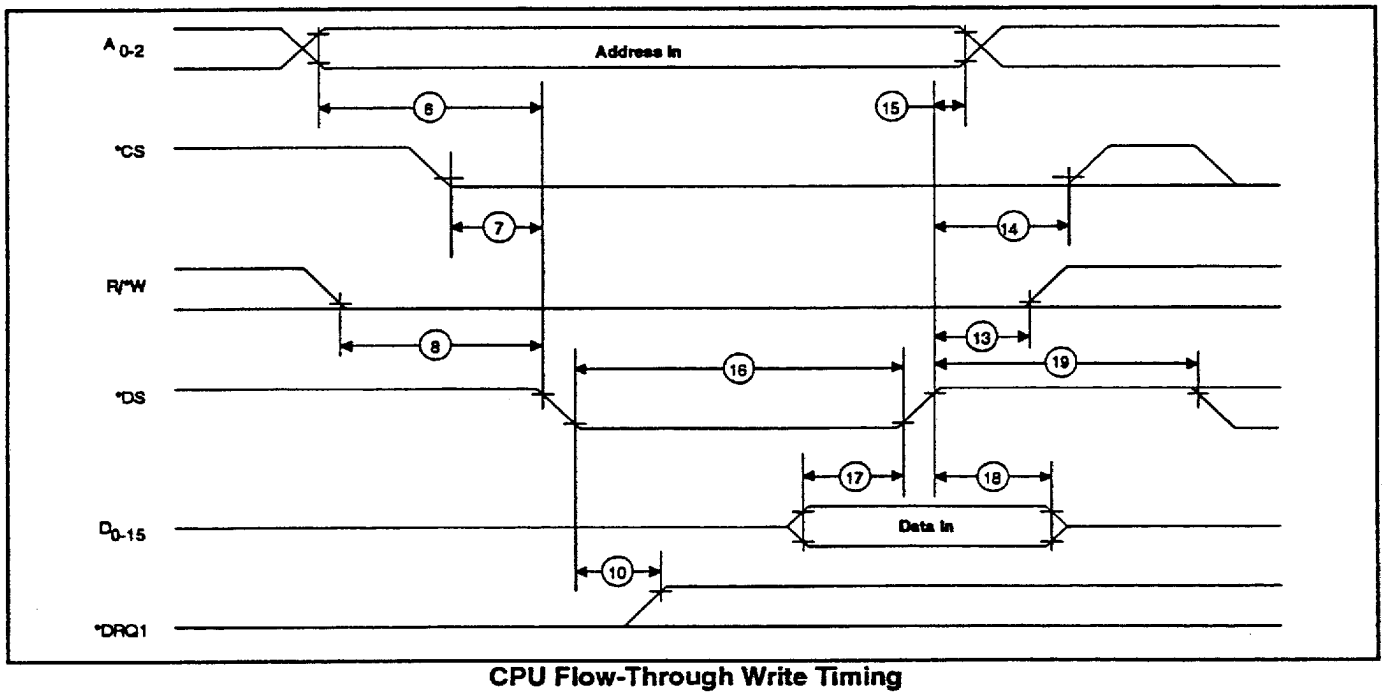
Notes: 1. Minimum *RESET LOW Width is four clock periods (see parameter 1).
2. Maximum *DS/*IDS LOW Width is fifteen clock periods.



Clock Timing

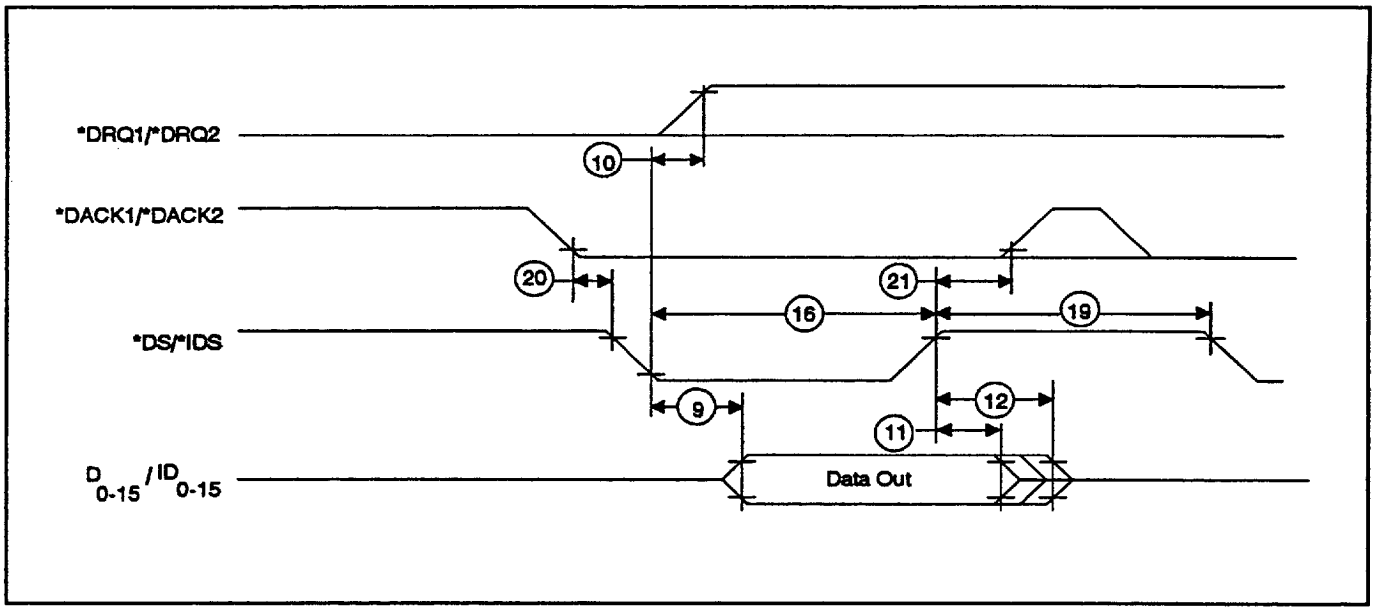


CPU Flow-Through Read Timing

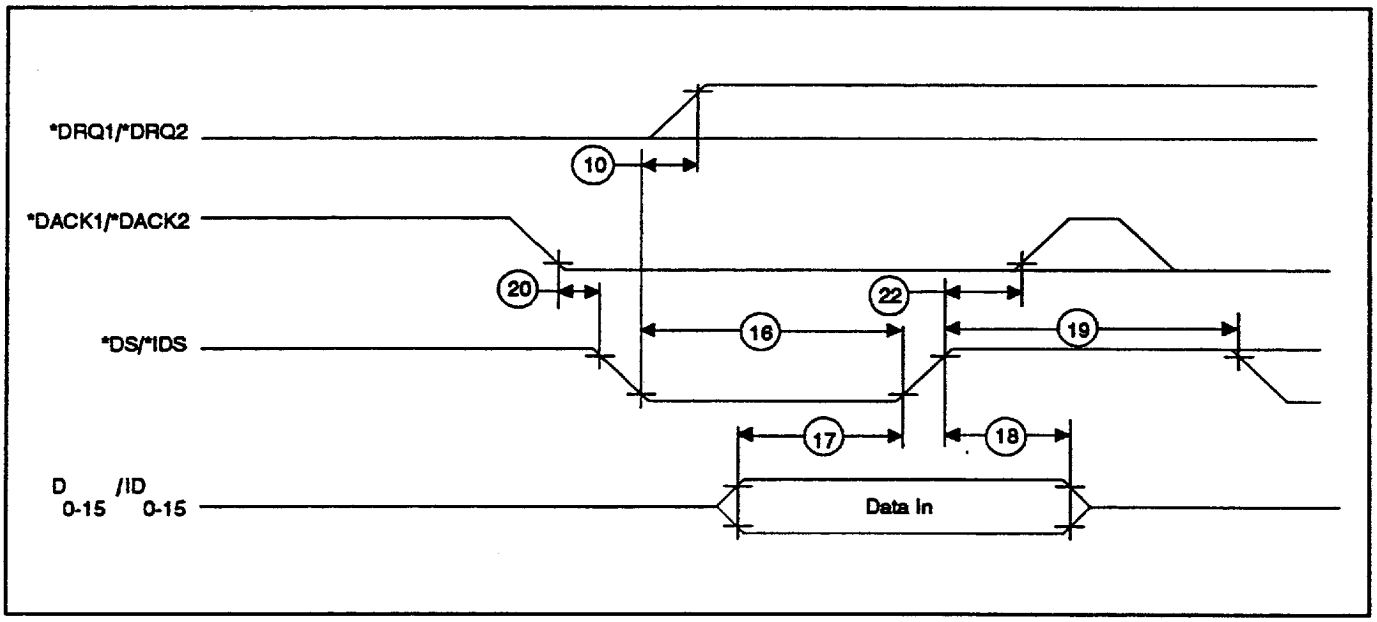


CPU Flow-Through Write Timing

SWITCHING WAVEFORMS

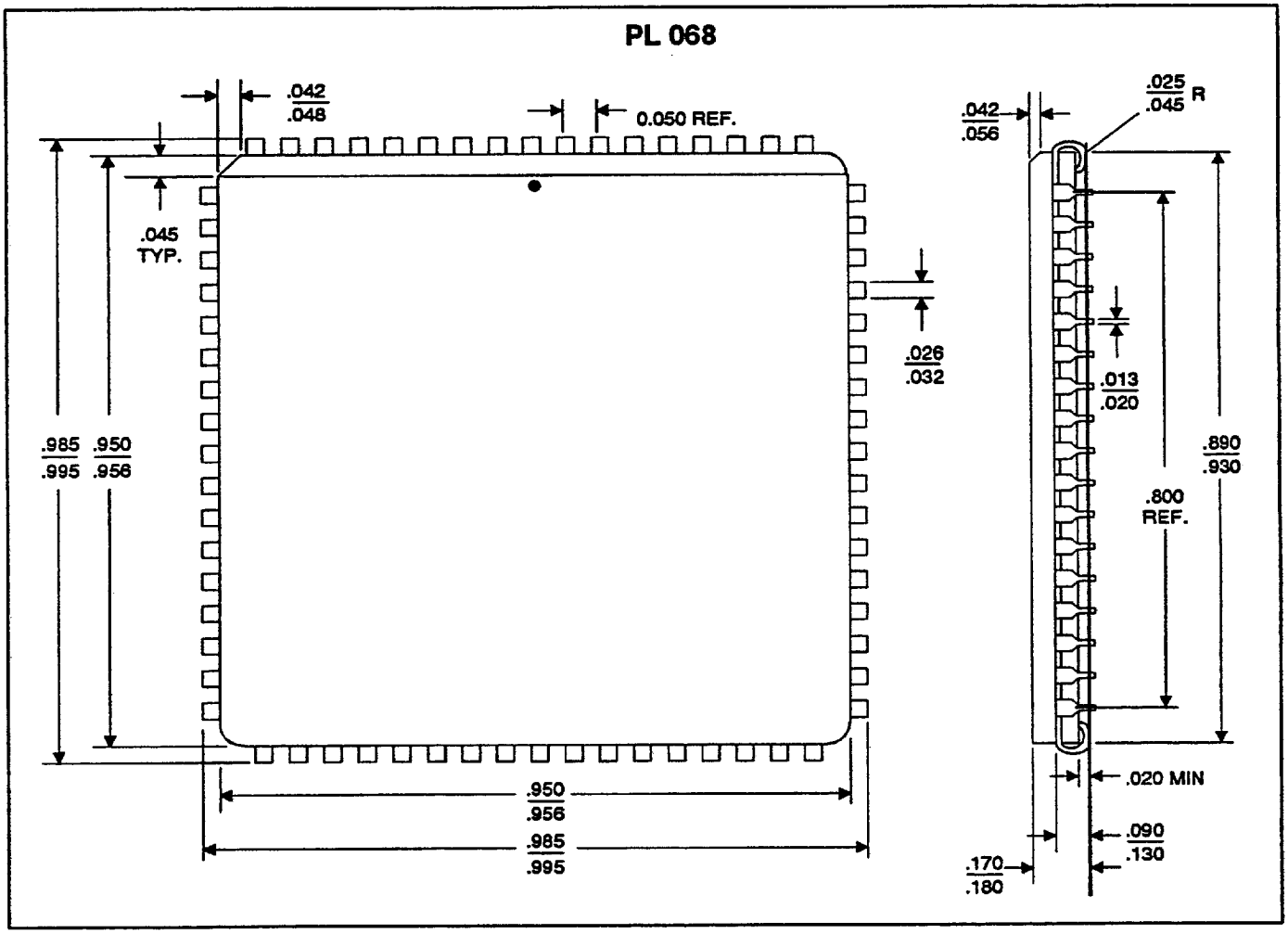


DMA Fly-by Read Timing



DMA Fly-by Write Timing

PHYSICAL DIMENSIONS



SWITCHING WAVEFORM