PCMCIA Flash Memory Card *1 MEGABYTE through 40 MEGABYTE (Intel/Sharp based)*

General Description

WEDC's FLA Series Flash memory cards offer high density linear Flash solid state storage solutions for code and data storage, high performance disk emulation and execute in place (XIP) applications in mobile PC and dedicated (embedded) equipment.

FLA series cards conform to PCMCIA international standard.

The card's control logic provides the system interface and controls the internal Flash memories. Card can be read/written in byte-wide or word-wide mode which allows for flexible integration into various systems. Combined with file management software, such as Flash Translation Layer (FTL), FLA Flash cards provide removable high-performance disk emulation.

The FLA series offers low power modes controlled by registers. Standard cards contain separate 2kB EEPROM memory for Card Information Structure (CIS) which can be used for easy identification of card characteristics.

The WEDC FLA series is based on Intel/Sharp Flash memories.

Note:
Standard options include attribute memory. Cards without attribute memory are available. Cards are also available with or without a hardware write protect switch.

Features

- Low cost High Density Linear Flash Card
- Supports 5V only systems or 5V systems with 12V VPP
- Based on Intel/Sharp FlashFile Components
- Fast Read Performance
  - 150ns or 200ns Maximum Access Time
- x8 / x16 Data Interface
- High Performance Random Writes
  - 8µs Typical Word Write Time
- Automated Write and Erase Algorithms
  - Command User Interface
- 100,000 Erase Cycles per Block
- 64K word symmetrical Block Architecture
- PC Card Standard Type I Form Factor

Architecture Overview

WEDC's FLA series is designed to support from 2 to 20, 4Mb, 8Mb or 16Mb components, providing a wide range of density options. Cards are based on the 28F008SA (8Mb) for 12V VPP applications or on the 28F004S5 (4Mb), 28F008S5 (8Mb) and 28F016S5 (16Mb) devices for 5V only applications. Devices codes for the 28F004S5, 28F008SA, 28F008S5 and the 28F016S5 are: A7H, A2H, A6H and AAh respectively. Systems should be able to recognize all four codes. Cards utilizing the 8Mb components provide densities ranging from 2MB to 20MB in 2MB increments, cards utilizing 16Mb components provide densities ranging from 4MB to 40MB in 4MB increments. 4 Mbit memory devices are used only for smallest capacity cards (1MB).

In support of the PC Card 95 standard for word wide access devices are paired. Therefore, the Flash array is structured in 64K word (128kBytes) blocks. Write, read and block erase operations can be performed as either a word or byte wide operation . By multiplexing A0, CE1# and CE2#, 8-bit hosts can access all data on data lines DQ0 - DQ7.

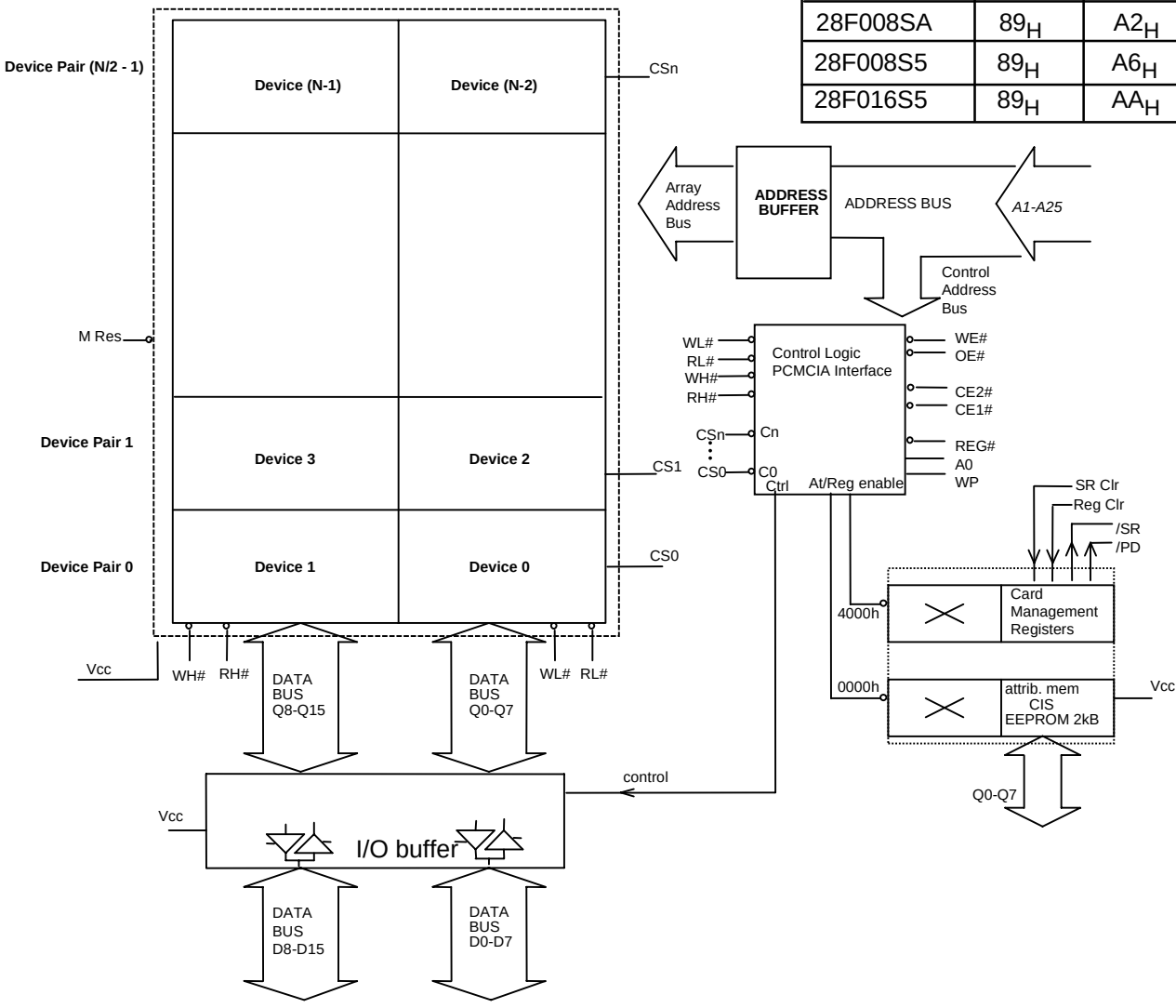
The FLA21-FLA36 series also supports the following PCMCIA compatible register functions: Soft Reset via the Configuration Option Register, Power Down (sleep mode) via the Configuration and Status Register and monitoring of Ready/Busy, Soft Reset and Power Down via the Card Status Register (cards without attribute memory and versions FLA51 - FLA66 do not have registers).

The FLA series cards conform with the PC Card Standard (PCMCIA) and JEIDA, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

WEDC's standard cards are shipped with WEDC's Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both a recessed (for label) and flat housing. Please contact WEDC sales representative for further information on Custom artwork.

Block Diagram

Device type	Manuf ID	Device ID
28F004S5	89_H	$A7_H$
28F008SA	89_H	$A2_H$
28F008S5	89_H	$A6_H$
28F016S5	89_H	AA_H



Registers in Attribute Memory Space

ADDRESS	Register NAME
4100h	Status Reg.
4002h	Config. and Status Reg.
4000h	Configuration Option Register

COR

Configuration Option Register: ADRS=4000h Write Only

SRES	LREQ	-Configuration Index-					
D7	*D6*	D5	D4	D3	D2	D1	D0

D7 Soft Reset, active High
1 = Reset State
0 = End Reset State
D6 LevelReq (not supported)
D5-D0 Configuration index (not supported)

CSR

Configuration Status Register: ADRS=4002h Write Only

not supported					PDwn	not supported	
D7	*D6*	*D5*	*D4*	*D3*	**D2**	*D1*	*D0*

D2 Power Down; active High
1=Place all memory devices in power down mode
0=normal operation Power On default=0

SR

Status Register: ADRS=4100h Read Only

not supported	SReset		PDwn	not supported		R/BSY
D7	*D6*	**D5**	D4	**D3**	*D2*	*D1*	**D0**

D5 Represents the state of SRESET bit in COR (4000h)
1=Reset
0=Normal operation
Power On default D5=0
D3 Represents the state of Power Down bit (D2) in CSR (4002h)
1=Power Down
D0 Reflects the card's Ready/Busy signal (pin 16) driven by memory components Ready/Busy outputs.This bit allows software polling of the card's Ready/Busy status.
1=Ready

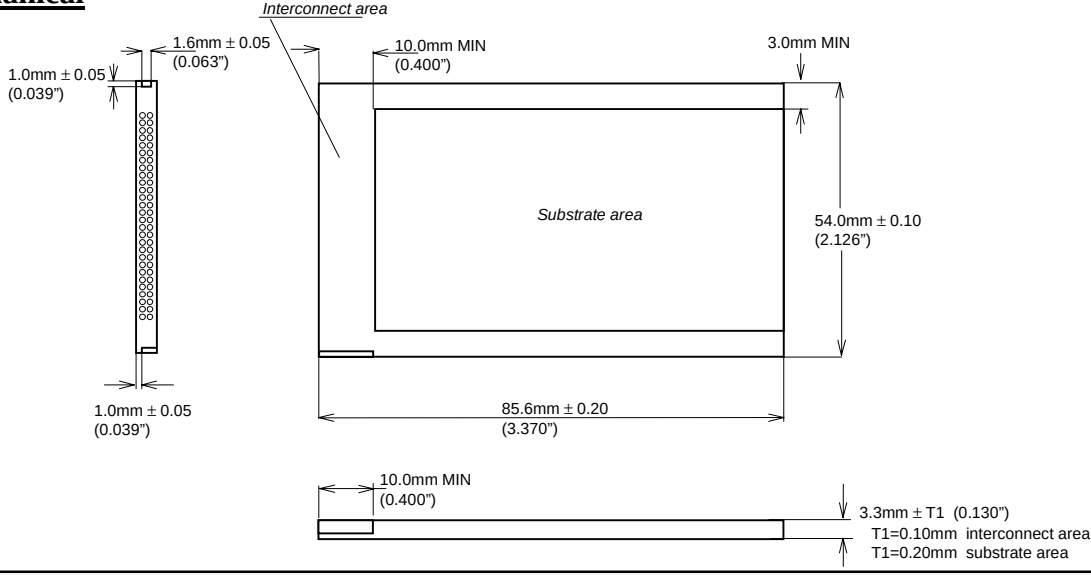
Pinout

Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#	I	Card enable 1	LOW
8	A10	I	Address bit 10	
9	OE#	I	Output enable	LOW
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready/Busy	LOW (4)
17	Vcc		Supply Voltage	
18	Vpp1		Prog. Voltage	N.C.
19	A16	I	Address bit 16	
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	CD1#	O	Card Detect 1	LOW
37	DQ11	I/O	Data bit 11	
38	DQ12	I/O	Data bit 12	
39	DQ13	I/O	Data bit 13	
40	DQ14	I/O	Data bit 14	
41	DQ15	I	Data bit 15	
42	CE2#	I	Card Enable 2	LOW
43	VS1	O	Voltage Sense 1	N.C.
44	RFU		Reserved	
45	RFU		Reserved	
46	A17	I	Address bit 17	
47	A18	I	Address bit 18	
48	A19	I	Address bit 19	
49	A20	I	Address bit 20	2MB(3)
50	A21	I	Address bit 21	4MB(3)
51	Vcc		Supply Voltage	
52	Vpp2		Prog. Voltage	N.C.
53	A22	I	Address bit 22	8MB(3)
54	A23	I	Address bit 23	16MB(3)
55	A24	I	Address bit 24	32MB(3)
56	A25	I	Address bit 25	64MB(3)
57	VS2	O	Voltage Sense 2	N.C.
58	RST	I	Card Reset	HIGH (4)
59	Wait#	O	Extended Bus cycle	Low(2,4)
60	RFU		Reserved	
61	REG#	I	Attrib Mem Select	
62	BVD2	O	Bat. Volt. Detect 2	(2)
63	BVD1	O	Bat. Volt. Detect 1	(2)
64	DQ8	I/O	Data bit 8	
65	DQ9	I/O	Data bit 9	
66	DQ10	O	Data bit 10	
67	CD2#	O	Card Detect 2	LOW
68	GND		Ground	

Notes:
1. RDY/BSY signal is an “Open drain” type output, pull-up resistor on host side is required.
2. Wait#, BVD1 and BVD2 are driven high for compatibility.
3. Shows density for which specified address bit is MSB. Higher order address bits are no connects (ie 4MB A21 is MSB A22 - A25 are NC).
4. NC - No Connection for FLA51 - FLA66.

Mechanical



Card Signal Description

Symbol	Type	Name and Function
A0 - A25	INPUT	**ADDRESS INPUTS:** A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not used in word access mode. A25 is the most significant bit
DQ0 - DQ15	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ15 is the MSB.
CE1#, CE2#	INPUT	**CARD ENABLE 1 AND 2:** CE1# enables even byte accesses, CE2# enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows 8-bit hosts to access all data on DQ0 - DQ7.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or program algorithms. A high output indicates that the card is ready to accept accesses. A low output indicates that one or more devices in the memory card are busy with internally timed erase or write activities.
CD1#, CD2#	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are internally connected to ground on the card. The host shall monitor these signals to detect card insertion (pulled-up on host side).
WP	OUTPUT	**WRITE PROTECT:** Write protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the Flash array. If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = "off".
VPP1, VPP2	N.C.	**PROGRAM/ERASE POWER SUPPLY:** Provides programming voltages for card (12V). Not connected for 5V only card.
VCC		**CARD POWER SUPPLY:** (5.0V).
GND		**CARD GROUND**
REG#	INPUT	**ATTRIBUTE MEMORY SELECT :** Active low signal, enables access to Attribute Memory Plane, occupied by Card Information Structure and Card Registers.
RST	INPUT	**RESET:** Active high signal for placing card in Power-on default state. Reset can be used as a Power-Down signal for the memory array.
WAIT#	OUTPUT	**WAIT:** This signal is pulled high internally for compatibility. No wait states are generated.
BVD1, BVD2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are pulled high to maintain SRAM card compatibility.
VS1, VS2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's VCC requirements. VS1 and VS2 are open to indicate a 5V card .
RFU		**RESERVED FOR FUTURE USE**
N.C.		**NO INTERNAL CONNECTION TO CARD:** pin may be driven or left floating

Functional Truth Table

READ function

Function Mode	/CE2	/CE1	A0	/OE	/WE	Common Memory /REG	Common Memory D15-D8	Common Memory D7-D0	Attribute Memory /REG	Attribute Memory D15-D8	Attribute Memory D7-D0
Standby Mode	H	H	X	X	X	X	High-Z	High-Z	X	High-Z	High-Z
Byte Access (8 bits)	H	L	L	L	H	H	High-Z	Even-Byte	L	High-Z	Even-Byte
	H	L	H	L	H	H	High-Z	Odd-Byte	L	High-Z	Not Valid
Word Access (16 bits)	L	L	X	L	H	H	Odd-Byte	Even-Byte	L	Not Valid	Even-Byte
Odd-Byte Only Access	L	H	X	L	H	H	Odd-Byte	High-Z	L	Not Valid	High-Z

WRITE function

Standby Mode	H	H	X	X	X	X	X	X	X	X	X
Byte Access (8 bits)	H	L	L	H	L	H	X	Even-Byte	L	X	Even-Byte
	H	L	H	H	L	H	X	Odd-Byte	L	X	X
Word Access (16 bits)	L	L	X	H	L	H	Odd-Byte	Even-Byte	L	X	Even-Byte
Odd-Byte Only Access	L	H	X	H	L	H	Odd-Byte	X	L	X	X

Absolute Maximum Ratings (1)

Operating Temperature TA (ambient)	
Commercial	0°C to +60 °C
Industrial	-40°C to +85 °C
Storage Temperature	
Commercial	-30°C to +80 °C
Industrial	-40°C to +85 °C
Voltage on any pin relative to VSS	-0.5V to VCC+0.5V
VCC supply Voltage relative to VSS	-0.5V to +7.0V

Note:
(1) Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics (1)

Symbol	Parameter	Density (Mbytes)	Notes	Typ(3)	Max	Units	Test Conditions
I_{CCR}	VCC Read Current	All			35	mA	VCC = VCCmax tcycle = 150ns,CMOS levels
I_{CCW}	VCC Program Current	All	28F008S5 28F016S5		75	mA	
I_{CCW}	VCC Program Current	All	28F008SA		30	mA	
I_{PPW}	VPP Program Current	All	Vpp=12V		30	mA	
I_{CCE}	VCC Erase Current	All			100	mA	
I_{CCS} (CMOS)	VCC Standby Current	2MB	2 28F008SA	110	230	µA	VCC = VCCmax Control Signals = VCC Reset = VSS, CMOS levels
		20MB		900			
		2MB	2 28F008S5	60			
		20MB		420			
		4MB	2 28F016S5	60			
		40MB		380			

CMOS Test Conditions: VCC = 5V ± 5%, VIL = VSS ± 0.2V, VIH = VCC ± 0.2V

Notes:
1. All currents are RMS values unless otherwise specified. ICCR, ICCW and ICCE are based on Byte wide operations. For 16 bit operation values are double.
2. Control Signals: CE_1#, CE_2#, OE#, WE#, REG#.
3. Typical: VCC = 5V, T = +25C.

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current	1		±20	µA	VCC = VCCMAX Vin =VCC or VSS
I_{LO}	Output Leakage Current	1		±20	µA	VCC = VCCMAX Vout =VCC or VSS
V_{IL}	Input Low Voltage	1	0	0.8	V	
V_{IH}	Input High Voltage	1	0.7VCC	VCC+0.5	V	
V_{OL}	Output Low Voltage	1		0.4	V	IOL = 3.2mA
V_{OH}	Output High Voltage	1	VCC-0.4	VCC	V	IOH = -2.0mA
V_{LKO}	VCC Erase/Program Lock Voltage	1	2.0		V	

Notes:
1. Values are the same for byte and word wide modes for all card densities.
2. Exceptions: Leakage currents on CE1#, CE2#, OE#, REG# and WE# will be < 500 µA when VIN = GND due to internal pull-up resistors. Leakage currents on RST will be <150µA when VIN=VCC due to internal pull-down resistor.

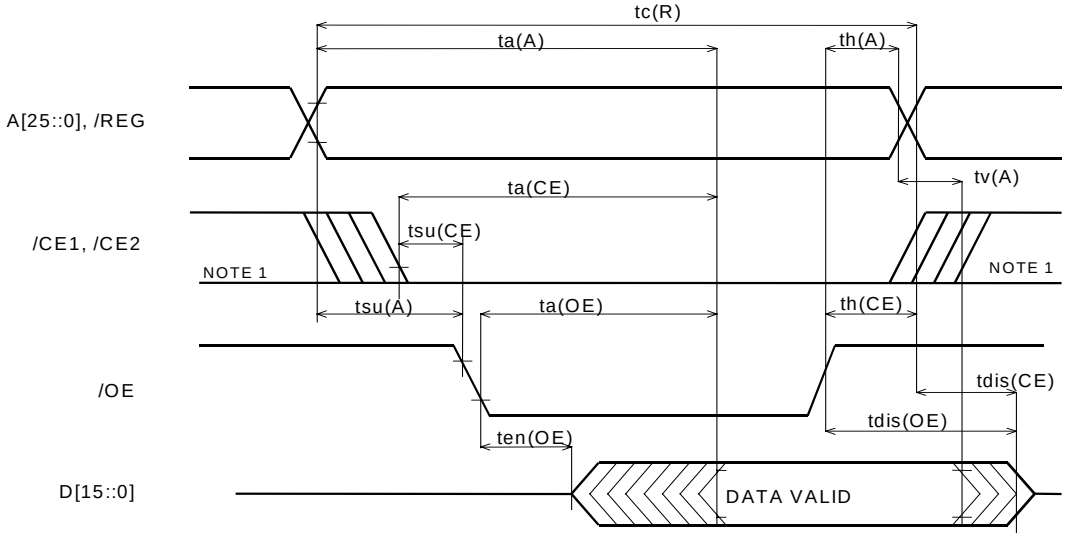
AC Characteristics

Read Timing Parameters

		150ns		
SYMBOL (PCMCIA)	**Parameter**	**Min**	**Max**	**Unit**
t_c(R)	Read Cycle Time	150		ns
t_a(A)	Address Access Time		150	ns
t_a(CE)	Card Enable Access Time		150	ns
t_a(OE)	Output Enable Access Time		75	ns
t_{su}(A)	Address Setup Time		20	ns
t_{su}(CE)	Card Enable Setup Time		0	ns
t_h(A)	Address Hold Time		20	ns
t_h(CE)	Card Enable Hold Time		20	ns
t_v(A)	Output Hold from Address Change		0	ns
t_{dis}(CE)	Output Disable Time from CE#		75	ns
t_{dis}(OE)	Output Disable Time from OE#		75	ns
t_{en}(CE)	Output Enable Time from CE#	5		ns
t_{en}(OE)	Output Enable Time from OE#	5		ns
t_{rec}(RSR)	Power Down recovery to Output Delay. VCC = 5V		500	ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Read Timing Diagram



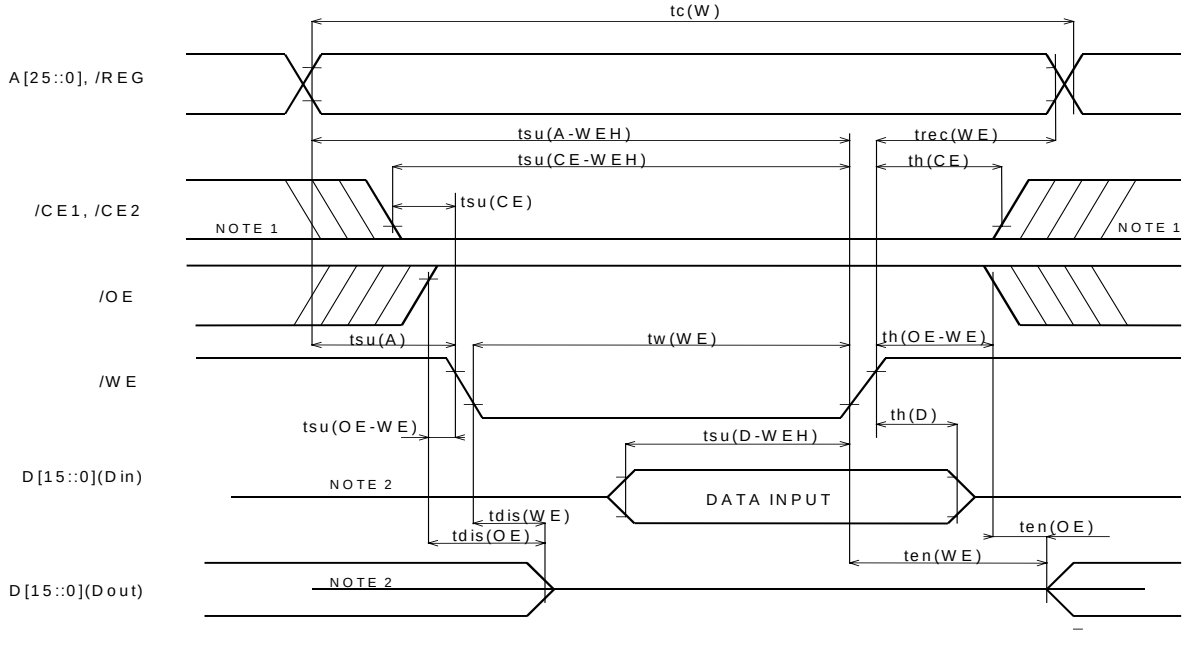
Note: Signal may be high or low in this area.

Write Timing Parameters

		150ns		
SYMBOL (PCMCIA)	**Parameter**	**Min**	**Max**	**Unit**
t_CW	Write Cycle Time	150		ns
t_w(WE)	Write Pulse Width	80		ns
t_{su}(A)	Address Setup Time	20		ns
t_{su}(A-WEH)	Address Setup Time for WE#	100		ns
t_{su}(CE-WEH)	Card Enable Setup Time for WE#	100		ns
t_{su}(D-WEH)	Data Setup Time for WE#	50		ns
t_h(D)	Data Hold Time	20		ns
t_{rec}(WE)	Write Recover Time	20		ns
t_{dis}(WE)	Output Disable Time from WE#		75	ns
t_{dis}(OE)	Output Disable Time from OE#		75	ns
t_{en}(WE)	Output Enable Time from WE#	5		ns
t_{en}(OE)	Output Enable Time from OE#	5		ns
t_{su}(OE-WE)	Output Enable Setup from WE#	10		ns
t_h(OE-WE)	Output Enable Hold from WE#	10		ns
t_{su}(CE)	Card Enable Setup Time from OE#	0		ns
t_h(CE)	Card Enable Hold Time	20		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Write Timing Diagram



Notes:
1. Signal may be high or low in this area
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.

Data Write and Erase Performance (1,3)

VCC = 5V ± 5%, T_A = 0C to + 70C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units
t_{WHQV1} t_{EHQV1}	Word/Byte Program time	4		8		µs
t_{WHQV2} t_{EHQV2}	Block Program Time	device SA		0.6	2.1	sec
		device S5	0.4	0.5		
	Block Erase Time	device SA		1.6	10	sec
		device S5	0.9	1.1		

Notes:
1. Typical: Nominal voltages and T_A = 25C.
2. Excludes system overhead.
3. Valid for all speed options.
4. To maximize system performance RDY/BSY# signal should be polled.

PRODUCT MARKING

WED 7P016FLA6200C15 C995 9915

- **EDI** — Company Name
- **7P016FLA6200C15** — Part number
- **C995** — Lot code / trace number
- **9915** — Date code

Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.

PART NUMBERING

7 P 016 FLA62 00 C 15

Card access time

15	150ns
25	250ns

Temperature range

C	Commercial	0°C to +70°C
I	Industrial	-40°C to +85°C

Packaging option

00	Standard, type 1

Card family and version

- See Card Family and Version Info. for details (next page)

Card capacity

016	16MB

PC card

P	Standard PCMCIA
R	Ruggedized PCMCIA

Card technology

7	FLASH
8	SRAM

Card Family and Version Information

FLA21-FLA24 Based on **28F008SA** (requires 12V VPP for programming and erase functions)

FLA21	No Attribute Memory, no Write Protect
FLA22	With Attribute Memory, no Write Protect
FLA23	No Attribute Memory, with Write Protect
FLA24	With Attribute Memory, with Write Protect

Example P/N **7P004FLA2200C15**

FLA25-FLA28 Based on **28F008S5** for 5V only applications

FLA25	No Attribute Memory, no Write Protect
FLA26	With Attribute Memory, no Write Protect
FLA27	No Attribute Memory, with Write Protect
FLA28	With Attribute Memory, with Write Protect

Example P/N **7P004FLA2600C15**

FLA29-FLA32 Based on **28F016S5** for 5V only applications

FLA29	No Attribute Memory, no Write Protect
FLA30	With Attribute Memory, no Write Protect
FLA31	No Attribute Memory, with Write Protect
FLA32	With Attribute Memory, with Write Protect

Example P/N **7P004FLA3000C15**

FLA33-FLA36 Based on **28F004S5** for 5V only applications

FLA33	No Attribute Memory, no Write Protect
FLA34	With Attribute Memory, no Write Protect
FLA35	No Attribute Memory, with Write Protect
FLA36	With Attribute Memory, with Write Protect

Example P/N **7P004FLA3600C15**

FLA51-FLA54 Based on **28F008SA** Similar to FLA21-FLA24: does not support registers and signals RST, RDY/BSY, Wait are not connected

FLA51	No Attribute Memory, no Write Protect
FLA52	With Attribute Memory, no Write Protect
FLA53	No Attribute Memory, with Write Protect
FLA54	With Attribute Memory, with Write Protect

Example P/N **7P004FLA5200C15**

FLA55-FLA58 Based on **28F008S5** Similar to FLA25-FLA28: does not support registers and signals RST, RDY/BSY, Wait are not connected

FLA55	No Attribute Memory, no Write Protect
FLA56	With Attribute Memory, no Write Protect
FLA57	No Attribute Memory, with Write Protect
FLA58	With Attribute Memory, with Write Protect

Example P/N **7P004FLA5600C15**

FLA59-FLA62 Based on **28F016S5** Similar to FLA29-FLA32: does not support registers and signals RST, RDY/BSY, Wait are not connected

FLA59	No Attribute Memory, no Write Protect
FLA60	With Attribute Memory, no Write Protect
FLA61	No Attribute Memory, with Write Protect
FLA62	With Attribute Memory, with Write Protect

Example P/N **7P004FLA6000C15**

FLA63-FLA66 Based on **28F004S5** Similar to FLA33-FLA36: does not support registers and signals RST, RDY/BSY, Wait are not connected

FLA63	No Attribute Memory, no Write Protect
FLA64	With Attribute Memory, no Write Protect
FLA65	No Attribute Memory, with Write Protect
FLA66	With Attribute Memory, with Write Protect

Example P/N **7P004FLA6600C15**

Ordering Information

7P XXX FLAYY SS T ZZ

where

XXX:	**002** [1]	**2MB**
	004	**4MB**
	006 [1]	**6MB**
	008	**8MB**
	010 [1]	**10MB**
	012	**12MB**
	014 [1]	**14MB**
	016	**16MB**
	018 [1]	**18MB**
	020	**20MB**
	024 [2]	**24MB**
	028 [2]	**28MB**
	032 [2]	**32MB**
	036 [2]	**36MB**
	040 [2]	**40MB**

[1] available only for FLA21-FLA24, FLA25-FLA28, FLA51-FLA54, and FLA55-FLA59
[2] available only for FLA29-FLA32 and FLA59-FLA62

FLAYY: **Card Family and Version (See Card Family and Version Information)**

SS:	**00**	**WEDC Logo Silkscreen**	
	01	**Blank Housing, Type I**	
	02	**Blank Housing, Type I Recessed**	
T:	**C**	**Commercial**	**0°C to +70°C**
	I**	**Industrial**	**-40°C to +85°C**
ZZ:	**15**	**150ns**	

Notes: Options without attribute memory and with hardware write protect switch are available.

** Denotes advanced information.

CIS Information for FLA Series Cards

Address	Value	Description
00H	**01H**	**CISTPL_DEVICE**
02H	**03H**	TPL_LINK
04H	**53H**	FLASH = 150ns (device writable)
06H	**06H**	CARD SIZE: 2MB
	0EH	4MB
	16H	6MB
	1EH	8MB
	26H	10MB
	2EH	12MB
	36H	14MB
	3EH	16MB
	46H	18MB
	4EH	20MB
	5EH	24MB
	6EH	28MB
	7EH	32MB
	8EH	36MB
	9EH	40MB
08H	**FFH**	END OF DEVICE
0AH	**18H**	**CISTPL_JEDEC_C**
0CH	**02H**	TPL_LINK
0EH	**89H**	INTEL - ID
10H	**A2H**	INTEL 28F008SA - ID
	A6H	INTEL 28F008S5 - ID
	AAH	INTEL 28F016S5 - ID
12H	**17H**	**CISTPL_DEVICE_A**
14H	**03H**	TPL_LINK
16H	**42H**	EEPROM - 200ns
18H	**01H**	Device Size = 2KBytes
1AH	**FFH**	END OF TUPLE
1CH	**1EH**	**CISTPL_DEVICEGEO**
1EH	**06H**	TPL_LINK
20H	**02H**	DGTPL_BUS
22H	**11H**	DGTPL_EBS
24H	**01H**	DGTPL_RBS
26H	**01H**	DGTPL_WBS
28H	**01H**	DGTPL_PART
2AH	**01H**	FLASH DEVICE
		NON-INTERLEAVED
2CH	**20H**	**CISTPL_MANFID**
2EH	**04H**	TPL_LINK(04H)

Address	Value	Description
30H	**F6H**	**EDI** TPLMID_MANF: LSB
32H	**01H**	**EDI** TPLMID_MANF: MSB
34H	**00H**	*LSB: Number Not Assigned*
36H	**00H**	*MSB: Number Not Assigned*
38H	**15H**	**CISTPL_VERS1**
3AH	**47H**	TPL_LINK
3CH	**05H**	TPLLV1_MAJOR
3EH	**00H**	TPLLV1_MINOR
40H	**45H**	E
42H	**44H**	D
44H	**49H**	I
46H	**37H**	7
48H	**50H**	P
4AH	**30H**	0
4CH		*x*
4EH		*x*
50H	**46H**	F
52H	**4CH**	L
54H	**41H**	A
56H	**32H**	2 based on
58H	**32H**	2 28F008SA
	32H	2 based on
	36H	6 28F008S5
	33H	3 based on
	30H	0 28F016S5
5AH	**2DH**	-
5CH	**2DH**	-
5EH	**2DH**	-
60H	**31H**	1
62H	**35H**	5
64H	**20H**	SPACE
66H	**00H**	END TEXT
68H	**43H**	C
6AH	**4FH**	O
6CH	**50H**	P
6EH	**59H**	Y
70H	**52H**	R
72H	**49H**	I
74H	**47H**	G
76H	**48H**	H
78H	**54H**	T
7AH	**20H**	SPACE

CIS Information for FLA Series Cards (Cont.)

Address	Value	Description
7CH	**45H**	E
7EH	**4CH**	L
80H	**45H**	E
82H	**43H**	C
84H	**54H**	T
86H	**52H**	R
88H	**4FH**	O
8AH	**4EH**	N
8CH	**49H**	I
8EH	**43H**	C
90H	**20H**	SPACE
92H	**44H**	D
94H	**45H**	E
96H	**53H**	S
98H	**49H**	I
9AH	**47H**	G
9CH	**4EH**	N
9EH	**53H**	S
A0H	**20H**	SPACE
A2H	**49H**	I
A4H	**4EH**	N
A6H	**43H**	C
A8H	**4FH**	O
AAH	**52H**	R
ACH	**50H**	P
AEH	**4FH**	O
B0H	**52H**	R
B2H	**41H**	A
B4H	**54H**	T
B6H	**45H**	E
B8H	**44H**	D
BAH	**20H**	SPACE
BCH	**00H**	END TEXT
BEH	**31H**	1
C0H	**39H**	9
C2H	**39H**	9
C4H	**37H**	7
C6H	**00H**	END TEXT
C8H	**FFH**	END OF LIST
CAH	**1AH**	**CISTPL_CONF**
CCH	**05H**	TPL_LINK
CEH	**01H**	TPCC_SZ
D0H	**00H**	TPCC_LAST
D2H	**00H**	TPCC_RADR
D4H	**40H**	TPCC_RADR
D6H	**03H**	TPCC_RMSK
D8H	**00H**	NULL CONTROL TUPLE
DAH	**FFH**	**CISTPL_END**
DCH	**00H**	INVALID ADDRESS

Revision History:

rev level	*description*	*date*
rev 0	**initial release**	**May 26, 1998**
rev 1	**Logo change**	**May 27, 1999**
rev 2	**Change in Ordering info: added FLA24, took "EDI" off of all part numbers, changed "EDI Silkscreen" to "WEDC Logo Silkscreen"**	**January 31, 2000**
rev 3	**Heading/Logo changed and added to all pages Changes to Pages 1 & 12 Pages 9-11: Added Product Marking Info, added Family and Version Information, edited Ordering Info, edited General description and edited Architecture Overview**	**May 30, 2000**
rev 4	**Corrected Errors on pgs. 6 & 7**	**August 1, 2000**

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