

P4C1257

ULTRA HIGH SPEED 256K x 1

STATIC CMOS RAMS (SCRAMS)

★ FEATURES

- High Speed (Equal Access and Cycle Times)
 - 25/35 ns (Commercial)
 - 25/35/45/55 ns (Military)
- Low Power (Commercial/Military)
 - 605/660 mW Active – 25/35/45/55
 - 193/220 mW Standby (TTL Input)
 - 138/193 mW Standby (CMOS Input) P4C1257
- Single 5V±10% Power Supply
- Separate Data I/O
- Three-State Output
- TTL/CMOS Compatible Output
- Fully TTL Compatible Inputs
- Produced with PACE II Technology™
- Standard Pinout (JEDEC Approved)
 - 24-Pin 300 mil DIP, SOJ

★ DESCRIPTION

The P4C1257 is a 262,144-bit ultra high-speed CMOS static RAM organized as 256Kx1. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply.

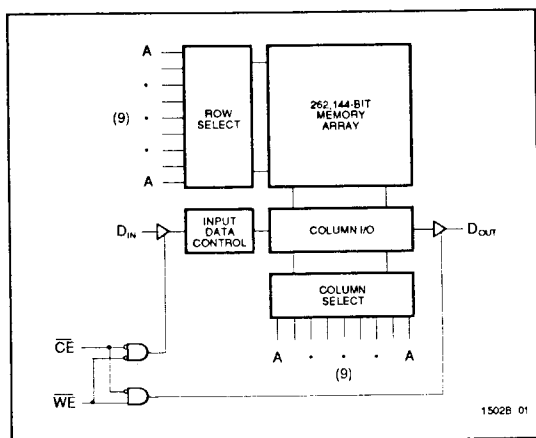
Access times as fast as 25 nanoseconds permit greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low level in both active and standby modes. The P4C1257 is a member of a family of PACE RAM™ products offering super fast access times never before available at these complexity levels in TTL-compatible bipolar or CMOS technologies.

The P4C1257 is manufactured using PACE II Technology which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths giving 400 picoseconds loaded* internal gate delays. PACE II Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

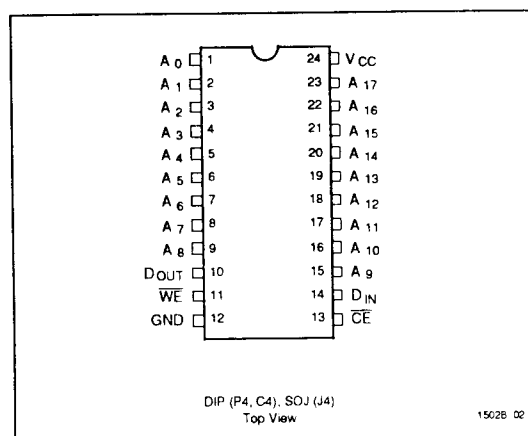
The P4C1257 is available in 24-pin 300 mil DIP and SOJ packages.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

★ FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to $V_{CC} + 0.5$	V
T_A	Operating Temperature	-55 to +125	°C

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Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

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RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade ⁽²⁾	Ambient Temperature	GND	V_{CC}
Military	-55 to +125°C	0V	5.0V ± 10%

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Grade ⁽²⁾	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICSOver recommended operating temperature and supply voltage⁽²⁾

Symbol	Parameter	Test Conditions	P4C1257		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.2	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5 ⁽³⁾	0.8	V
V_{HC}	CMOS Input High Voltage		$V_{CC} - 0.2$	$V_{CC} + 0.5$	V
V_{LC}	CMOS Input Low Voltage		-0.5 ⁽³⁾	0.2	V
V_{CD}	Input Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-1.2	V
V_{OL}	Output Low Voltage (TTL Load)	$I_{OL} = +8 \text{ mA}, V_{CC} = \text{Min.}$		0.4	V
V_{OLC}	Output Low Voltage (CMOS Load)	$I_{OLC} = +100 \mu\text{A}, V_{CC} = \text{Min.}$		0.2	V
V_{OH}	Output High Voltage (TTL Load)	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min.}$	2.4		V
V_{OHC}	Output High Voltage (CMOS Load)	$I_{OHC} = -100 \mu\text{A}, V_{CC} = \text{Min.}$	$V_{CC} - 0.2$		V
I_{LI}	Input Leakage Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND to } V_{CC}$	Mil. -10 Com'l. -5	+10 +5	μA
I_{LO}	Output Leakage Current	$V_{CC} = \text{Max.}, CE = V_{IH}$ $V_{OUT} = \text{GND to } V_{CC}$	Mil. -10 Com'l. -5	+10 +5	μA

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CAPACITANCES⁽⁴⁾ $(V_{CC} = 5.0\text{V}, T_A = 25^\circ\text{C}, f = 1.0\text{MHz})$

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	5	pF

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Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	7	pF

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Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V_{IL} and I_{IL} not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20 ns.
- This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS

Over recommended operating temperature and supply voltage⁽²⁾

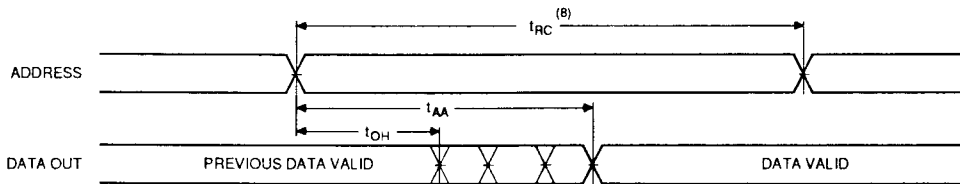
Symbol	Parameter	Test Conditions	P4C1257		Unit
			Min	Max	
I_{CC}	Dynamic Operating Current – 25, 35, 45, 55	$V_{CC} = \text{Max.}, f = \text{Max.},$ Mil. Outputs Open Com'l.	—	120	mA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH}$ Mil. $V_{CC} = \text{Max.},$ Com'l. $f = \text{Max.},$ Outputs Open	—	40	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{HC}$ Mil. $V_{CC} = \text{Max.},$ Com'l. $f = 0,$ Outputs Open, $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	—	35	mA
			—	25	

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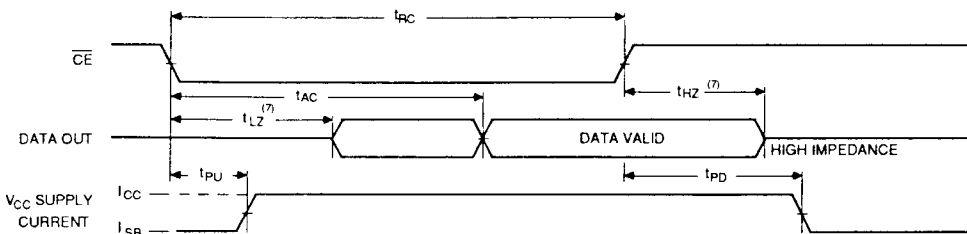
AC CHARACTERISTICS—READ CYCLE(V_{CC} = 5V ± 10%, All Temperature Ranges)⁽²⁾

Symbol	Parameter	-25		-35		-45		-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{RC}	Read Cycle Time	25		35		45		55		ns
t _{AA}	Address Access Time		25		35		45		55	ns
t _{AC}	Chip Enable Access Time		25		35		45		55	ns
t _{OH}	Output Hold from Address Change	3		3		3		3		ns
t _{LZ}	Chip Enable to Output in Low Z	3		3		3		3		ns
t _{HZ}	Chip Disable to Output in High Z		12		17		20		25	ns
t _{PU}	Chip Enable to Power Up Time	0		0		0		0		ns
t _{PD}	Chip Disable to Power Down Time		25		35		45		55	ns

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TIMING WAVEFORM OF READ CYCLE NO. 1 ⁽⁶⁾

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TIMING WAVEFORM OF READ CYCLE NO. 2 ⁽⁶⁾

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Notes:

5. $\overline{CE}$ is low and $\overline{WE}$ is high for READ cycle.
6. $\overline{WE}$ is high, and address must be valid prior to or coincident with $\overline{CE}$ transition low.
7. Transition is measured $\pm 200\text{mV}$ from steady state voltage prior to change with specified loading in Figure 1. This parameter is sampled and not 100% tested.
8. Read Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS—WRITE CYCLE

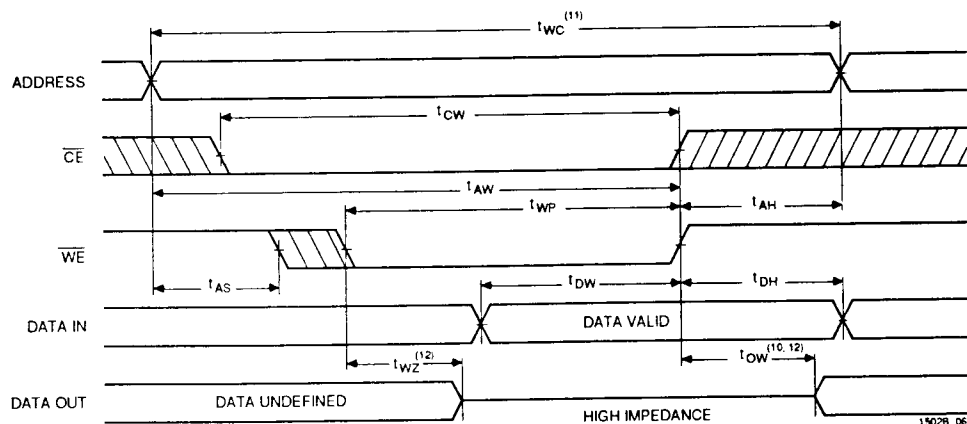
($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

Symbol	Parameter	-25		-35		-45		-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	25		35		45		55		ns
t_{CW}	Chip Enable Time to End of Write	20		25		35		45		ns
t_{AW}	Address Valid to End of Write	20		25		35		45		ns
t_{AS}	Address Set-up Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	20		25		25		35		ns
t_{AH}	Address Hold Time from End of Write	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	15		15		20		25		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		15		15		20		25	ns
t_{OW}	Output Active from End of Write	3		3		3		3		ns

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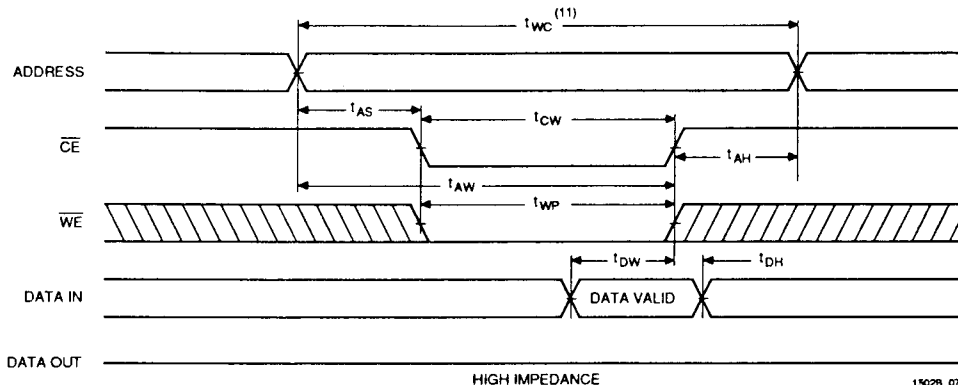
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)⁽⁹⁾



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Notes:

9. $\overline{CE}$ and $\overline{WE}$ must be LOW for WRITE cycle.
10. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
11. Write Cycle Time is measured from the last valid address to the first transition address.
12. Transition is measured $\pm 200mV$ from steady state voltage prior to change with specified loading in Figure 1. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CE}}$ CONTROLLED) ⁽⁹⁾

AC TEST CONDITIONS

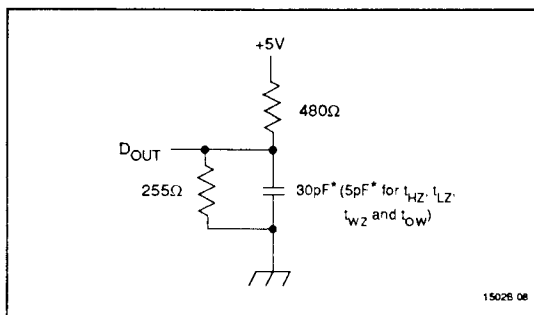
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

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TRUTH TABLE

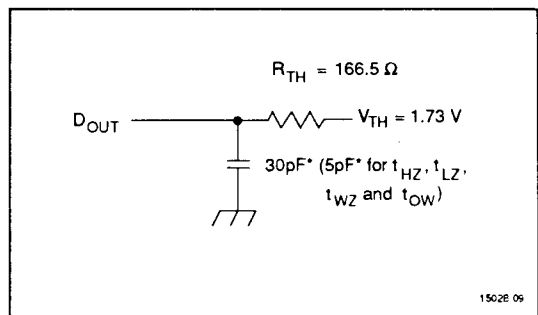
Mode	$\overline{\text{CE}}$	$\overline{\text{WE}}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

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Figure 1. Output Load



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Figure 2. Thevenin Equivalent

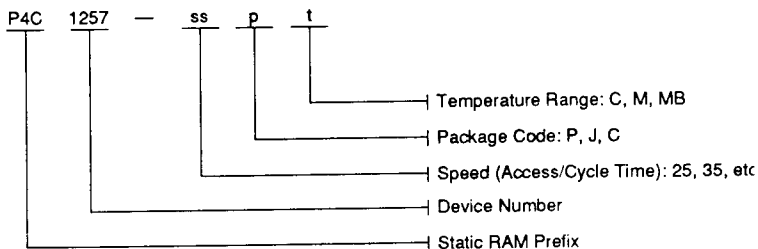
* including scope and test fixture.

Note:

Because of the ultra-high speed of the P4C1257, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50 Ω test environment should be terminated into a 50 Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116 Ω resistor must be used in series with D_{OUT} to match 166 Ω (Thevenin Resistance).

ORDERING INFORMATION

The following part numbering scheme is used for



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PACKAGE SUFFIX

Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
J	Plastic SOJ, 300 mil wide standard
C	Sidebrazed DIP, 300 mil wide standard

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TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C to +70°C.
M	Military Temperature Range, -55°C to +125°C.
MB	Mil. Temp. with MIL-STD-883D Class B compliance

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SELECTION GUIDE

The P4C1257 is available in the following temperature, speed and package options.

Temperature Range	Package \ Speed	25	35	45	55
Commercial	Plastic DIP	-25PC	-35PC	N/A	N/A
	Plastic SOJ	-25JC	-35JC	N/A	N/A
	Sidebrazed DIP	-25CC	-35CC	N/A	N/A
Military Temperature	Sidebrazed DIP	-25CM	-35CM	-45CM	-55CM
Military Processed*	Sidebrazed DIP	-25CMB	-35CMB	-45CMB	-55CMB

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* Military temperature range with MIL-STD-883 Revision D, Class B processing.

N/A = Not available