REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	Pages 1, 2, 3, 4, 14, 15, 16, editorial changes. Pages 5, 6, 7, 8, symbol corrections. Page 18, added vendor.	9 Dec 81	
B	Add device type 03. Type 02 inactive for new design: Use MIL-M-38510/52002 for case Q. Types 01 and new type 03 are still active.	6 Apr 83	
C	Add device types 04 and 05.	31 Oct 84	
D	Case temperature to +125°C. Add L_{CC} package, electrical test improvements.	12 Nov 85	
E	Change to military drawing format. Add device type 06, changes to 1.4, add vendor CAGE number 66958, delete vendor CAGE number 34335, changes to table I, changes to figures 1, 2, and 3. Editorial changes throughout. Change Code Ident. No. to 67268.	17 Dec 87	

CURRENT CAGE CODE 67268

REV	E	E	E	E																					
PAGE	24	25	26	27																					

REV STATUS OF PAGES	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
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Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
21 July 1980

AMSC N/A

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SIZE: A | CODE IDENT. NO.: 14933

REV: E

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROPROCESSOR, 16-BIT N-CHANNEL, SINGLE CHIP, MICROCIRCUIT, SILICON GATE

DWG NO. 80003

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5962-E428

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DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

80003	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit	Case outline
01	Z8001	4.0 MHz	X, U, Z
02	Z8002	4.0 MHz	Q, Y
03	Z8001A	6.0 MHz	X, U, Z
04	Z8001B	10 MHz	X, U, Z
05	Z8002B	10 MHz	Q, Y
06	Z8002A	6.0 MHz	Y

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead 9/16" x 2-1/16"), dual-in-line package
U	C-6 (52-terminal .750" x .750"), square chip carrier package
X	See figure 1 (48-lead 9/16" x 2-7/16"), dual-in-line package
Y	C-5 (44-terminal .650" x .650"), square chip carrier package
Z	C-7 (68-terminal .950" x .950"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range with respect to ground (V_{CC})	-0.3 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation, (P_D)(per device type)	2.2 W
Lead temperature (soldering, 5 seconds)	+270°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	14°C/W
Cases Q, U, Y, and Z	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH}):	
Logic inputs	2.2 V dc to V_{CC} +0.3 V dc
Clock input	V_{CC} -0.4 V dc to V_{CC} +0.3 V dc
RESET, (NMI)	2.4 V dc to V_{CC} +0.3 V dc
Maximum low level input voltage (V_{IL}):	
Logic inputs	-0.3 V dc to +0.8 V dc
Clock input	-0.3 V dc to +0.45 V dc

Frequency of operation:	
01, 02	0.5 MHz to 4.0 MHz
03, 06	0.5 MHz to 6.0 MHz
04, 05	0.5 MHz to 10.0 MHz
Case operating temperature range (T_C)	-55°C to +125°C
Clock rise time (tr):	
01, 02	20 ns maximum
03, 06	15 ns maximum
04, 05	10 ns maximum
Clock fall time (tf):	
01, 02	20 ns maximum
04, 05	10 ns maximum
03, 06	15 ns maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic functions. The logic functions shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock input low voltage	V_{IL1}	Driven by external clock generator	1, 2, 3	01,02,03, 04,05,06	-0.3 1/	0.45	V
Clock input high voltage	V_{IH1}	Driven by external clock generator	1, 2, 3	01,02,03, 04,05,06	V_{CC} -0.4	V_{CC} +0.3 1/	V
Input low voltage	V_{IL2}		1, 2, 3	01,02,03, 04,05,06	-0.3 1/	0.8	V
Input high voltage	V_{IH2}		1, 2, 3	01,02,03, 04,05,06	2.4	V_{CC} +0.3 1/	V
Reset input high voltage (NMI)	V_{IH3}		1, 2, 3	01,02,03, 04,05,06	2.4	V_{CC} +0.3 1/	V
High level output voltage all outputs	V_{OH}	I_{OH} = -250 µA V_{CC} = 4.5 V	1, 2, 3	01,02,03, 04,05,06	2.4		V
Low level output voltage all outputs	V_{OL}	I_{OL} = 2.0 mA V_{CC} = 4.5 V	1, 2, 3	01,02,03, 04,05,06		0.4	V
High-impedance (off-state) output current (HIGH) (IN FLOAT)	I_{ZH}	V_{IN} = 2.4 V V_{CC} = 5.5 V	1, 2, 3	01,02,03, 04,05,06	-10	+10	µA
High-impedance (off-state) output current (LOW) (IN FLOAT)	I_{ZL}	V_{IN} = 0.4 V V_{CC} = 5.5 V	1, 2, 3	01,02,03, 04,05,06	-10	+10	µA
High level input current (input and bidirectional)	I_{IH}	V_{IN} = 2.4 V V_{CC} = 5.5 V	1, 2, 3	01,02,03, 04,05,06	-10	+10	µA
Low level input current (input and bidirectional)	I_{IL}	V_{IN} = 0.4 V V_{CC} = 5.5 V	1, 2, 3	01,02,03, 04,05,06	-10	+10	µA
Low level input current (SEGT)	I_{ILS}	$0.4 < V_{IN} < 2.4$ V $4.5\ V \le V_{CC} \le 5.5$ V	1, 2, 3	01,03,04		+200	µA
Supply current	I_{CC}	V_{CC} = 5.5 V	1, 2, 3	01,02,03, 04,05,06		400	mA
Functional tests		See 4.3.1c	7, 8	01,02,03, 04,05,06			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Waveform reference 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Clock pulse	t_{cyc}	4.5 V $\le V_{CC} \le$ 5.5 V C_L = 50 to 100 pF ±10% all outputs	1	9, 10, 11	01,02	250	2000	ns
					03,06	165	2000	
					04,05	100	2000	
Clock pulse width (low)	t_{PWL1}		2	9, 10, 11	01,02	105		ns
					03,06	70		
					04,05	40		
Clock pulse width (high)	t_{PWH1}		3	9, 10, 11	01,02	105		ns
					03,06	70		
					04,05	40		
Clock ↑ to segment number valid 3/ 4/	TdC(SNv)		6	9, 10, 11	01		130	ns
					03		110	
					04		90	
Clock ↑ to segment number not valid 4/	TdC(SNn)		7	9, 10, 11	01	20		ns
					03	10		
					04	0		
Clock ↑ to bus float 1/	TdC(Bz)		8	9, 10, 11	01,02		65	ns
					03,06		55	
					04,05		50	
Clock ↑ to address valid	TdC(A)		9	9, 10, 11	01,02		100	ns
					03,06		75	
					04,05		65	
Clock ↑ to address float 1/	TdC(Az)		10	9, 10, 11	01,02		65	ns
					03,06		55	
					04,05		50	
Address valid to data in required valid	TdA(DR)		11	9, 10, 11 5/	01,02		475	ns
					03,06		305	
					04,05		180	
Data to CLK ↑ setup time	TsDR(C)		12	9, 10, 11	01,02	30		ns
					03,06	20		
					04,05	10		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Waveform reference 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
$\overline{DS}$ ↓ to address active	TdDS(A)	4.5 V ≤ V_{CC} ≤ 5.5 V C_L = 50 to 100 pF ±10% all outputs	13	9, 10, 11 5/	01,02	80		ns
					03,06	45		
					04,05	20		
Clock ↑ to data out valid	TdC(DW)		14	9, 10, 11	01,02		100	ns
					03,06		75	
					04,05		60	
Data in to $\overline{DS}$ ↑ hold time	ThDR(DS)		15	9, 10, 11	01,02	0		ns
					03,06	0		
					04,05	0		
Data out valid to $\overline{DS}$ ↑ delay	TdDW(DS)		16	9, 10, 11 5/	01,02	295		ns
					03,06	195		
					04,05	110		
Address valid to $\overline{MREQ}$ ↓ delay	TdA(MR)		17	9, 10, 11 5/	01,02	55		ns
					03,06	35		
					04,05	20		
Clock ↓ to $\overline{MREQ}$ ↓ delay	TdC(MR)		18	9, 10, 11	01,02		80	ns
					03,06		70	
					04,05		50	
$\overline{MREQ}$ width (High)	TwMRh		19	9, 10, 11 5/	01,02	210		ns
					03,06	135		
					04,05	80		
$\overline{MREQ}$ ↓ to address not active 1/	TdMR(A)		20	9, 10, 11 5/	01,02	70		ns
					03,06	35		
					04,05	15		
Data out valid to $\overline{DS}$ ↓ (Write delay)	TdDW(DSW)		21	9, 10, 11 5/	01,02	55		ns
					03,06	35		
					04,05	15		
$\overline{MREQ}$ ↓ to data in required valid	TdMR(DR)		22	9, 10, 11 5/	01,02		370	ns
					03,06		230	
					04,05		140	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Waveform reference 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Clock ↓ to $\overline{MREQ}$ ↑ delay	TdC(MR)	$4.5\ V \le V_{CC} \le 5.5\ V$ C_L = 50 to 100 pF ±10% all outputs	23	9, 10, 11	01,02		80	ns
					03,06		60	
					04,05		50	
Clock ↑ to $\overline{AS}$ ↓ delay	TdC(ASf)		24	9, 10, 11	01,02		80	ns
					03,06		60	
					04,05		45	
Address valid to $\overline{AS}$ ↑ delay delay	TdA(AS)		25	9, 10, 11 5/	01,02	55		ns
					03,06	35		
					04,05	20		
Clock ↓ to $\overline{AS}$ ↑ delay	TdC(ASr)		26	9, 10, 11	01,02		90	ns
					03,06		80	
					04,05		45	
$\overline{AS}$ ↑ to data in required valid	TdAS(DR)		27	9, 10, 11 5/	01,02		360	ns
					03,06		220	
					04,05		140	
$\overline{DS}$ ↑ to $\overline{AS}$ ↓ delay	TdDS(AS)		28	9, 10, 11 5/	01,02	70		ns
					03,06	35		
					04,05	15		
$\overline{AS}$ width (Low)	TwAS		29	9, 10, 11 5/	01,02	85		ns
					03,06	55		
					04,05	30		
$\overline{AS}$ ↑ to address not active delay 1/	TdAS(A)		30	9, 10, 11 5/	01,02	70		ns
					03,06	45		
					04,05	15		
Address float to $\overline{DS}$ (Read) ↓ delay 1/	TdAz(DSR)		31	9, 10, 11	01,02	0		ns
					03,06	0		
					04,05	0		
$\overline{AS}$ ↑ to $\overline{DS}$ ↓ (Read) delay	TdAS(DSR)		32	9, 10, 11 5/	01,02	80		ns
					03,06	55		
					04,05	30		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Waveform reference 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
$\overline{DS}$ (Read) ↓ to data in required valid	TdDSR(DR)	4.5 V $\le V_{CC} \le$ 5.5 V C_L = 50 to 100 pF ±10% all outputs	33	9, 10, 11 5/	01,02		205	ns
					03,06		130	
					04,05		70	
Clock ↓ to $\overline{DS}$ ↑ delay	TdC(DSr)		34	9, 10, 11	01,02		70	ns
					03,06		65	
					04,05		50	
$\overline{DS}$ ↑ to data out not valid 1/	TdDS(DW)		35	9, 10, 11 5/	01,02	75		ns
					03,06	45		
					04,05	25		
Address valid to $\overline{DS}$ (Read) ↓ delay	TdA(DSR)		36	9, 10, 11 5/	01,02	180		ns
					03,06	110		
					04,05	65		
Clock ↑ to $\overline{DS}$ (Read) ↓ delay	TdC(DSR)		37	9, 10, 11	01,02		120	ns
					03,06		85	
					04,05		65	
$\overline{DS}$ (Read) width (Low)	TwDSR		38	9, 10, 11 5/	01,02	275		ns
					03,06	185		
					04,05	110		
Clock ↓ to $\overline{DS}$ (Write) ↓ delay	TdC(DSW)		39	9, 10, 11	01,02		95	ns
					03,06		80	
					04,05		65	
$\overline{DS}$ (Write) width (Low)	TwDSW		40	9, 10, 11 5/	01,02	185		ns
					03,06	110		
					04,05	75		
$\overline{DS}$ (Input) ↓ to data in required valid	TdDSI(DR)		41	9, 10, 11 5/	01,02		330	ns
					03,06		210	
					04,05		120	
Clock ↓ to $\overline{DS}$ (I_O) ↓ delay	TdC(DSf)		42	9, 10, 11	01,02		120	ns
					03,06		90	
					04,05		70	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Waveform reference 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
$\overline{DS}$ (I/O) width (low)	TwDS	$4.5\ V \le V_{CC} \le 5.5\ V$ C_L = 50 to 100 pF ±10% all outputs	43	9, 10, 11 5/	01,02	410		ns
					03,06	255		
					04,05	160		
$\overline{AS}$ ↑ to $\overline{DS}$ (acknowledge) ↓ delay	TdAS(DSA)		44	9, 10, 11 5/	01,02	1065		ns
					03,06	690		
					04,05	410		
Clock ↑ to $\overline{DS}$ (acknowledge) ↓ delay	TdC(DSA)		45	9, 10, 11	01,02		120	ns
					03,06		85	
					04,05		70	
$\overline{DS}$ (acknowledge) ↓ to data in required delay	TdDSA(DR)		46	9, 10, 11 5/	01,02		455	ns
					03,06		295	
					04,05		165	
Clock ↑ to status valid delay	TdC(S)		47	9, 10, 11	01,02		110	ns
					03,06		85	
					04,05		65	
Status valid to $\overline{AS}$ ↑ delay	TdS(AS)		48	9, 10, 11 5/	01,02	50		ns
					03,06	30		
					04,05	10		
$\overline{RESET}$ to clock ↑ set-up time	TsR(C)		49	9, 10, 11	01,02	180		ns
					03,06	70		
					04,05	50		
$\overline{RESET}$ to clock ↑ hold-time	ThR(C)		50	9, 10, 11	01,02	0		ns
					03,06	0		
					04,05	0		
$\overline{NMI}$ width (low)	TwNMI		51	9, 10, 11	01,02	100		ns
					03,06	70		
					04,05	50		
$\overline{NMI}$ to clock ↑ set-up time	TsNMI(C)		52	9, 10, 11	01,02	140		ns
					03,06	70		
					04,05	50		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Waveform reference 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
VI, NVI to clock + set-up time	TsVI(C)	$4.5\ V \le V_{CC} \le 5.5\ V$ C_L = 50 to 100 pF ±10% all outputs	53	9, 10, 11	01,02	110		ns
					03,06	50		
					04,05	40		
VI, NVI to clock + hold time	ThVI(C)		54	9, 10, 11	01,02	20		ns
					03,06	20		
					04,05	10		
$\overline{SEGT}$ to clock + set-up time 4/	TsSGT(C)		55	9, 10, 11	01	70		ns
					03	55		
					04	40		
$\overline{SEGT}$ to clock + hold time 4/	ThsSGT(C)		56	9, 10, 11	01	0		ns
					03	0		
					04	0		
$\overline{MI}$ to clock + set-up time	TsMI(C)		57	9, 10, 11	01,02	180		ns
					03,06	140		
					04,05	80		
$\overline{MI}$ to clock + hold time	ThMI(C)		58	9, 10, 11	01,02	0		ns
					03,06	0		
					04,05	0		
Clock + to $\overline{MO}$ delay time	TdC(MO)		59	9, 10, 11	01,02		120	ns
					03,06		85	
					04,05		80	
$\overline{STOP}$ to clock + set-up time	TsSTP(C)		60	9, 10, 11	01,02	140		ns
					03,06	100		
					04,05	50		
$\overline{STOP}$ to clock + hold time	ThSTP(C)		61	9, 10, 11	01,02	0		ns
					03,06	0		
					04,05	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Waveform reference 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
$\overline{WAIT}$ to to clock ↑ set-up time	TsW(C)	4.5 V $\le V_{CC} \le$ 5.5 V C_L = 50 to 100 pF ±10% all outputs	62	9, 10, 11	01,02	50		ns
					03,06	30		
					04,05	20		
$\overline{WAIT}$ to clock ↑ hold time	ThW(C)		63	9, 10, 11	01,02	10		ns
					03,06	10		
					04,05	5		
$\overline{BUSRQ}$ to clock ↑ set-up time	TsBRQ(C)		64	9, 10, 11	01,02	90		ns
					03,06	80		
					04,05	60		
$\overline{BUSRQ}$ to clock ↑ hold time	ThBRQ(C)		65	9, 10, 11	01,02	10		ns
					03,06	10		
					04,05	5		
Clock ↑ to $\overline{BUSAK}$ ↑ delay	TdC(BAKr)		66	9, 10, 11	01,02		100	ns
					03,06		75	
					04,05		65	
Clock ↑ to $\overline{BUSAK}$ ↓ delay	TdC(BAKf)		67	9, 10, 11	01,02		100	ns
					03,06		75	
					04,05		65	
Address valid width	TwA		68	9, 10, 11 5/	01,02	150		ns
					03,06	95		
					04,05	50		
$\overline{DS}$ ↑ to status not valid 1/	TdDS(s)		69	9, 10, 11 5/	01,02	80		ns
					03,06	55		
					04,05	30		

1/ Guaranteed, if not tested.

2/ The waveform reference number refers to the position where the parameter appears on figure 4.

3/ For waveform reference number 6, C_L = 50 pF ±10%.

4/ These parameters are for 01, 03, and 04 devices only.

5/ These waveform reference number parameters are clock dependent. The limits provided are at F_{MAX}. To determine the limits at other frequencies use the following equations:

Waveform reference number	Device types 01 and 02	Device types 03 and 06	Device types 04 and 05
11	$2\ t_{cyc} + t_{PWH1} - 130$ ns	$2\ t_{cyc} + t_{PWH1} - 95$ ns	$2\ t_{cyc} + t_{PWH1} - 60$ ns
13	$t_{PWL1} - 25$ ns	$t_{PWL1} - 25$ ns	$t_{PWL1} - 20$ ns
16	$t_{cyc} + t_{PWH1} - 60$ ns	$t_{cyc} + t_{PWL1} - 40$ ns	$t_{cyc} + t_{PWH1} - 30$ ns
17	$t_{PWH1} - 50$ ns	$t_{PWH1} - 35$ ns	$t_{PWH1} - 20$ ns
19	$t_{cyc} - 40$ ns	$t_{cyc} - 30$ ns	$t_{cyc} - 20$ ns
20	$t_{PWL1} - 35$ ns	$t_{PWL1} - 35$ ns	$t_{PWL1} - 20$ ns
21	$t_{PWH1} - 50$ ns	$t_{PWH1} - 35$ ns	$t_{PWH1} - 25$ ns
22	$2\ t_{cyc} - 130$ ns	$2\ t_{cyc} - 100$ ns	$2\ t_{cyc} - 60$ ns
25	$t_{PWH1} - 50$ ns	$t_{PWH1} - 35$ ns	$t_{PWH1} - 20$ ns
27	$2\ t_{cyc} - 140$ ns	$2\ t_{cyc} - 110$ ns	$2\ t_{cyc} - 60$ ns
28	$t_{PWL1} - 35$ ns	$t_{PWL1} - 35$ ns	$t_{PWL1} - 25$ ns
29	$t_{PWH1} - 20$ ns	$t_{PWH1} - 15$ ns	$t_{PWH1} - 10$ ns
30	$t_{PWL1} - 35$ ns	$t_{PWL1} - 25$ ns	$t_{PWL1} - 20$ ns
32	$t_{PWL1} - 25$ ns	$t_{PWL1} - 15$ ns	$t_{PWL1} - 10$ ns
33	$t_{cyc} + t_{PWH1} - 150$ ns	$t_{cyc} + t_{PWH1} - 105$ ns	$t_{cyc} + t_{PWH1} - 70$ ns
35	$t_{PWL1} - 30$ ns	$t_{PWL1} - 25$ ns	$t_{PWL1} - 15$ ns
36	$t_{cyc} - 70$ ns	$t_{cyc} - 55$ ns	$t_{cyc} - 35$ ns
38	$t_{cyc} + t_{PWH1} - 80$ ns	$t_{cyc} + t_{PWH1} - 50$ ns	$t_{cyc} + t_{PWH1} - 30$ ns
40	$t_{cyc} - 65$ ns	$t_{cyc} - 55$ ns	$t_{cyc} - 25$ ns
41	$2\ t_{cyc} - 170$ ns	$2\ t_{cyc} - 120$ ns	$2\ t_{cyc} - 80$ ns
43	$2\ t_{cyc} - 90$ ns	$2\ t_{cyc} - 75$ ns	$2\ t_{cyc} - 40$ ns
44	$4\ t_{cyc} + t_{PWL1} - 40$ ns	$4\ t_{cyc} + t_{PWL1} - 40$ ns	$4\ t_{cyc} + t_{PWL1} - 30$ ns
46	$2\ t_{cyc} + t_{PWH1} - 150$ ns	$2\ t_{cyc} + t_{PWH1} - 105$ ns	$2\ t_{cyc} + t_{PWH1} - 75$ ns
48	$t_{PWH1} - 55$ ns	$t_{PWH1} - 40$ ns	$t_{PWH1} - 30$ ns
68	$t_{cyc} - 90$ ns	$t_{cyc} - 70$ ns	$t_{cyc} - 50$ ns
69	$t_{PWL1} - 25$ ns	$t_{PWL1} - 15$ ns	$t_{PWL1} - 10$ ns

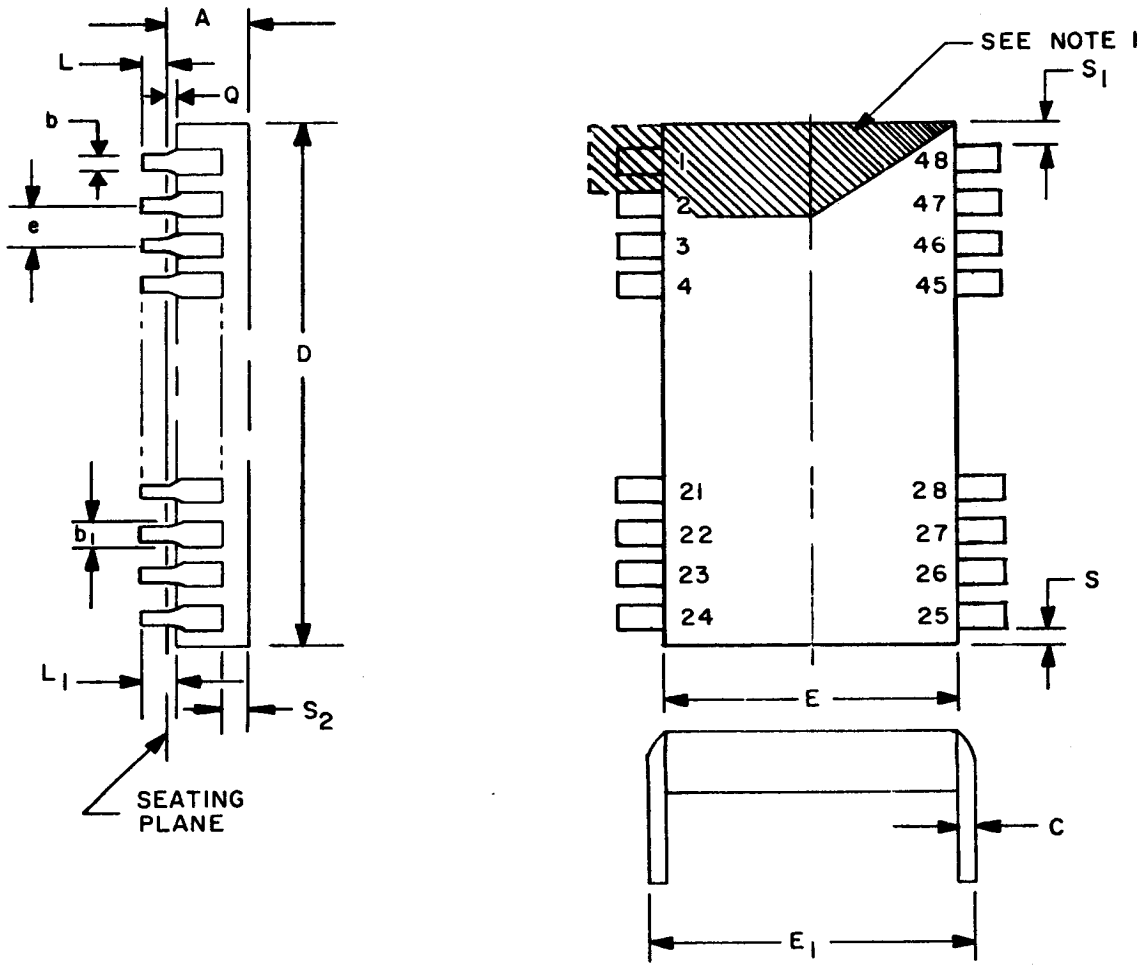

FIGURE 1. Case outline X (48-lead, 9/16" x 2 7/16"), dual-in-line package, types 01, 03, and 04.

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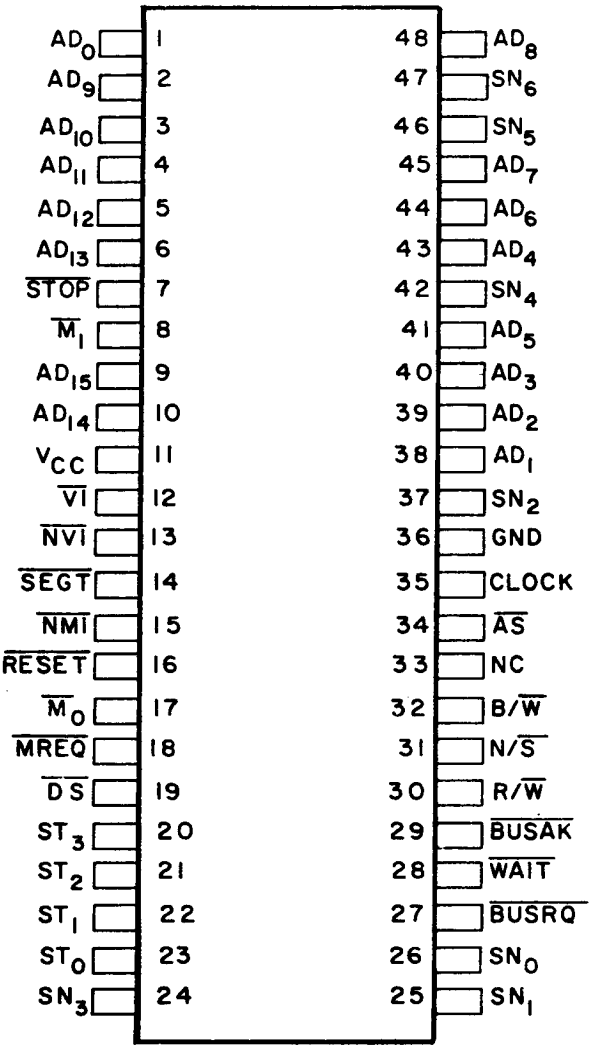
Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	---	.225	---	5.72	
b	.014	.023	0.36	0.58	7
b_1	.030	.070	0.76	1.78	2,7
c	.008	.015	0.20	0.38	7
D	---	2.480	---	62.99	
E	.510	.620	12.95	15.75	
E_1	.520	.620	13.21	15.75	6
e	.100 BSC		2.54 BSC		4,8
L	.120	.200	3.05	5.08	
L_1	.150	---	3.81	---	
Q	.020	.060	0.51	1.52	3
S	---	.098	---	2.40	5
S_1	.005	---	0.13	---	5
S_2	.005	---	0.13	---	9

NOTES:
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be .020 (0.51 mm) for leads number 1, 24, 25 and 48 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (0.25 mm) of its exact longitudinal position relative to pins 1 and 48.
5. Applies to all four corners (leads number 1, 24, 25 and 48) shall apply (see MIL-M-38510, Appendix C).
6. Lead center when α is 0^o. E_1 shall be measured at the centerline of the leads.
7. All leads - increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A is applied.
8. Forty-six spaces.
9. The top of the lead shall not exceed above the brazed pad top surface.

FIGURE 1. Case outline X (48-lead, 9/16" x 2 7/16"), dual-in-line package, types 01, 03, and 04 - Continued.

(Top view) for Cases X and Q

Device types 01, 03, and 04



Device types 02 and 05

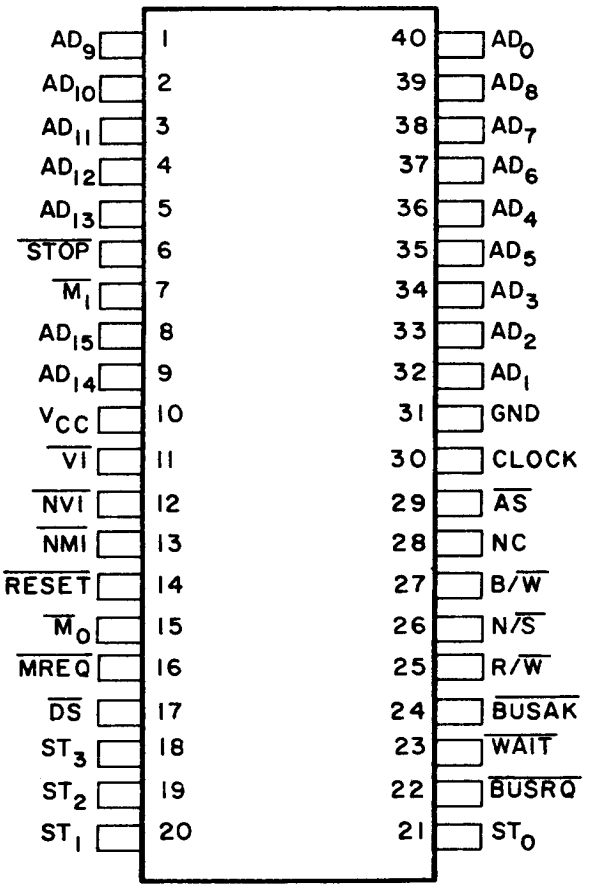
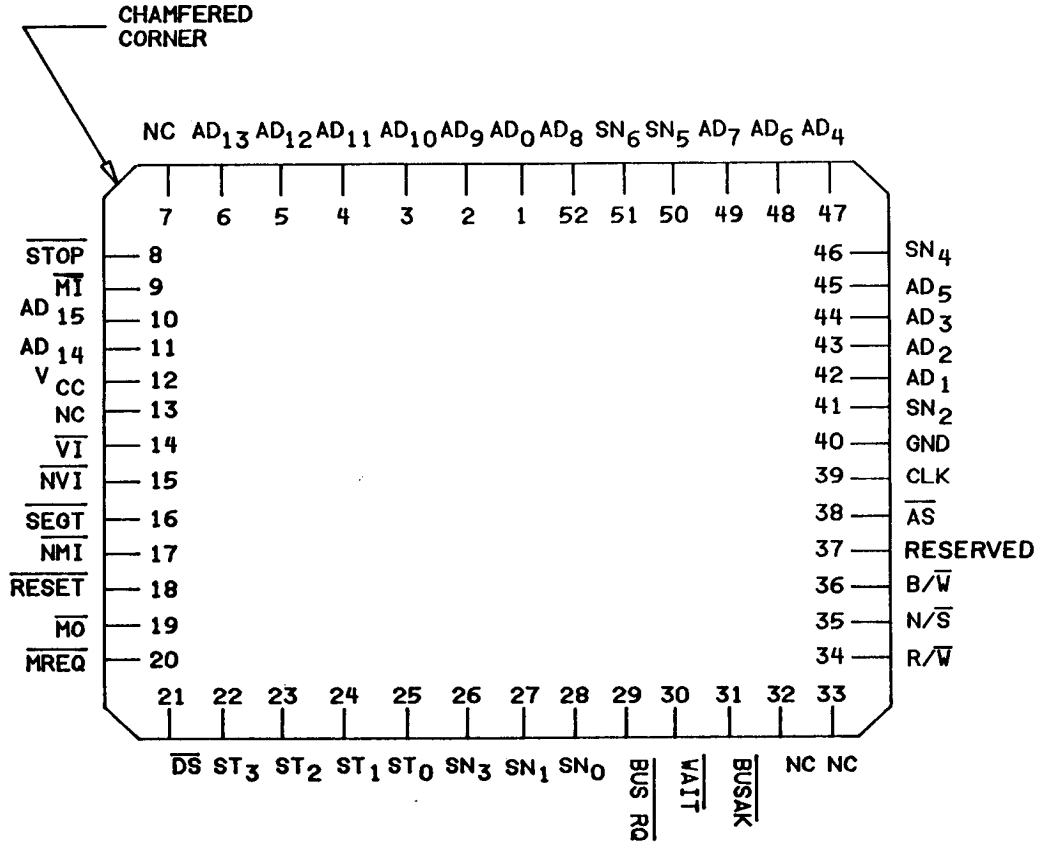


FIGURE 2. Terminal connections.

Case outline U, (52-terminal, .750" x .750")
Square chip carrier package

Device types 01, 03, and 04



NC = No connection

FIGURE 2. Terminal connections - Continued.

Case outline Z, (68-terminal, .950" x .950")
Square chip carrier package

Device types 01, 03, and 04

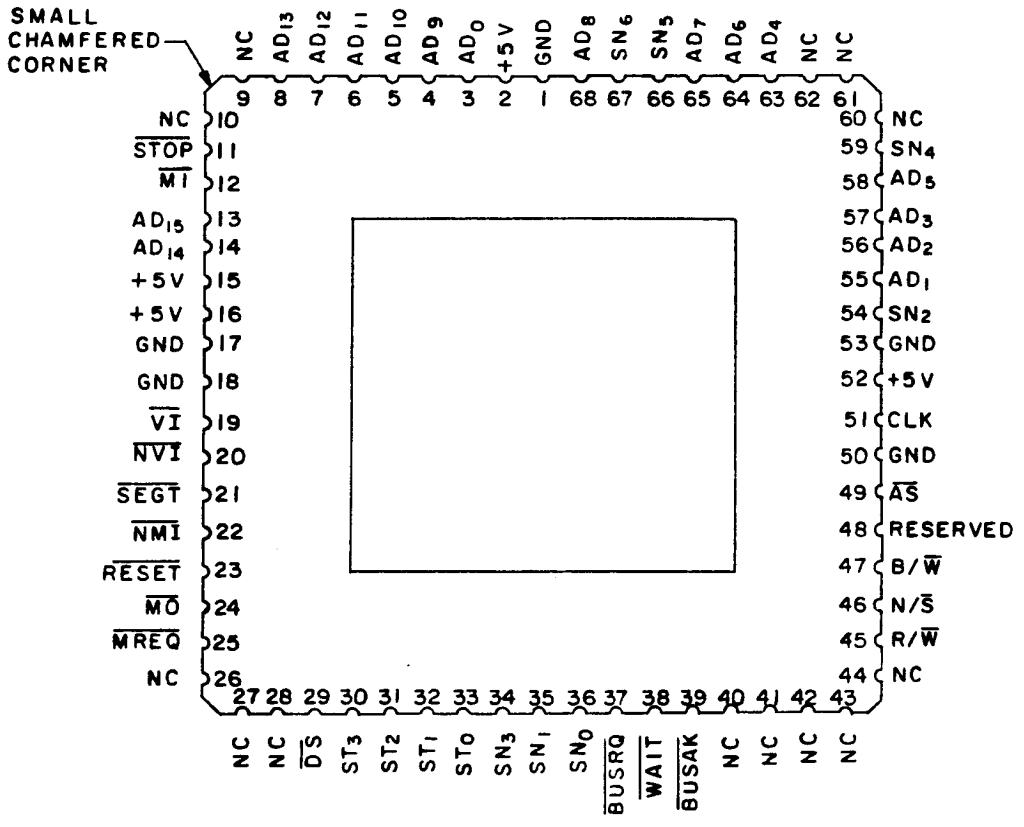
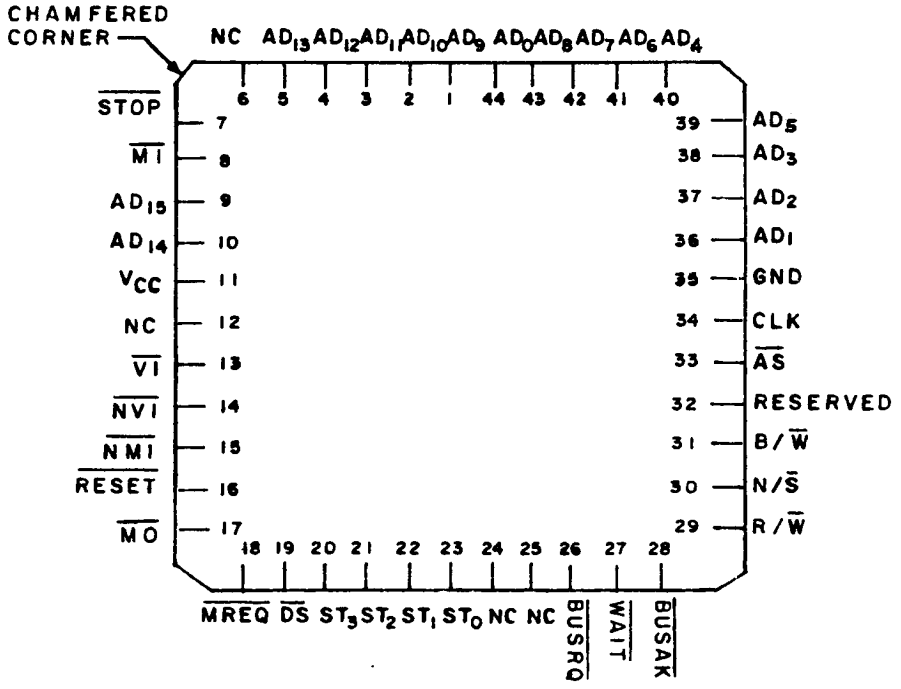


FIGURE 2. Terminal connections - Continued.

Case outline Y, (44-terminal, .650" x .650")
Square chip carrier package

Device types 02, 05, and 06



NC = No connection

FIGURE 2. Terminal connections - Continued.

Device types 01, 03, and 04

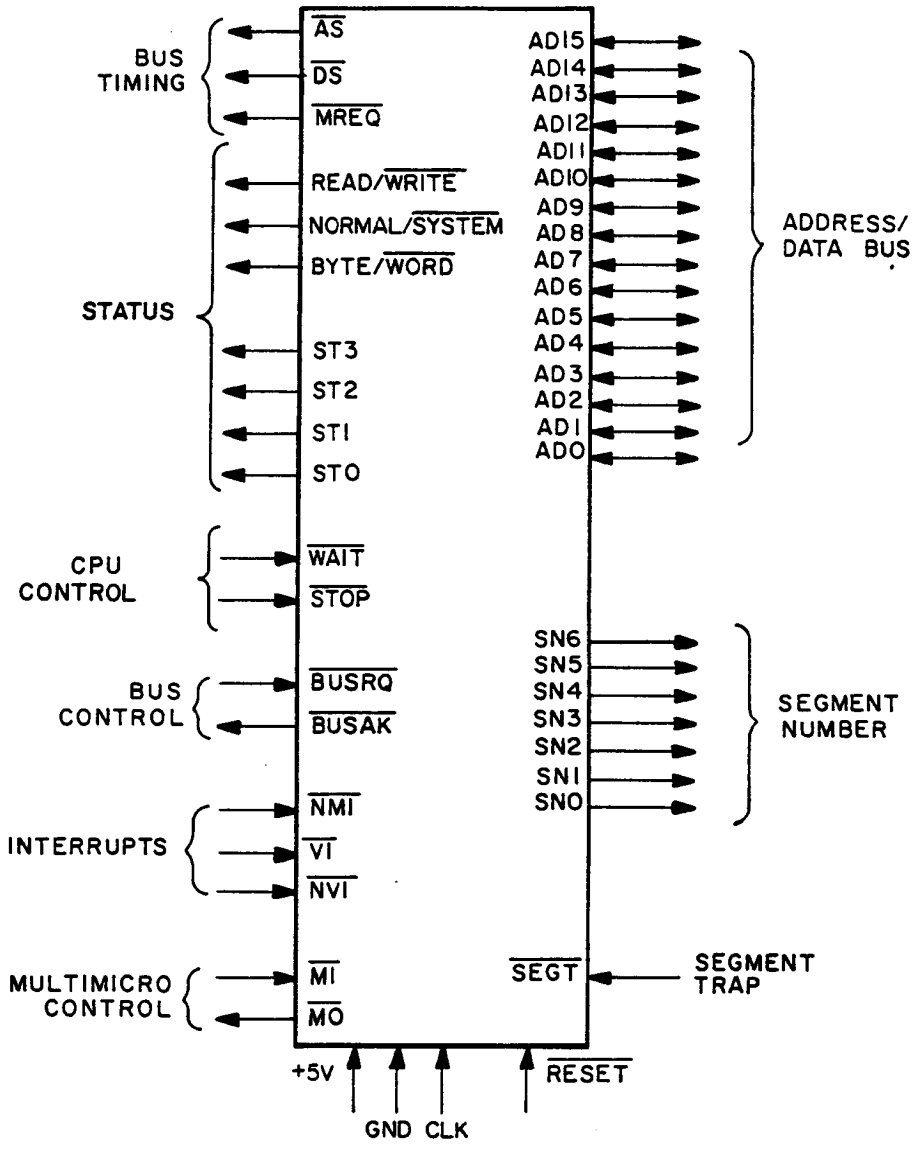


FIGURE 3. Logic functions.

Device types 02, 05, and 06

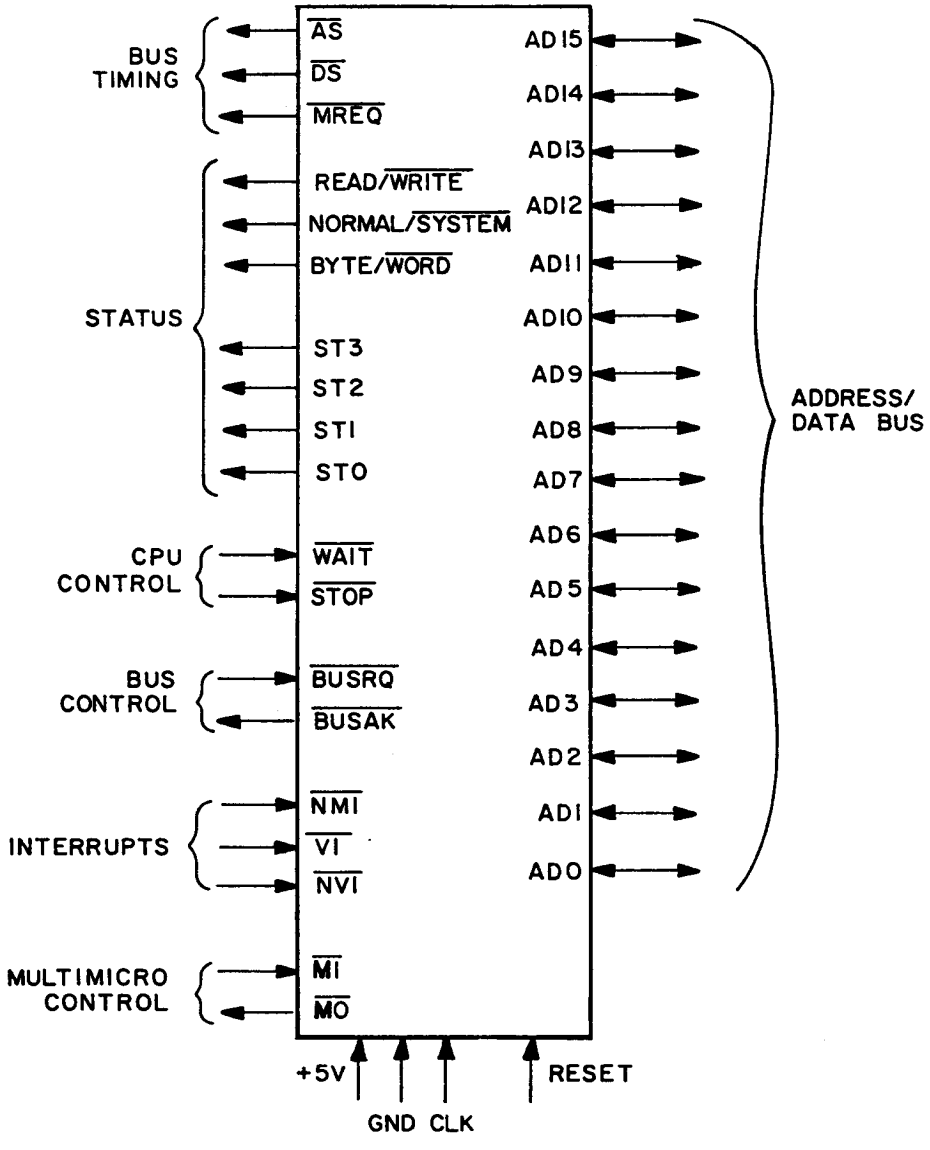


FIGURE 3. Logic functions - Continued.

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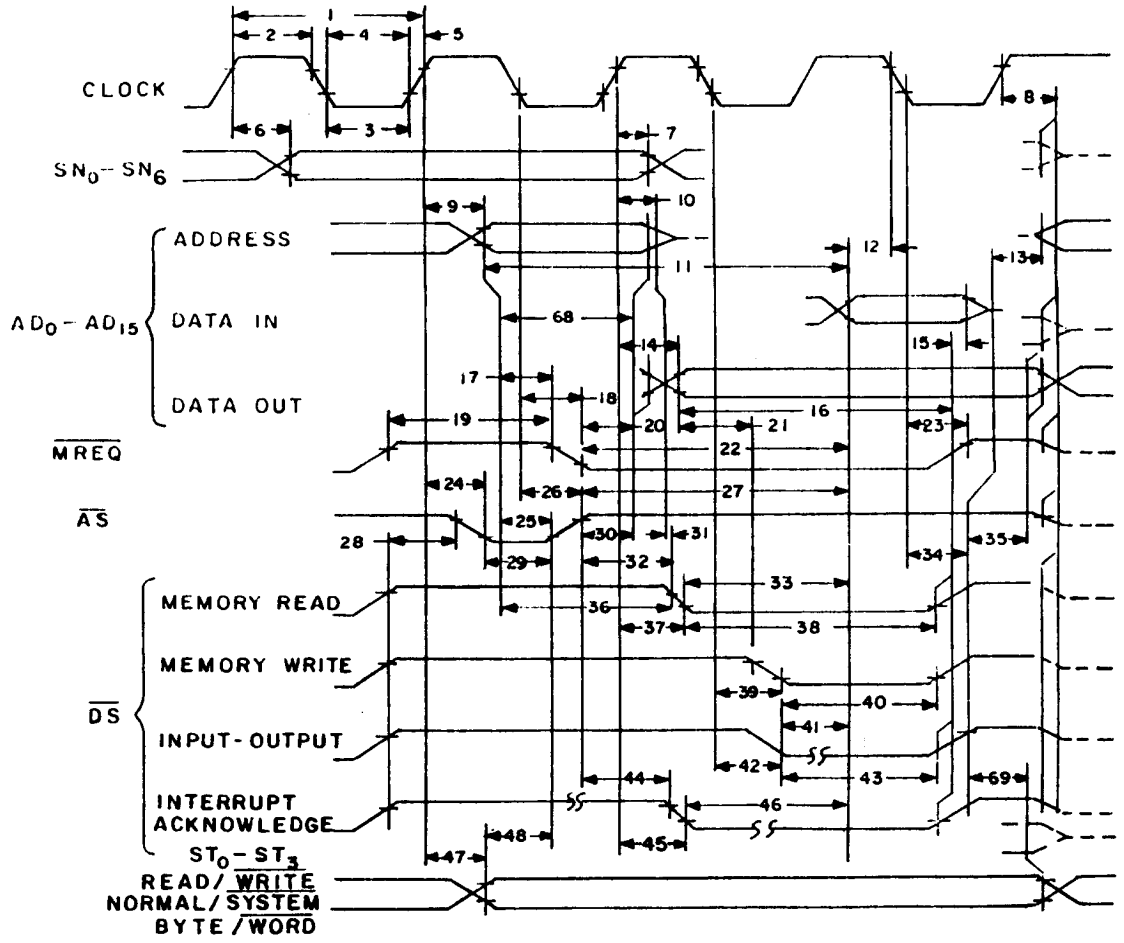

FIGURE 4. AC timing diagrams.

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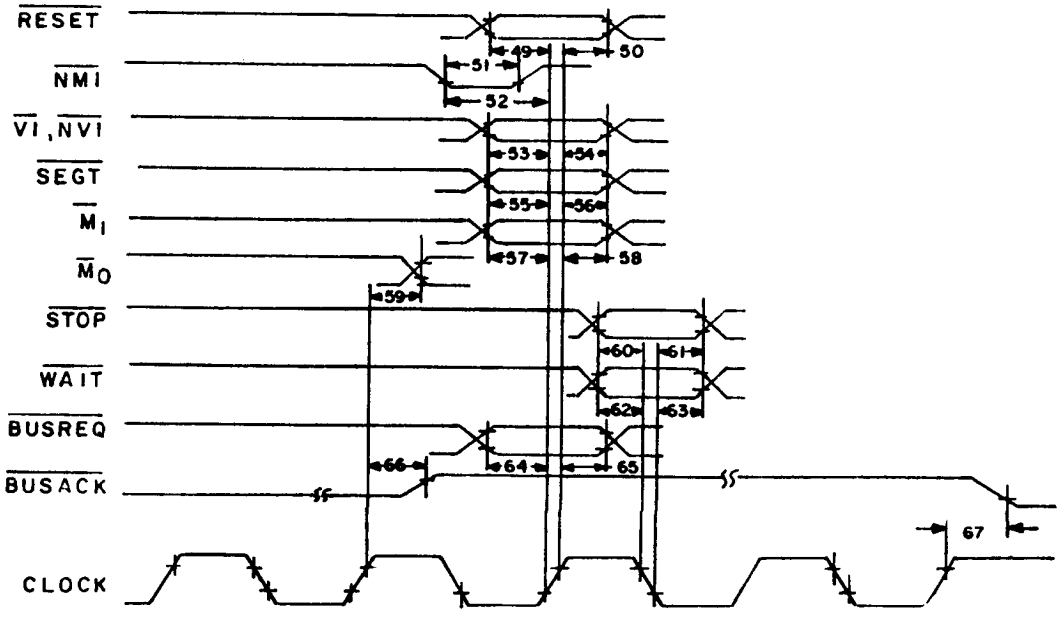

FIGURE 4. AC timing diagrams - Continued

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, D, or E using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7, functional testing shall include verification of instruction set.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.
**Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, D, or E using circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/5200XBXX.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-6375.

6.4 Symbols, definitions, and functional descriptions. The symbols, definitions, and functional description for this device shall be as follows:

SYSTEM DEFINITIONS

SYMBOL	FUNCTION
AD_0-AD_{15} (Address/Data Bus)	Inputs/outputs, active High, three-state. These multiplexed address and data lines are used both I/O and to address memory. AD_{15} = MSB.
$\overline{AS}$ (Address Strobe)	Output, active Low, three-state. The rising edge of $\overline{AS}$ indicates addresses are valid.
$\overline{BUSAK}$ (Bus Acknowledge)	Output, active Low. A Low on this line indicates the CPU has relinquished control of the bus. This occurs after completion of the current machine cycle. BUSAK goes inactive one clock cycle after the synchronization of $\overline{BUSRQ}$ being released.
$\overline{BUSRQ}$ (Bus Request)	Input, active Low. This line must be driven Low to request the bus from the CPU. It is sampled for being active at the beginning of each machine cycle. When it is released, it is synchronized with the next rising clock edge.
$\overline{DS}$ (Data Strobe)	Output, active Low, three-state. This line times the data in and out of the CPU.
$\overline{MREQ}$ (Memory Request)	Output, active Low, three-state. A Low on this line indicates that the address/data bus holds a memory address.
$\overline{MI}$, $\overline{MO}$ (Multi-Micro In, Multi-Micro Out)	Input and output, active Low. These two lines form a resource-request daisy chain that allows one CPU in a multi-microprocessor system to access a shared resource. $\overline{MI}$ is sampled on the rising edge of T_3 of the last machine cycle of any instruction and internally latched.
$\overline{NMI}$ (Non-Maskable Interrupt)	Edge triggered, input, active Low. A high-to-low transition on NMI request a non-maskable interrupt. The NMI interrupt has the highest priority of the three types of interrupts. The internal $\overline{NMI}$ latch is sampled on the rising edge of T_3 of the last machine cycle of any instruction.
$\overline{NVI}$ (Non-Vectored Interrupt)	Input, active Low. A low on this line requests a non-vectored interrupt. It is sampled on the rising edge of T_3 of the last machine cycle of any instruction.
CLK (System CLock)	Input. CLK is a 5 V single-phase time-base input.

SYSTEM DEFINITIONS

SYMBOL	FUNCTION
$\overline{\text{RESET}}$ (Reset)	Input, active Low. A low on this line resets the CPU. RESET must be active for at least five clock cycles.
R/$\overline{\text{W}}$ (Read/Write)	Output, Low = Write, three-state. R/$\overline{\text{W}}$ indicates that the CPU is reading from or writing to memory or I/O.
ST_0-ST_3 (Status)	Outputs, active High, three-state. These lines specify the CPU status.
$\overline{\text{STOP}}$ (Stop)	Input, active Low. This input can be used to single-step instruction execution. It is sampled on the last falling clock edge preceding any first instruction fetch cycle.
$\overline{\text{VI}}$ (Vectored Interrupt)	Input, active Low. A Low on this line requests a vectored interrupt. It is sampled on the rising edge of T_3 of the last machine cycle of any instruction.
$\overline{\text{WAIT}}$ (Wait)	Input, active Low. This line indicates to the CPU that the memory or I/O device is not ready for data transfer. It is sampled on the falling edge of T_2 and any subsequent $\overline{\text{WAIT}}$ states.
B/$\overline{\text{W}}$ (Byte/Word)	Output, Low = word, three-state. This signal defines the type of memory reference on the 16-bit address/data bus.
N/$\overline{\text{S}}$ (Normal/System Mode)	Output, Low = system mode, three-state. N/$\overline{\text{S}}$ indicates the CPU is in the normal or system mode.
SN_0-SN_6 (Segment Number)	Outputs, active High, three-state. These lines provide the 7-bit segment number used to address one of 128 segments by the memory management unit. Outputs by the 01, 03, and 04 parts only. SN_6 = MSB.
$\overline{\text{SEGT}}$ (Segment Trap)	Input, active Low. The memory management unit interrupts the CPU with a low on this line when the MMU detects a segmentation trap. Input on the 01, 03, and 04 parts only. It is sampled on the rising edge of T_3 of the last machine cycle of any instruction.

6.5 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor 1/ similar part number	Replacement military specification part number
8000301XX	56708 66958	Z0800104CMB Z8001D2/883	M38510/52001BXX
8000301ZX	66958	Z8001K2/883	M38510/52001BTX
8000301UX	56708 66958	Z0800104LMB Z8001K2/883	M38510/52001BZX

See footnotes at end of table.

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Military drawing part number	Vendor CAGE number	Vendor 1/ similar part number	Replacement military specification part number
8000302QX 2/	56708 66958	Z0800204CMB Z8002D2/883	M38510/52002BQX
8000302YX	56708 66958	Z0800204LMB Z8002K2/883	M38510/52002BYX
8000303XX	56708 66958	Z0800106CMB Z8001AD2/883	M38510/52003BXX
8000303ZX	66958	Z8001AK2/883	M38510/52003BTX
8000303UX	56708 66958	Z0800106LMB Z8001AK2/883	M38510/52003BZX
8000304XX	56708 66958	Z0800110CMB Z8001BD2/883	M38510/5200XBXX
8000304ZX	66958	Z8001BK2/883	M38510/5200XBTX
8000304UX	56708 66958	Z0800110LMB Z8001BK2/883	M38510/5200XBZX
8000305QX	56708 66958	Z0800210CMB Z8002BD2/883	M38510/5200XBQX
8000305YX	56708 66958	Z0800210LMB Z8002BK2/883	M38510/5200XBYX
8000306YX	56708 66958	Z0800206LMB Z8002AK2/883	M38510/52004BYX

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ Inactive for new design. Use applicable QPL-38510 device.

Vendor CAGE number	Vendor name and address
56708	Zilog, Incorporated 210 Hacienda Avenue Campbell, CA 95008
66958	SGS Semiconductor Corporation 1000 East Bell Road Phoenix, AZ 85022

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