REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
F	Add margin test. Delete one vendor, CAGE 01295. Delete reprogrammability of EPROMS. Add device types 07, 08, 09, 10, and 11. Add program method C and characteristics. Minor changes to table I, table II, and table III. Change to military drawing format.	87 MAY 12	M.A. Frye
G	Make changes to parameters in table IIIC. Delete one vendor, CAGE 34335, from devices 03 and 04. Editorial changes throughout. Changes in notes under Table I.	1988 MAY 23	M.A. Frye

CURRENT CAGE CODE 67268

REV																							
SHEET																							
REV	G	G	F																				
SHEET	22	23	24																				
REV STATUS OF SHEETS	REV	G	G	G	G	G	G	F	F	G	G	F	F	F	F	F	F	F	F	F	F	F	G
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Kirk Affeian

CHECKED BY: Ray Monnin

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 14 JULY 1980

REVISION LEVEL: G

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, NMOS 4KX8 UV ERASEABLE PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	80012

SHEET 1 OF 24

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E778

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

80012	01	J	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access time	Temperature range
01	(see 6.4)	4KX8-bit UV EPROM	450 ns	-55°C to 100°C
02	(see 6.4)	4KX8-bit UV EPROM	450 ns	-55°C to 100°C
03	(see 6.4)	4KX8-bit UV EPROM	250 ns	-55°C to 125°C
04	(see 6.4)	4KX8-bit UV EPROM	450 ns	-55°C to 125°C
05	(see 6.4)	4KX8-bit UV EPROM	350 ns	-55°C to 125°C
06	(see 6.4)	4KX8-bit UV EPROM	450 ns	-55°C to 125°C
07	(see 6.4)	4KX8-bit UV EPROM	150 ns	-55°C to 125°C
08	(see 6.4)	4KX8-bit UV EPROM	200 ns	-55°C to 125°C
09	(see 6.4)	4KX8-bit UV EPROM	250 ns	-55°C to 125°C
10	(see 6.4)	4KX8-bit UV EPROM	300 ns	-55°C to 125°C
11	(see 6.4)	4KX8-bit UV EPROM	450 ns	-55°C to 125°C

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24-pin, 1.290" x 0.610" x 0.225"), dual-in-line package 1/

1.3 Absolute maximum ratings.

Supply voltage, V_{CC}	-0.3 V dc to 6.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation, P_D	1.0 W
Lead temperature (soldering 10 seconds)	300°C
Thermal resistance, junction to case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+160°C
All input or output voltages with respect to ground	-0.3 V dc to 6.0 V dc
V_{PP} supply voltage with respect to ground during program:	
Devices 01, 02, 05, 06	-0.3 V dc to 26.5 V dc
Devices 03, 04	-0.3 V dc to 22.0 V dc
Devices 07, 08, 09, 10, 11	-0.3 V dc to 13.3 V dc

1/ Lid shall be transparent to permit ultraviolet light erasure.

1.4 Recommended operating conditions.

Case operating temperature range (T_C):	
Devices 01, 02	-55°C to +100°C
Devices 03 - 11	-55°C to +125°C
Input low voltage, V_{IL}	-0.1 V dc to 0.8 V dc
Input high voltage, V_{IH}	2.0 V dc to 6.5 V dc
Supply voltage, V_{CC}	+4.5 V dc to +5.5 V dc
High level program input voltage $V_{IN(PR)}$:	
Devices 01, 02, 05, 06	24 V dc to 26 V dc
Devices 03, 04	20.5 V dc to 21.5 V dc
Devices 07, 08, 09, 10, 11	12.0 V dc to 13.3 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/	Device type	Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	I_{OH} = -400 µA V_{IL} = 0.8 V, V_{IH} = 2.0 V	All	1, 2, 3	2.4		V
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V	All	1, 2, 3		0.45	V
Output leakage current	I_{OL}	V_{OUT} = 5.5 V $\overline{CE}$ = V_{IH} or PD/$\overline{PGM}$ = V_{IH}	All	1, 2, 3		10	µA
Supply current (standby) 3/	I_{SB}	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IL} or PD/$\overline{PGM}$ = V_{IH}	01,02,03 04,05,06	1, 2, 3		45	mA
			07,08,09 10,11	1, 2, 3		40	
Supply current (active) 3/	I_{CC}	$\overline{OE}$ = $\overline{CE}$ = V_{IL} or PD/$\overline{PGM}$ = V_{IH}	01,03,04	1, 2, 3		150	mA
			02,05,06			160	
			07,08,09 10,11			100	
Input capacitance 4/	C_{IN}	V_{IN} = 0 V See 4.3.1c T_C = 25°C f = 1 MHz	All	4		6	pF
Address to output delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} 5/ or PD/$\overline{PGM}$ = V_{IL}	07	9, 10, 11		150	ns
			08			200	
			03,09			250	
			10			300	
			05			350	
			01,02,04 06,11			450	
Chip enable to output delay	t_{CE}	$\overline{OE}$ = V_{IL} 5/ or PD/$\overline{PGM}$ = V_{IL}	07	9, 10, 11		150	ns
			08			200	
			03,09			250	
			10			300	
			05			350	
			01,02,04 06,11			450	
Output enable to output delay	t_{OE}	$\overline{CE}$ = V_{IL} 5/ or PD/$\overline{PGM}$ = V_{IL}	07,08	9, 10, 11		75	ns
			03,05,09			100	
			10			110	
			01,02,04 06,11			150	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Output enable high to output float 6/	t_{DF}	$\overline{CE}$ = V_{IL} 5/ or PD/$\overline{PGM}$ = V_{IL}	07,08,09,10	9, 10, 11		60	ns
			03			70	
			11			80	
			05			110	
			01,02,04,06			130	
Address to output hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} 5/ or PD/$\overline{PGM}$ = V_{IL}	All	9, 10, 11	0		ns

1/ For device types 01 and 02, T_C = -55°C to 100°C, GND = 0 V, V_{CC} = 5 V, and for device type 02 only, V_{PP} = V_{CC}. For device types 03, 04, 05, and 06, T_C = -55°C to +125°C, GND = 0 V, V_{CC} = 5 V, and for device types 05 and 06, V_{PP} = V_{CC}. For device types 07, 08, 09, 10, and 11, T_C = -55°C to 125°C, GND = 0 V, V_{CC} = 5 V.

2/ For device types 02, 05, 06, 07, 08, 09, 10, and 11 only, V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

3/ For device types 02, 05, 06, 07, 08, 09, 10, and 11 only, V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.

4/ For device types 01, 03, and 04, the input capacitance on pin 20 shall be 20 pF maximum.

5/ Output load: See figures 4 and 5; t_r and t_f <20 ns;
Input pulse levels: device types 01, 02, 05, and 06 = 0.8 V to 2.2 V; device types 03, 04, 07, 08, 09, 10, and 11 = .45 V to 2.4 V
Input timing reference level: device types 01, 02, 05, 06, 07, 08, 09, 10, and 11 = 1.0 V and 2.0 V; device types 03, 04 = 0.8 V to 2.0 V
Output timing reference level: 0.8 V and 2.0 V.

6/ If not tested, shall be guaranteed to the limits specified in table I.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.5.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.5.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 and table III.

3.5.3 Verification of erasure or programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern, or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and shall be removed from the lot.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE II. Electrical test requirements.

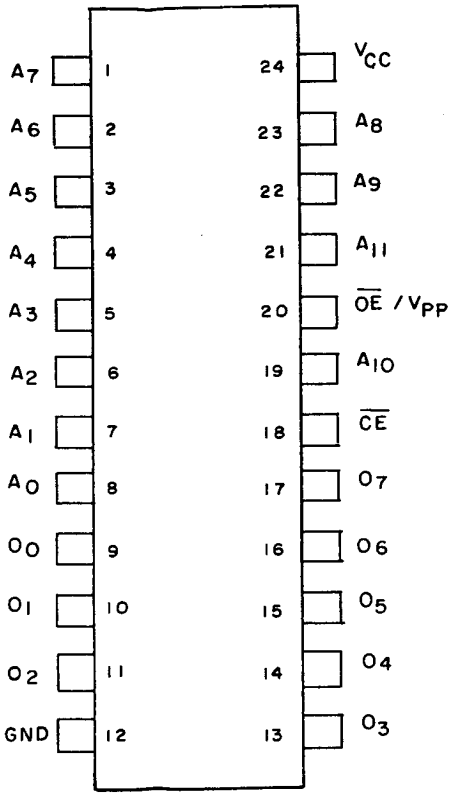
MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2

NOTES:
1. (*) Indicates PDA applies to subgroup 1.
2. Any or all subgroup may be combined when using a high speed tester.
3. Subgroup 7 shall consist of verifying the pattern specified.
4. For all electrical tests, the device shall be programmed to the pattern specified.

Device types 01, 03, 04, 07, 08, 09, 10, and 11

Dual-in-line package

Case J



Pin names

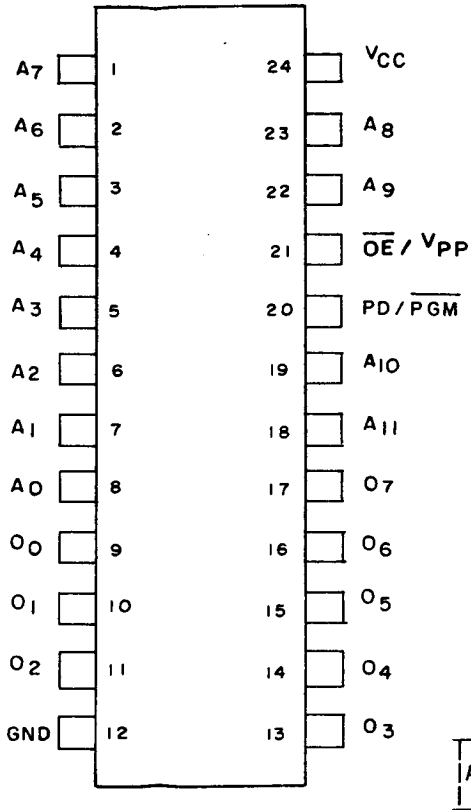
A_0-A_{11}	Addresses
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
O_0-O_7	Outputs

FIGURE 1. Terminal connections (top view).

Device types 02, 05, and 06

Dual-in-line package

Case J



Pin names

A_0-A_{11}	Addresses
PD/$\overline{PGM}$	Chip enable
O_0-O_7	Outputs
$\overline{OE}$/Vpp	Output enable

FIGURE 1. Terminal connections (top view) - Continued.

Device types 01, 03, 04, 07, 08, 09, 10, and 11

Pin Mode	$\overline{CE}$	$\overline{OE}/V_{pp}$	Outputs
Read	L	L	D_{OUT}
Standby	H	X	High Z
Program	L	V_{pp}	High Z
Program verify	L	L	D_{OUT}
Program inhibit	H	V_{pp}	High Z

L = Low level
H = High level

Device types 02, 05, and 06

Pin Mode	$PD/\overline{PGM}$	V_{pp}	Outputs
Read	L	H	D_{OUT}
Output disable	H	H	High Z
Power down	H	H	High Z
Start programming	H to L	V_{pp}	D_{IN}
Inhibit programming	H	V_{pp}	High Z

X = Don't care
V_{pp} = Program voltage

FIGURE 2. Truth tables.

Device types 01, 02, 03, 04, 05, 06, 07, 08, 09, 10, and 11

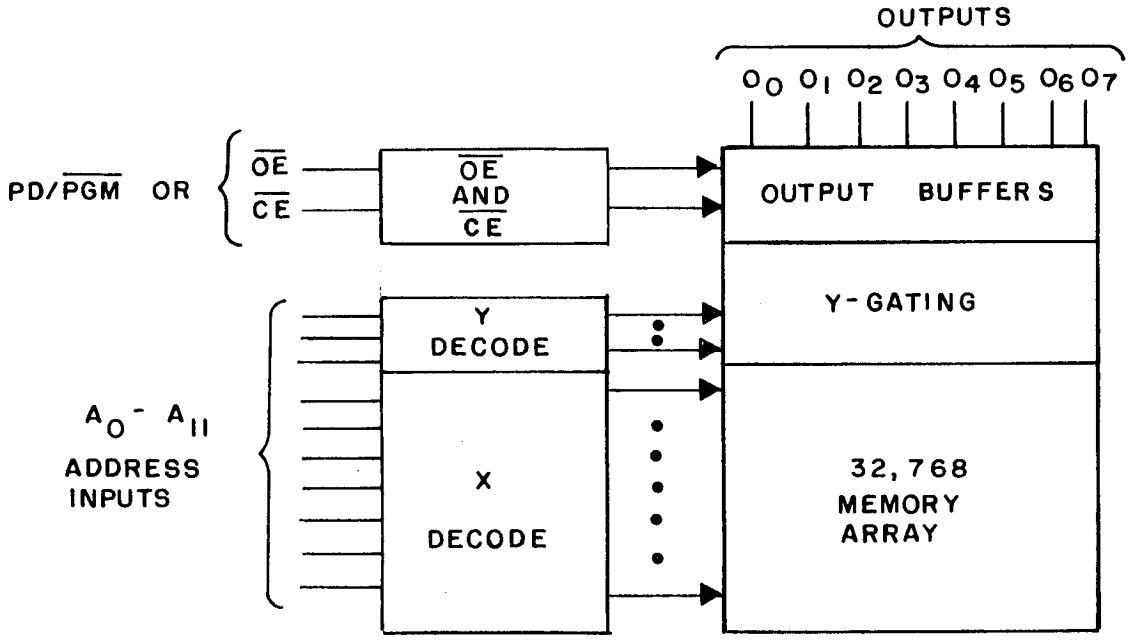
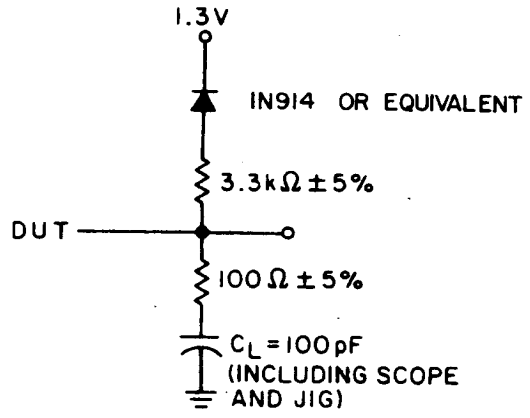


FIGURE 3. Block diagram.

Device types 01, 03, 04, 07, 08, 09, 10, and 11



Device types 02, 05, and 06

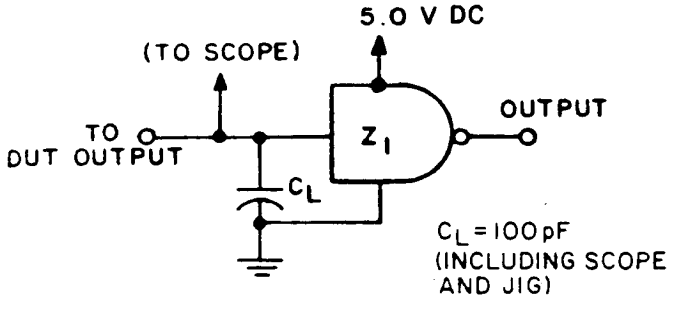
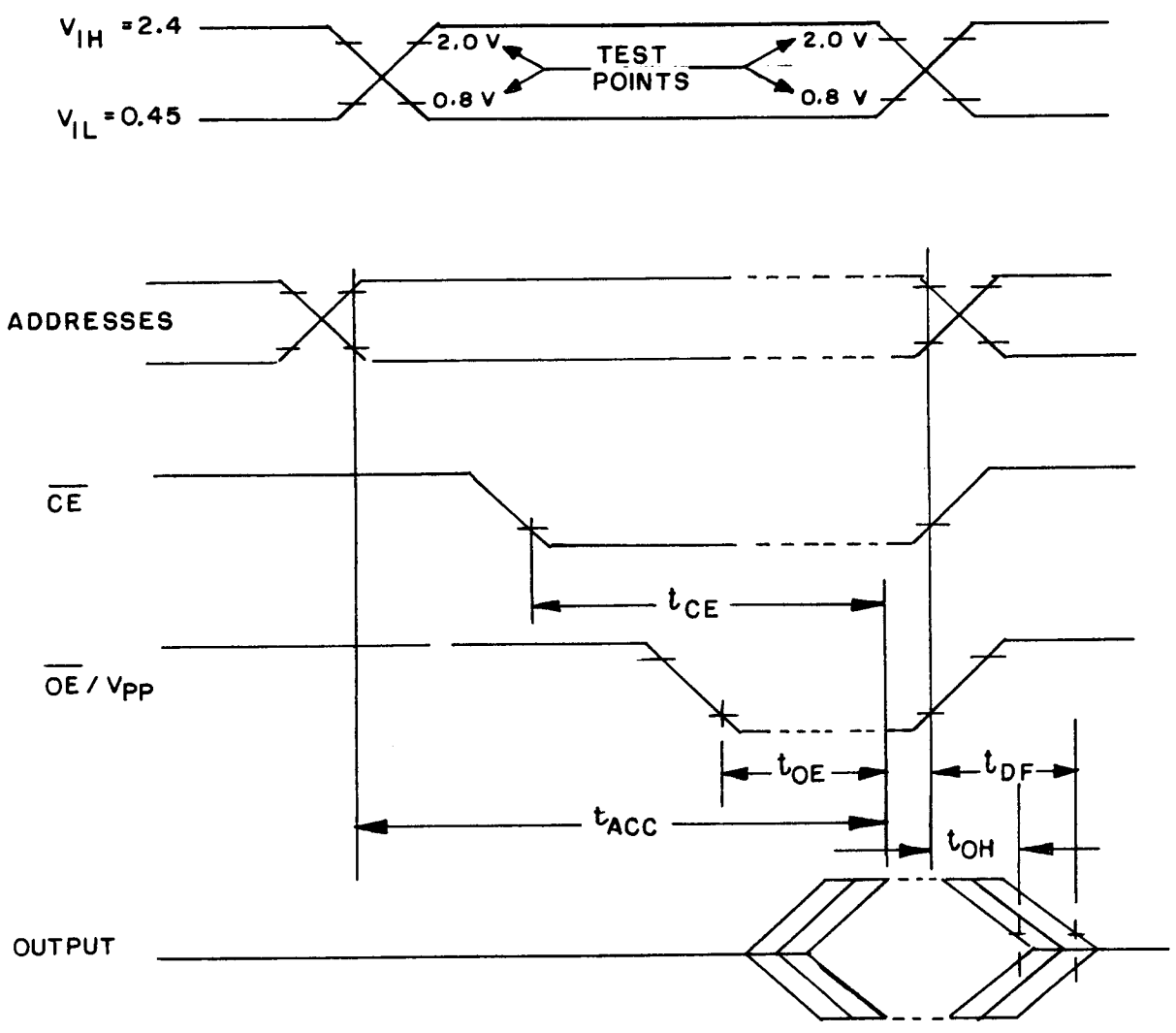


FIGURE 4. Output load.

Device types 01, 03, 04, 07, 08, 09, 10, and 11

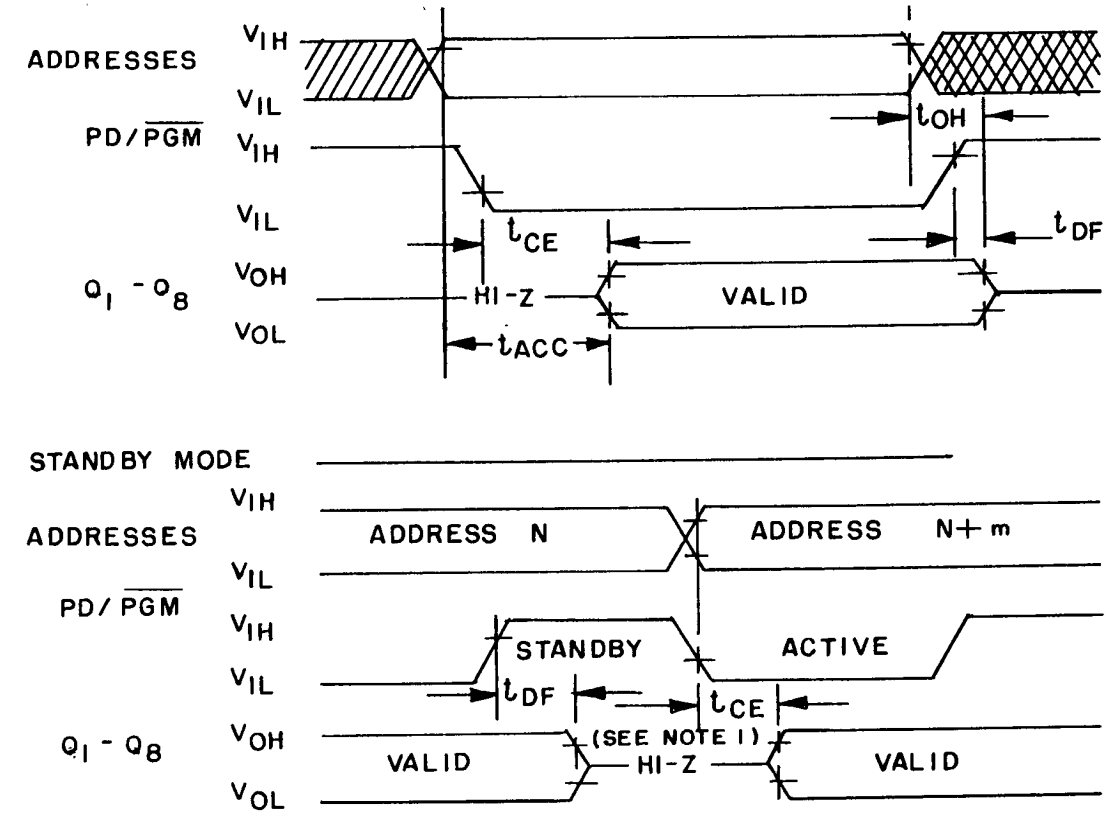


NOTE:
1. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

FIGURE 5. Timing diagram.

Device types 02, 05, and 06

READ CYCLE TIMING



NOTES:
1. V_{CC} shall be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. C_L = 100 pF includes jig and probe capacitance. Z_1 = TTL gate or equivalent.
3. Input rise and fall times $\leq$ 20 ns.
4. Input pulse levels 0.8 V to 2.2 V.
5. Timing measurement reference levels: Inputs 1.0 V and 2.0 V, Outputs 0.8 V and 2.0 V.
6. t_{CE} referenced to PD/$\overline{PGM}$ or the address, whichever occurs last.

FIGURE 5. Timing diagram - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps.

Margin test method A.

1. Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2).
2. Bake, unbiased, for 12 hours at 200°C.
3. Perform a margin test using Vm = V_{CC} = 6.0 V at 25°C using loose timing.
4. Erase device, then program 45 percent - 50 percent of the bits to a worst case speed pattern.
5. Perform dynamic burn-in (see 4.2a).
6. Perform a margin test using Vm = V_{CC} = 6.0 V at 25°C.
7. Perform 100 percent electrical testing at +125°C and -55°C. Perform 100 percent ac and dc electricals at 25°C.
8. Erase device (see 3.5.1), except devices submitted for groups A, B, C and D.
9. Verify erasure (see 3.5.3).

Margin test method B

1. Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2). The remaining cells shall provide a worst case speed pattern.
2. Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.
3. Perform a margin test using Vm = +6.0 V at 25°C using loose timing (i.e., t_{ACC} = 1 µs).
4. Perform dynamic burn-in (see 4.2a).

5. Margin at Vm = 6.0 V.

6. Perform electrical tests (see 4.2).

7. Erase (see 3.5.1), except devices submitted for groups A, B, C and D testing.

8. Verify erasure (see 3.5.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. All devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for group C and D testing).

e. Subgroup 7 shall consist of verifying the EPROM pattern specified.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing the devices shall be erased and verified.

4.4 Erasing procedure. The device is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 253.7 nm. The recommended integrated dose (i.e., UV intensity X exposure time) is 15 W-s/cm^2. An example of an ultraviolet source which can erase the device in 30 minutes is the Model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the EPROM should be placed about 1 inch from the lamp tubes. After erasure, all bits are in the high state.

4.5 Programming procedure.

4.5.1 Programming procedures for method A. The programming characteristics in table IIIA and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming the waveforms of figure 6 and programming characteristics of table IIIA shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be change to an "H" by ultraviolet light erasure (see 4.4).

c. Programming occurs when V_{pp} is 21.0 ±0.5 V and chip enable is brought low.

4.5.2 Programming procedures for method B. The programming characteristics in table IIIB and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming the waveforms of figure 7 and programming characteristics of table IIIB shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.4).

c. The circuit is set up for programming operation by setting PD/$\overline{PGM}$ input to V_{IH} and V_{pp} set to 25 V ±1.0 V. The word address is selected in the same manner as in the read mode. Data to be programmed, 8-Bits in parallel, are presented to the data lines (O_0 - O_7). Logic levels for address and data lines, and the supply voltages are the same as for the read mode. After address and data set up, one program pulse (V_{IL}) per address is applied to the program input (Pin 20). The programming time for a single bit is only 50 ms and for all bits is approximately 200 seconds.

4.5.3 Programming procedures for method C. The programming characteristics in table IIIC and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming the waveforms of figure 6 and programming characteristics of table IIIC shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programming "L" can be changed to an "H" by ultraviolet light erasure (see 4.4).

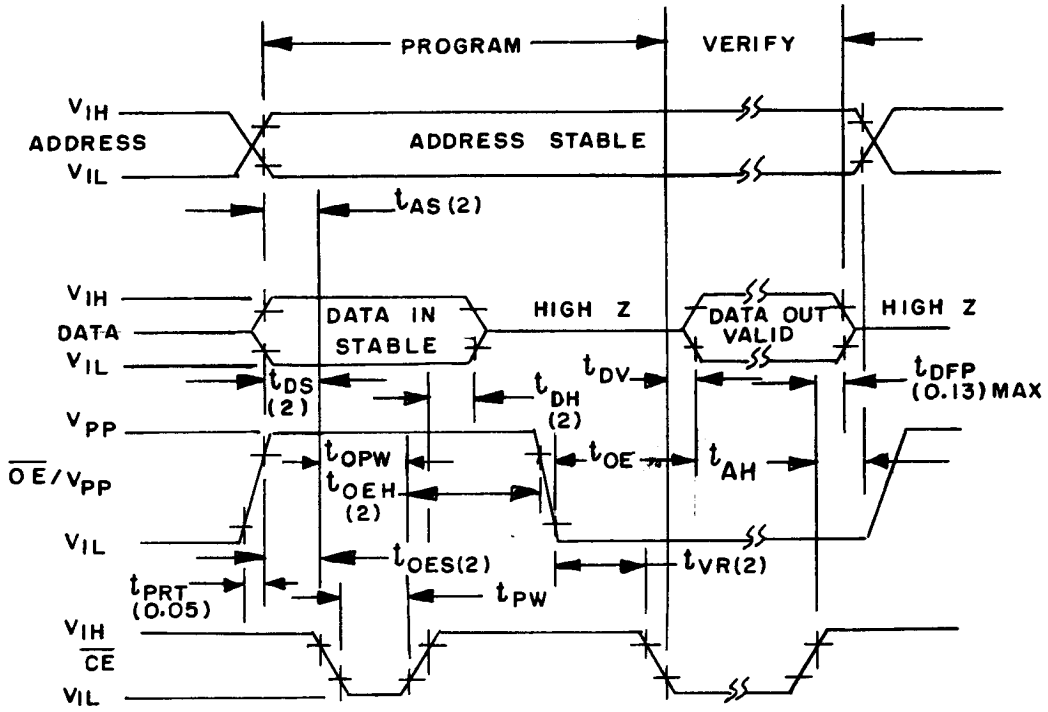
c. Programming occurs when V_{pp} is 12.0 V to 13.3 V and chip enable is brought low.

4.6 Programming procedure identification. The programming procedure to be utilized shall be identified by the manufacturer's circuit designator. The circuit designator is cross-referenced in 6.4 herein with the manufacturer's symbol or CAGE number.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

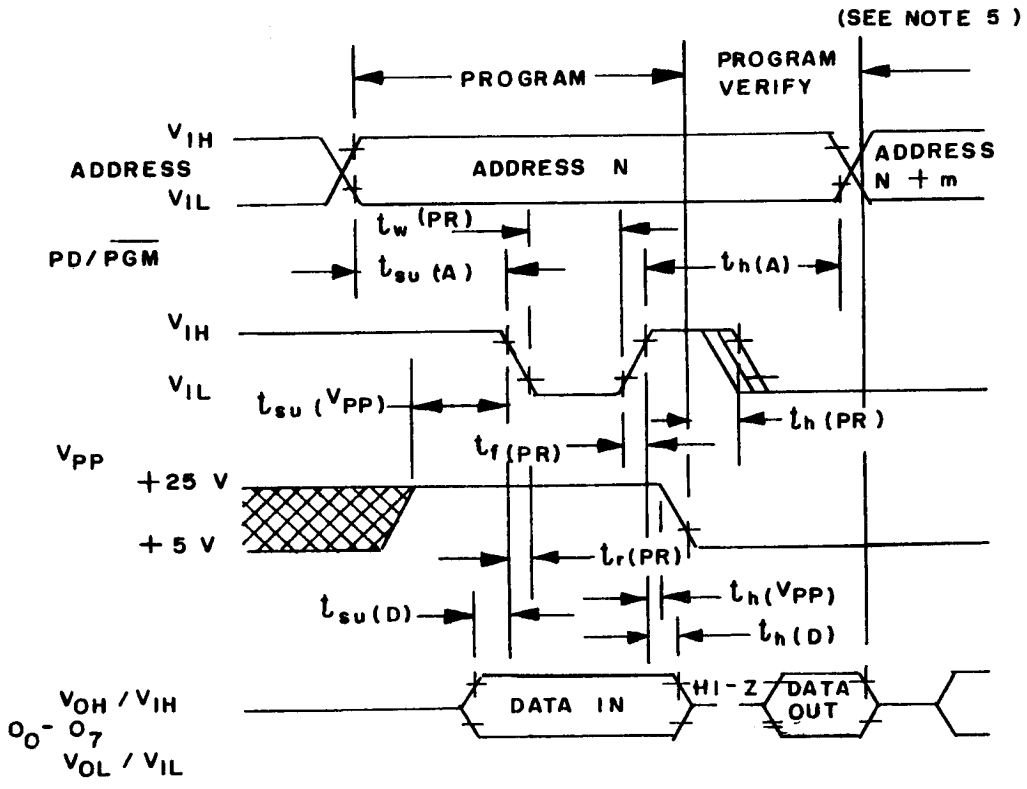
Device types 01, 03, 04, 07, 08, 09, 10, and 11



NOTES:
1. All times shown in parentheses are minimum and μs unless otherwise specified.
2. The input timing reference level is 0.8 V for as V_{IL} and 2 V for a V_{IH}.

FIGURE 6. Programming timing diagram for method A. and C.

Device types 02, 05, and 06



NOTES:
1. Input timing reference levels are 1.0 V and 2.0 V.
2. Output timing reference levels are 0.8 V and 2.0 V.
3. Input pulse rise and fall times (10% to 90%) are 20 ns.
4. Input pulse levels are 0.8 V to 2.2 V.
5. Program verify equivalent to read mode.

FIGURE 7. Programming timing diagram for method B.

TABLE IIIA. Programming characteristics for method A.

Symbol	Parameter	Limits			Units	Test conditions
		Min.	Typ.	Max.		
I_I	Input current (all inputs)			10	µA	$V_{IN} = V_{IL}$ or V_{IH}
V_{OL}	Output low voltage during verify			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output high voltage during verify	2.4			V	I_{OH} = -400 µA
I_{CC}	V_{CC} supply current		85	125	mA	
V_{IL}	Input low level (all inputs)	-0.1		0.8	V	
V_{IH}	Input high level (all inputs except $\overline{OE}/V_{pp}$)	2.0		$V_{CC}+1$	V	
I_{PP}	V_{pp} program current			30	mA	$\overline{CE} = V_{IL}$, V_{pp} = 21 V
V_{ID}	Aq intelligent identifier voltage	11.5		12.5	V	
t_{AS}	Address setup time	2			µs	
t_{OES}	$\overline{OE}$ setup time	2			µs	
t_{DS}	Data setup time	2			µs	
t_{AH}	Address hold time	0			µs	
t_{OEH}	$\overline{OE}$ hold time	2			µs	
t_{DH}	Data hold time	2			µs	
t_{DFP}	Chip enable high to output not driven	0		130	ns	
t_{DV}	Data valid from $\overline{CE}$			1	µs	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$
t_{PW}	$\overline{CE}$ pulse width during programming	45	50	55	ms	
t_{PRT}	$\overline{OE}$ pulse rise time during programming	50			ns	
t_{VR}	V_{pp} recovery time	2			µs	

NOTES:
1. For all switching characteristics and timing measurements, input pulse levels are 0.45 V to 2.4 V and V_{pp} = 21 V ±0.5 V during programming. All ac and dc measurements are made at 10% and 90% points with a 50% pattern.
2. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.
3. When programming the device, a 0.1 µF capacitor is required across $\overline{OE}/V_{pp}$ and ground to suppress spurious voltage transients which may damage the device.

TABLE IIIB. Programming characteristics for method B.

Symbol	Parameter	Limits			Units
		Min.	Typ. +	Max.	
$t_{W(PR)}$	Pulse width, program pulse	45	50	55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			µs
$t_{su(D)}$	Data setup time	2			µs
$t_{su(V_{pp})}$	Setup time from V_{pp}	0			ns
$t_{h(A)}$	Address hold time	2			µs
$t_{h(D)}$	Data hold time	2			µs
$t_{h(PR)}$	Program pulse hold time	0			ns
$t_{h(V_{pp})}$	V_{pp} hold time	0			ns
I_{pp2}	Program pulse current			30	mA

Typical values are at nominal voltages.

NOTES:
1. For all switching characteristics and timing measurements, input pulse levels are 0.65 V to 2.2 V and V_{pp} = 25 V ±1 V during programming. All ac and dc measurements are made at 10% and 90% points with a 50% pattern.
2. Common test conditions apply for t_{DF} except during programming. For t_{ACC} and t_{DF}, PD/$\overline{PGM}$ = V_{IL}.

TABLE IIIC. Programming characteristics for method C.

Symbol	Parameter	Limits			Units	Test conditions
		Min.	Typ.	Max.		
I_I	Input current (all inputs)			10	µA	$V_{IN} = V_{IL}$ or V_{IH}
V_{OL}	Output low voltage during verify			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output high voltage during verify	2.4			V	I_{OH} = -400 µA
I_{CC}	V_{CC} supply current			100	mA	
V_{IL}	Input low level (all inputs)	-0.1		0.8	V	
V_{IH}	Input high level (all inputs except $\overline{OE}/V_{pp}$)	2.0		$V_{CC}+1$	V	
I_{PP}	V_{pp} program current			30	mA	$\overline{CE} = V_{IL}$, V_{pp} = 12.5 V
V_{ID}	Ag intelligent identifier voltage	11.5		12.5	V	
t_{AS}	Address setup time	2			µs	
t_{OES}	$\overline{OE}$ setup time	2			µs	
t_{DS}	Data setup time	2			µs	
t_{AH}	Address hold time	2			µs	
t_{OEH}	$\overline{OE}$ hold time	2			µs	
t_{DH}	Data hold time	2			µs	
t_{DFP}	Chip enable high to output not driven	0		130	ns	
t_{OE}	Data valid from $\overline{OE}$			150	ns	
t_{DV}	Data valid from $\overline{CE}$			450	ns	
t_{PW}	PGM pulse width during programming	.95	1.0	1.05	ms	
t_{OPW}	PGM pulse width during over programming	1.9	2.0	55	ms	

See footnotes at end of table.

TABLE IIIC. Programming characteristics for method C - Continued.

Symbol	Parameter	Limits			Units	Test conditions
		Min.	Typ.	Max.		
t_{VPS}	V_{PP} setup time	2			µs	
t_{VCS}	V_{CC} setup time	2			µs	
t_{CCS}	$\overline{CE}$ setup time	2			µs	

NOTES:
1. For all switching characteristics and timing measurements, input pulse levels are 0.8 V to 2.0 V and V_{PP} = 12.0 V to 13.3 V during programming. All ac and dc measurements are made at 10% and 90% points with a 50% pattern.
2. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.
3. When programming the 2732B, a 0.1 µF capacitor is required across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/222XXBJX.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.6) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number	Replacement military specification part number 1/	Programming method
8001201JX 2/	34649	MD2732/B		A
8001202JX 3/	4/	SMJ2532-45JS	M38510/22201BJX	B
8001203JX	34649	MD2732A25/B		A
	4/	AM2732A-25/BJA		A
8001204JX	34649	MD2732A45/B		A
	4/	AM2732A-45/BJA		A
8001205JX	4/	SMJ2532-35JM		B
8001206JX	4/	SMJ2532-45JM	M38510/22201BJX	B
8001207JX	34335	AM2732B-150/BJA		C
8001208JX	34335	AM2732B-200/BJA		C

See footnotes at end of table.

Military drawing part number	Vendor CAGE number	Vendor similar part number	Replacement military specification part number 1/	Programming method
8001209JX	34335	AM2732B-250/BJA		C
8001210JX	34335	AM2732B-300/BJA		C
8001211JX	34335	AM2732B-450/BJA		C

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ Device type 01 is inactive for new design. Device type 04 at full military temperature range is the preferred device.
3/ Device type 02 is inactive for new design. Device type 06 at full military temperature range is the preferred device.
4/ Not available from any approved source.

Vendor CAGE number	Vendor name and address	Margin test method
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051	B
34335	Advanced Micro Devices 901 Thompson Place Sunnyvale, CA 94086	A

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