

P4C188/P4C188L ULTRA HIGH SPEED 16K x 4 STATIC CMOS RAMS (SCRAMS)

★ FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
 - 12/15/20/25 ns (Commercial)
 - 20/25/35/45/55 ns (Military)
- Low Power (Commercial/Military)
 - 715 mW Active – 12/15
 - 550/660 mW Active – 20/25/35/45/55
 - 193/220 mW Standby (TTL Input)
 - 83/110 mW Standby (CMOS Input) P4C188
 - 15 mW Standby (CMOS Input) P4C188L (Military)

- Single 5V±10% Power Supply
- Data Retention with 2.0V Supply (P4C188L Military)
- Three-State Outputs
- TTL/CMOS Compatible Outputs
- Fully TTL Compatible Inputs
- Produced with PACE Technology™
- Standard Pinout (JEDEC Approved)
 - 22-Pin 300 mil DIP
 - 24-Pin 300 mil SOJ
 - 22-Pin 290 x 490 mil LCC

★ DESCRIPTION

The P4C188 and P4C188L are 65,536-bit ultra high speed static RAMs organized as 16K x 4. The CMOS memories require no clocks or refreshing and have equal access and cycle times. Inputs and outputs are fully TTL-compatible. The RAMs operate from a single 5V±10% tolerance power supply. With battery backup, data integrity is maintained for supply voltages down to 2.0V. Current drain is typically 10 µA from a 2.0V supply.

Access times as fast as 12 nanoseconds are available, permitting greatly enhanced system speeds. CMOS is utilized to reduce power consumption to a low 715mW active, 193mW standby and only 5mW in the P4C188L version. The P4C188 and P4C188L are members of a family of PACE RAM™ products offering super fast access times never before available at these complexity levels in TTL-compatible bipolar or CMOS technologies.

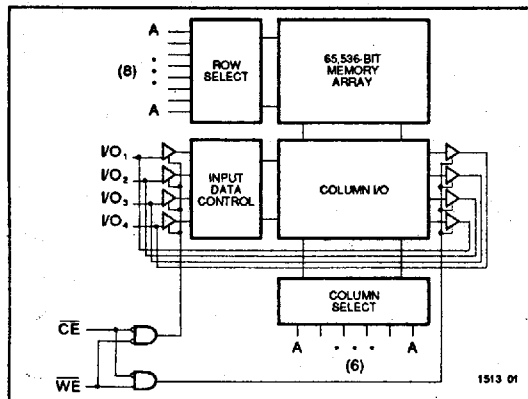
The P4C188 and P4C188L are manufactured with PACE Technology which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths giving 500 picoseconds loaded* internal gate delays.

PACE Technology includes two level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

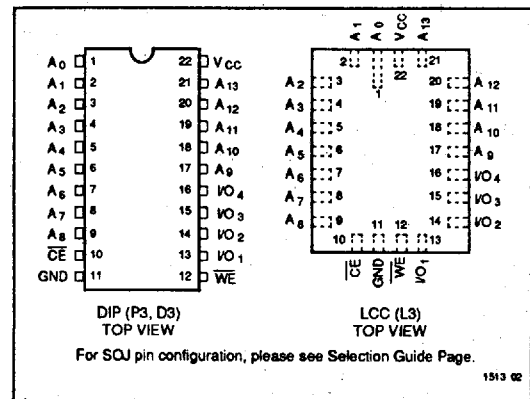
The P4C188 and P4C188L are available in 22-pin 300 mil DIP, 24-pin 300 mil SOJ and 22-pin LCC packages providing excellent board level densities.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.
For a fan-in/fan-out of 1, the internal gate delay is 200 picoseconds at room temperature and 5.0V.

★ FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



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P4C188/188L

MAXIMUM RATINGS⁽¹⁾

T-46-23-10

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to $V_{CC} + 0.5$	V
T_A	Operating Temperature	-55 to +125	°C

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Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

1513 Tbl 02

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade ⁽²⁾	Ambient Temperature	GND	V_{CC}
Military	-55 to +125°C	0V	5.0V ± 10%

1513 Tbl 03

Grade ⁽²⁾	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

1513 Tbl 04

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage⁽²⁾

Symbol	Parameter	Test Conditions	P4C188		P4C188L		Unit
			Min	Max	Min	Max	
V_{IH}	Input High Voltage		2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage		-0.5 ⁽³⁾	0.8	-0.5 ⁽³⁾	0.8	V
V_{HC}	CMOS Input High Voltage		$V_{CC} - 0.2$	$V_{CC} + 0.5$	$V_{CC} - 0.2$	$V_{CC} + 0.5$	V
V_{LC}	CMOS Input Low Voltage		-0.5 ⁽³⁾	0.2	-0.5 ⁽³⁾	0.2	V
V_{CD}	Input Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-1.2		-1.2	V
V_{OL}	Output Low Voltage (TTL Load)	$I_{OL} = +8 \text{ mA}, V_{CC} = \text{Min.}$		0.4		0.4	V
V_{OH}	Output High Voltage (TTL Load)	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min.}$	2.4		2.4		V
I_{LI}	Input Leakage Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND to } V_{CC}$	Mil. -10 Com'l. -5	+10 +5	-5 n/a	+5 n/a	µA
I_{LO}	Output Leakage Current	$V_{CC} = \text{Max.}, \overline{CE} = V_{IH},$ $V_{OUT} = \text{GND to } V_{CC}$	Mil. -10 Com'l. -5	+10 +5	-5 n/a	+5 n/a	µA

n/a = Not Applicable

1513 Tbl 05

CAPACITANCES⁽⁴⁾

($V_{CC} = 5.0V, T_A = 25^\circ\text{C}, f = 1.0\text{MHz}$)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	pF

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Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	7	pF

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Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V_{IH} and I_{IL} not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20ns.
- This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS

Over recommended operating temperature and supply voltage⁽²⁾

T-46-23-10

Symbol	Parameter	Test Conditions	P4C188		P4C188L		Unit
			Min	Max	Min	Max	
I_{CC}	Dynamic Operating Current – 12, 15	$V_{CC} = \text{Max.}, f = \text{Max.},$ Outputs Open	Mil. Com'l.	— n/a	— 130	— n/a	mA
I_{CC}	Dynamic Operating Current – 20, 25, 35, 45, 55	$V_{CC} = \text{Max.}, f = \text{Max.},$ Outputs Open	Mil. Com'l.	— 120	— 100	— 120	mA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH},$ $V_{CC} = \text{Max.},$ $f = \text{Max.},$ Outputs Open	Mil. Com'l.	— 40	— 35	— 40	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{HC},$ $V_{CC} = \text{Max.},$ $f = 0,$ Outputs Open, $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	Mil. Com'l.	— 20	— 15	— 2.7	mA

n/a = Not Applicable

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DATA RETENTION CHARACTERISTICS (P4C188L Military Temperature Only)

Symbol	Parameter	Test Condition	Min	Typ.* $V_{CC} =$		Max $V_{CC} =$		Unit
				2.0V	3.0V	2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		10	15	600	900	μA
t_{CDR}	Chip Deselect to Data Retention Time		0					ns
$t_R^{\dagger}$	Operation Recovery Time		$t_{RC}^{\ddagger}$					ns

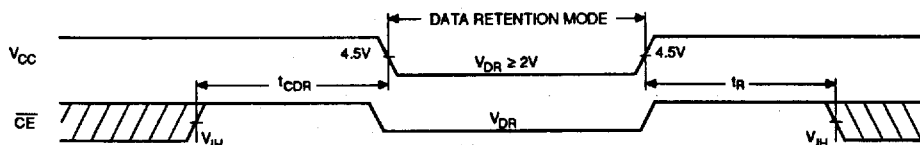
* $T_A = +25^{\circ}C$

$t_{RC}^{\ddagger}$ = Read Cycle Time

$t_R^{\dagger}$ This parameter is guaranteed but not tested.

1513 Tbl 09

DATA RETENTION WAVEFORM



1513 03

AC CHARACTERISTICS—READ CYCLE

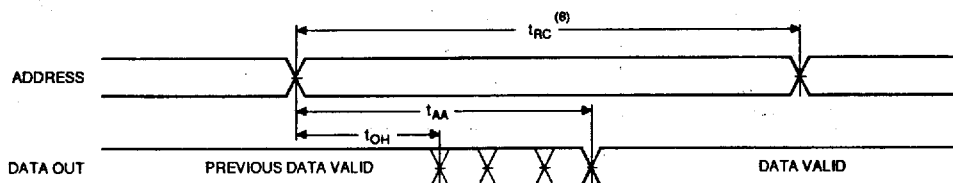
($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

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Sym.	Parameter	-12		-15		-20		-25		-35		-45		-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	12		15		20		25		35		45		55		ns
t_{AA}	Address Access Time		12		15		20		25		35		45		55	ns
t_{AC}	Chip Enable Access Time		12		15		20		25		35		45		55	ns
t_{OH}	Output Hold from Address Change	1		2		3		3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		3		3		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		6		6		8		10		20		25		25	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		12		15		20		25		35		45		55	ns

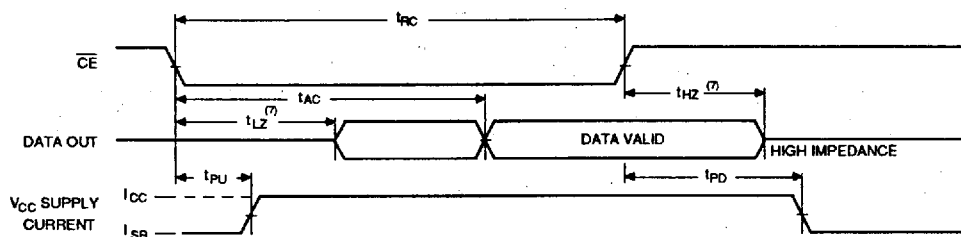
1513 Tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1⁽⁶⁾



1513 04

TIMING WAVEFORM OF READ CYCLE NO. 2⁽⁶⁾



1513 05

Notes:

5. $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{WE}$ is HIGH, and address must be valid prior to or coincident with $\overline{CE}$ transition LOW.
7. Transition is measured $\pm 200mV$ from steady state voltage prior to

change with specified loading in Figure 1. This parameter is sampled and not 100% tested.

8. Read Cycle Time is measured from the last valid address to the first transitioning address.

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AC CHARACTERISTICS—WRITE CYCLE

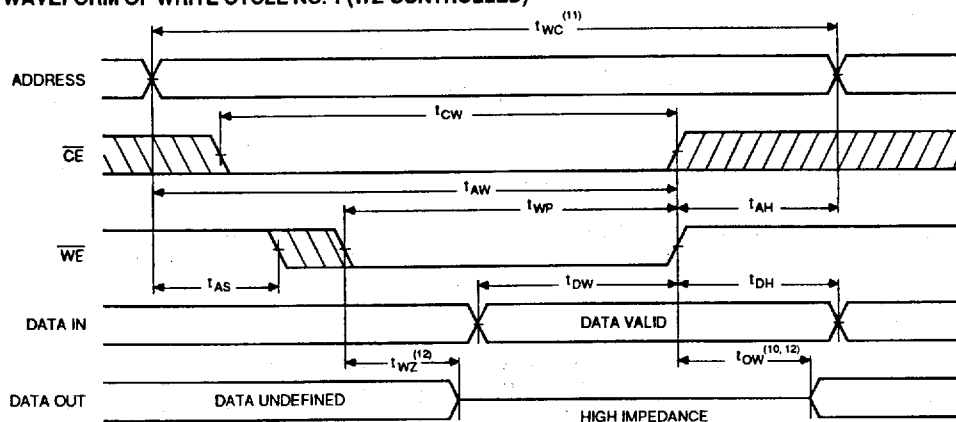
($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

Sym.	Parameter	-12		-15		-20		-25		-35		-45		-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	12		13		20		25		35		45		55		ns
t_{CW}	Chip Enable Time to End of Write	8		10		13		15		25		35		45		ns
t_{AW}	Address Valid to End of Write	8		10		15		20		25		35		40		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	9		10		13		15		25		35		45		ns
t_{AH}	Address Hold Time from End of Write	0		0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	6		7		8		10		15		20		25		ns
t_{DH}	Data Hold Time	0		0		0		0		0		5		5		ns
t_{WZ}	Write Enable to Output in High Z		6		6		8		10		15		20		25	ns
t_{OW}	Output Active from End of Write	2		2		2		2		3		3		3		ns

1513 TM 11

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TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)⁽⁹⁾



1513 06

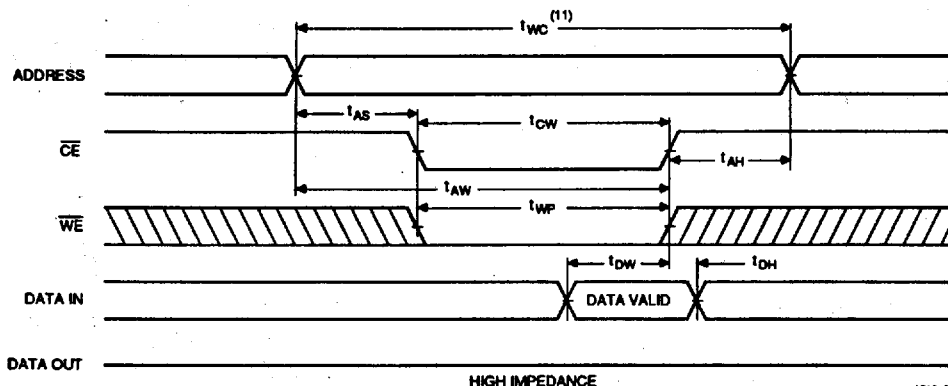
Notes:

9. $\overline{CE}$ and $\overline{WE}$ must be LOW for WRITE cycle.
10. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
11. Write Cycle Time is measured from the last valid address to the first transition address.

12. Transition is measured $\pm 200mV$ from steady state voltage prior to change with specified loading in Figure 1. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CE CONTROLLED) ^(a)

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HIGH IMPEDANCE

1513 07

AC TEST CONDITIONS

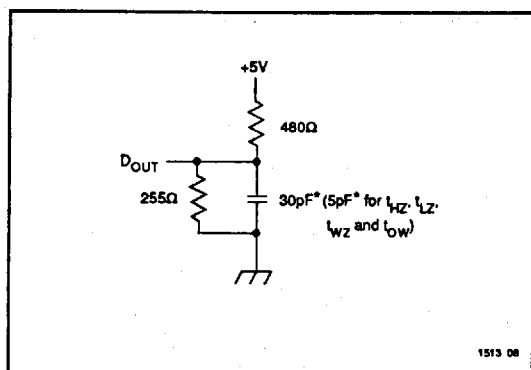
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

1513 TM 12

TRUTH TABLE

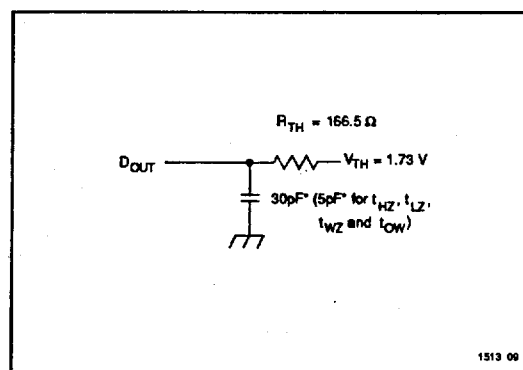
Mode	CE	WE	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	D _{OUT}	Active
Write	L	L	D _{IN}	Active

1513 TM 13



1513 08

Figure 1. Output Load



1513 09

Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:

Because of the ultra-high speed of the P4C188/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor is also required between V_{CC} and ground. To avoid signal

reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

PACKAGE SUFFIX

Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
J	Plastic SOJ, 300 mil wide standard
C	Sidebrazed DIP, 300 mil wide
L	Leadless Chip Carrier (ceramic)
D	CERDIP, 300 mil wide standard

1513 TM 14

TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C to +70°C.
M	Military Temperature Range, -55°C to +125°C.
MB	Mil. Temp. with MIL-STD-883D Class B compliance

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SELECTION GUIDE

The P4C188/L is available in the following temperature, speed and package options. The P4C188L is only available in Military Temperature range with access times of 25 ns or slower. The P4C188/188L is available to Standardized Military Drawing 5962-86859 and 5962-89692. Check Mil-Bul-103 for current listing of part types.

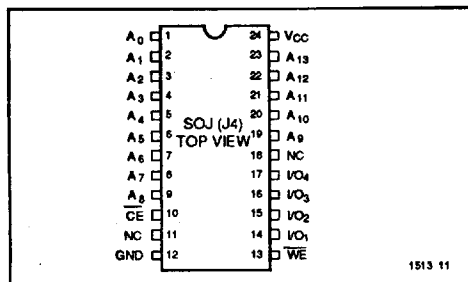
Temperature Range	Speed (ns)	12	15	20	25	35	45	55
Package								
Commercial	Plastic DIP	-12PC	-15PC	-20PC	-25PC	N/A	N/A	N/A
	Plastic SOJ	-12JC	-15JC	-20JC	-25JC	N/A	N/A	N/A
	CERDIP	-12CC	-15CC	-20DC	-25DC	N/A	N/A	N/A
	LCC	-12LC	-15LC	-20LC	-25LC	N/A	N/A	N/A
Military Temp.	CERDIP	N/A	N/A	-20DM	-25DM	-35DM	-45DM	-55DM
	LCC	N/A	N/A	-20LM	-25LM	-35LM	-45LM	-55LM
Military Processed*	CERDIP	N/A	N/A	-20CMB	-25DMB	-35DMB	-45DMB	-55DMB
	LCC	N/A	N/A	-20LMB	-25LMB	-35LMB	-45LMB	-55LMB

* Military temperature range with MIL-STD-883 Revision D, Class B processing.

N/A = Not available

1513 TM 16

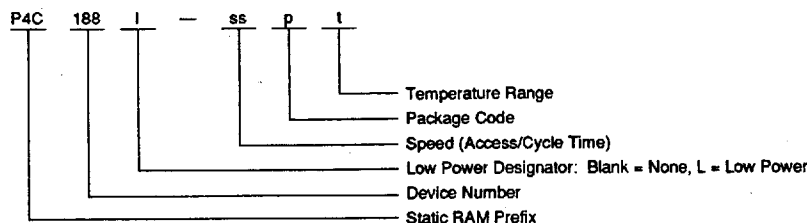
SOJ PIN CONFIGURATION



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ORDERING INFORMATION

The following part numbering scheme is used for



L = Ultra-low standby power designator L, if needed.

ss = Speed (access/cycle time in ns), e.g., 25, 35

p = Package code, i.e., P, J, D, L.

t = Temperature range, i.e., C, M, MB.

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