REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
E	Change to military drawing format. Change code ident. to 67268. Add vendor CAGE no. 27014 for device type 06CX. Page 11; table I: Change limits for $\Delta V_{IO}/\Delta T$. Inactivate package C for device types 02 and 05. Add device types 012X, 022X, 032X, 042X, 052X, and 062X. Editorial changes throughout.	11 FEB 1988	R.P. Evans

CURRENT CAGE CODE 67268

REV																										
PAGE																										
REV STATUS OF PAGES	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E								
	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17								

Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
30 June 1981

AMSC N/A

PREPARED BY: Charles E Besore

CHECKED BY: Da Di Cenzo

APPROVED BY: Robert P. Evans

SIZE: A

CODE IDENT. NO.: 14933

REV: E

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, LINEAR, BI-FET OPERATIONAL AMPLIFIERS, MONOLITHIC SILICON

DWG NO. 81023

PAGE 1 OF 17

5962-E486

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

81023	01	C	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit
01	061	Single operational amplifier, Bi-FET, low power.
02	062	Dual operational amplifier, Bi-FET, low power.
03	064	Quad operational amplifier, Bi-FET, low power.
04	071	Single operational amplifier, Bi-FET, low power.
05	072	Dual operational amplifier, Bi-FET, low power.
06	074, 147	Quad operational amplifier, Bi-FET, low power.

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
C	D-1 (14-lead, 1/4" X 3/4"), dual-in-line package
D	F-2 (14-lead, 1/4" X 3/8"), flat package
H	F-4 (10-lead, 1/4" X 1/4"), flat package
P	D-4 (8-lead, 1/4" X 3/8"), dual-in-line package
2	C-2 (20-terminal, .350" x .350"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	±18 V dc
Input voltage range 1/	±15 V dc
Differential input voltage range	±30 V dc
Storage temperature range	-65°C to +150°C
Output short-circuit duration 2/	Unlimited
Lead temperature (soldering, 60 seconds)	+300°C
Power dissipation, (P_D) (internally limited): 3/	
Case C	300 mW at T_A = +25°C
Case D	350 mW at T_A = +25°C
Case H	330 mW at T_A = +25°C
Case P	400 mW at T_A = +25°C
Case 2	280 mW at T_A = +25°C

1/ For supply voltages less than ±15 V dc, the maximum input voltage is equal to the supply voltage.
2/ Short circuit may be to ground or either power supply. Rating applied to +125°C case temperature or +75°C ambient temperature.
3/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

1.4 Recommended operating conditions.

Supply voltage range	±5 V dc to ±15 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases C, D, H, P, and 2	See MIL-M-38510 (appendix C)
Thermal resistance, junction-to-ambient (θ_{JA}):	
Cases C and P	120°C/W
Case D	140°C/W
Case H	185°C/W
Case 2	65°C/W

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended ambient operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics (device types 01 and 02).

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$, unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Input offset voltage	V_{IO}	$\pm V_{CC} = \pm 15$ V; ± 9 V $V_{CM} = 0$ V	$T_A = +25°C$	1	-6	6	mV
		$\pm V_{CC} = \pm 15$ V at $V_{CM} = 0$ V	$T_A = -55°C$, $+125°C$	2, 3	-9	9	mV
Input offset voltage temperature sensitivity 1/	$\frac{\Delta V_{IO}}{\Delta T}$	$V_{CM} = 0$ V		1, 2, 3	-60	60	µV/°C
Input offset current	I_{IO} 2/	$V_{CM} = 0$ V	$T_A = +25°C$	1	-100	100	pA
			$T_A = +125°C$	2	-20	20	nA
Input bias current	$+I_{IB}$ 3/	$V_{CM} = 0$ V	$T_A = +25°C$	1	-200	200	pA
			$T_A = +125°C$	2	-50	50	nA
	$-I_{IB}$ 3/	$V_{CM} = 0$ V	$T_A = +25°C$	1	-200	200	pA
			$T_A = +125°C$	2	-50	50	nA

See footnotes at end of table.

☆ U.S. GOVERNMENT PRINTING OFFICE: 1987 - 549-096

TABLE I. Electrical performance characteristics (device types 01 and 02) - Continued.

Test	Symbol	Conditions $-55°C \leq T_A \leq 125°C$, unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Power supply rejection ratio	PSRR	$\pm V_{CC}$ = +15 V; T_A = 25°C $\pm V_{CC}$ = ±9 V		1	80	---	dB
Input voltage common mode rejection 4/	CMRR	-11.5 V ≤ VCM ≤ 11.5 V; T_A = 25°C		1	80	---	dB
Supply current (per amplifier)	I_{CC}	T_A = 25°C		1	---	0.3	mA
Output voltage swing (maximum)	$+V_{op}$, $-V_{op}$	R_L = 10 kΩ		4, 5, 6	±10	---	V
Open loop voltage gain (single ended) 5/	Avs(+) Avs(-)	$R_L \geq$ 10 kΩ, V_{OUT} = -10 to 10 V		4, 5, 6	4	---	V/mV
Slew rate	SR(+) and SR(-)	V_{IN} = ±5 V; Av = 1	T_A = +25°C	7	2	---	V/µs
			T_A = -55°C, +125°C 1/	8	0.7	---	V/µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 03) - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$, unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Input offset voltage	V_{IO}	$\pm V_{CC} = \pm 15$ V; ± 9 V; $T_A = +25°C$ $V_{CM} = 0$ V		1	-9	9	mV
		$\pm V_{CC} = \pm 15$ V at $V_{CM} = 0$ V; $T_A = -55°C$, $+125°C$		2, 3	-15	15	mV
Input offset voltage temperature sensitivity 1/	$\frac{\Delta V_{IO}}{\Delta T}$	$V_{CM} = 0$ V		1, 2, 3	-60	60	µV/°C
Input offset current	I_{IO} 2/	$V_{CM} = 0$ V	$T_A = +25°C$	1	-100	100	pA
			$T_A = +125°C$	2	-20	20	nA
Input bias current	$+I_{IB}$ 3/	$V_{CM} = 0$ V	$T_A = +25°C$	1	-200	200	pA
			$T_A = +125°C$	2	-50	50	nA
	$-I_{IB}$ 3/	$V_{CM} = 0$ V	$T_A = +25°C$	1	-200	200	pA
			$T_A = +125°C$	2	-50	50	nA

See footnotes at end of table.

☆ U.S. GOVERNMENT PRINTING OFFICE: 1987—549-096

TABLE I. Electrical performance characteristics (device type 03) - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$, unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Power supply rejection ratio	PSRR	$\pm V_{CC}$ = ±15 V; ±9 V, T_A = +25°C		1	80	---	dB
Input voltage common mode rejection 4/	CMRR	-11.5 V $\le V_{CM} \le$ 11.5 V T_A = +25°C		1	80	---	dB
Supply current (per amplifier)	I_{CC}	T_A = +25°C		1	---	0.3	mA
Output voltage swing (maximum)	$+V_{op}$, $-V_{op}$	R_L = 10 kΩ		4, 5, 6	±10	---	V
Open loop voltage gain (single ended) 5/	Avs(+) Avs(-)	V_{OUT} = -10 to 10 V $R_L \ge$ 10 kΩ		4, 5, 6	4	---	V/mV
Slew rate	SR(+) and SR(-)	V_{IN} = ±5 V Av = 1	T_A = +25°C	7	2	---	V/µs
			T_A = -55°C, +125°C 1/	8	0.7	---	V/µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device types 04 and 05) - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$, unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Input offset voltage	V_{IO}	$\pm V_{CC} = \pm 15$ V; ± 9 V; $T_A = +25°C$ $V_{CM} = 0$ V		1	-6	6	mV
		$\pm V_{CC} = \pm 15$ V at $V_{CM} = 0$ V $T_A = -55°C$, $+125°C$		2, 3	-9	9	mV
Input offset voltage temperature sensitivity 1/	$\frac{\Delta V_{IO}}{\Delta T}$	$V_{CM} = 0$ V		1, 2, 3	-30	30	µV/°C
Input offset current	I_{IO} 2/	$V_{CM} = 0$ V	$T_A = +25°C$	1	-100	100	pA
			$T_A = +125°C$	2	-20	20	nA
Input bias current	$+I_{IB}$ 3/	$V_{CM} = 0$ V	$T_A = +25°C$	1	-200	200	pA
			$T_A = +125°C$	2	-50	50	nA
	$-I_{IB}$ 3/	$\pm V_{CC} = \pm 15$ V; $V_{CM} = 0$ V; $t \le 25$ ms	$T_A = +25°C$	1	-200	200	pA
			$T_A = +125°C$	2	-50	50	nA
Power supply rejection ratio	PSRR	$\pm V_{CC} = \pm 15$ V; ± 9 V; $T_A = +25°C$		1	80	---	dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device types 04 and 05) - Continued.

Test	Symbol	Conditions $-55°C \leq T_A \leq 125°C$, unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Input voltage common mode rejection 4/	CMRR	$-11\ V \leq V_{CM} \leq 11\ V$; $T_A = +25°C$	1	80	---	dB
Supply current (per amplifier)	I_{CC}	$T_A = +25°C$	1	---	3.5	mA
Output voltage swing (maximum)	$+V_{op}$ $-V_{op}$	$R_L = 10\ k\Omega$	4, 5, 6	±12	---	V
		$R_L = \pm 2\ k\Omega$	4, 5, 6	±10	---	V
Open loop voltage gain (single ended) 5/	Avs(+) Avs(-)	$V_{OUT} = -10$ to 10 V $R_L \geq 2\ k\Omega$	4	35	---	V/mV
			5, 6	15	---	V/mV
Slew rate	SR(+) and SR(-)	$V_{IN} = \pm 5$ V; Av = 1	7	8	---	V/µs
			8	5	---	V/µs

See footnotes at end of table.

☆ U.S. GOVERNMENT PRINTING OFFICE: 1987—549-096

TABLE I. Electrical performance characteristics (device type 06) - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$, unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Input offset voltage	V_{IO}	$\pm V_{CC} = \pm 15$ V; ± 9 V; $T_A = +25°C$ $V_{CM} = 0$ V		1	-9	9	mV
		$\pm V_{CC} = \pm 15$ V at $V_{CM} = 0$ V $T_A = -55°C, +125°C$		2, 3	-15	15	mV
Input offset voltage temperature sensitivity 1/	$\frac{\Delta V_{IO}}{\Delta T}$	$V_{CM} = 0$ V		1, 2, 3	-50	50	µV/°C
Input offset current	I_{IO} 2/	$V_{CM} = 0$ V	$T_A = +25°C$	1	-100	100	pA
			$T_A = +125°C$	2	-20	20	nA
Input bias current	$+I_{IB}$ 3/	$V_{CM} = 0$ V	$T_A = +25°C$	1	-200	200	pA
			$T_A = +125°C$	2	-50	50	nA
	$-I_{IB}$ 3/	$V_{CM} = 0$ V	$T_A = +25°C$	1	-200	200	pA
			$T_A = +125°C$	2	-50	50	nA
Power supply rejection ratio	+PSRR	$\pm V_{CC} = \pm 15$ V; ± 9 V; $T_A = +25°C$		1	80	---	dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device type 06) - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$, unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Input voltage common mode rejection 4/	CMRR	$-11\ V \le V_{CM} \le 11\ V$; $T_A = +25°C$		1	80	---	dB
Supply current (per amplifier)	I_{CC}	$T_A = +25°C$		1	---	3.5	mA
Output voltage swing (maximum)	$+V_{op}$ $-V_{op}$	$R_L = 10\ k\Omega$		4, 5, 6	±12	---	V
		$R_L = 2\ k\Omega$		4, 5, 6	±10	---	V
Open loop voltage gain (single ended) 5/	Avs(+) Avs(-)	$R_L \ge 2\ k\Omega$ $V_{OUT} = -10$ to 10 V		4	35	---	V/mV
				5, 6	15	---	V/mV
Slew rate	SR(+) and SR(-)	$V_{IN} = \pm 5$ V; $Av = 1$	$T_A = +25°C$	7	8	---	V/µs
			$T_A = -55°C, +125°C$ 1/	8	5	---	V/µs

1/ If not tested shall be guaranteed to the specified limits.

2/ I_{IO} is calculated as the difference between $+I_{IB}$ and $-I_{IB}$.

3/ Bias currents are actually junction leakage currents which double (approximately) for each 10°C increase in junction temperature T_J. Measurement of bias current is specified at T_J rather than T_A, since normal warmup thermal transients will affect the bias currents. The measurements for bias currents must be made within 100 ms after power is first applied to the device for test. Measurement at $T_A = -55°C$ is not necessary since excepted values are too small for typical test systems.

4/ CMRR is calculated from V_{IO} measurements at $V_{CM} = +11$ and -11 V for TL071, 072, 074, and +11.5 V and -11.5 V for TL061, 062, and 063.

5/ Because of thermal feedback effects from output to input, open loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 4
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 7, 8
Groups C and D end-point electrical parameters (method 5005)	1

*PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

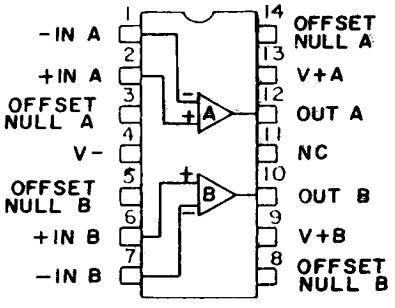
6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/1190XBXX.

Device types 02 and 05

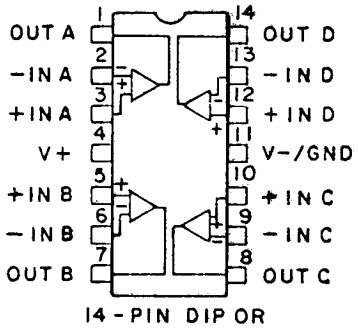
Case C



14 - PIN DIP
(TOP VIEW)

Device types 03 and 06

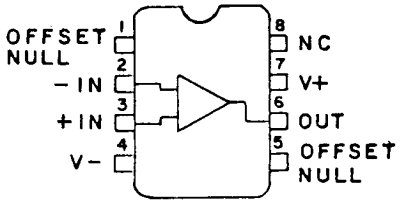
Cases C and D



14 - PIN DIP OR
FLAT PACK
(TOP VIEW)

Device types 01 and 04

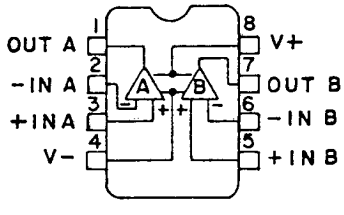
Case P



8-PIN MINI DIP
(TOP VIEW)

Device types 02 and 05

Case P



8-PIN MINI DIP
(TOP VIEW)

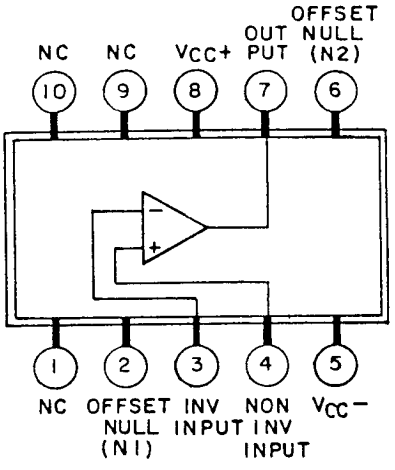
FIGURE 1. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		81023
		REVISION LEVEL E	SHEET 14

☆ U.S. GOVERNMENT PRINTING OFFICE: 1987--549-096

Device types 01 and 04

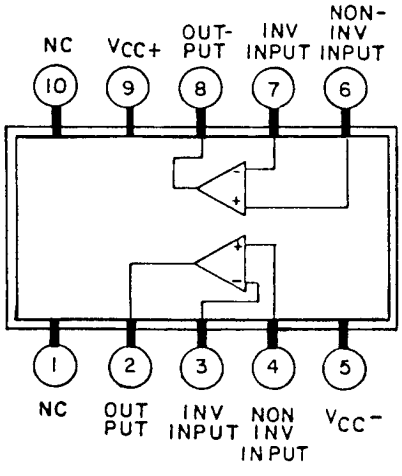
Case H



10-PIN FLAT PACK
(TOP VIEW)

Device types 02 and 05

Case H

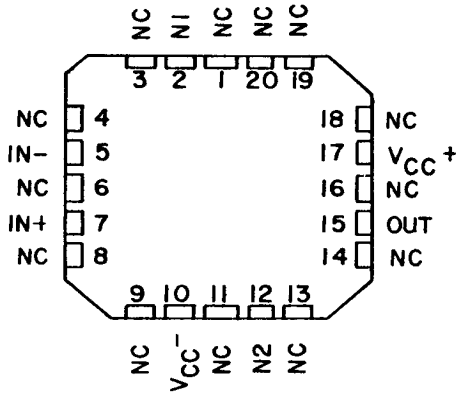


10-PIN FLAT PACK
(TOP VIEW)

FIGURE 1. Terminal connections - Continued.

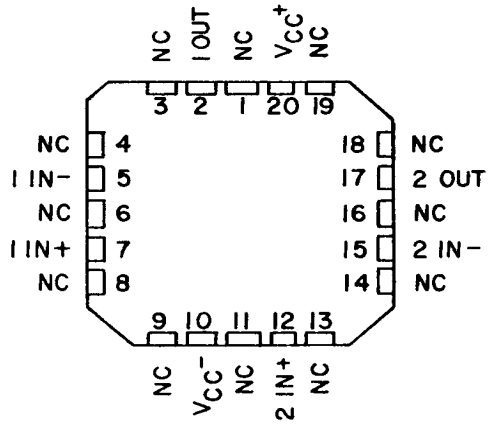
Device types 01 and 04

Case 2



Device types 02 and 05

Case 2



Device types 03 and 06

Case 2

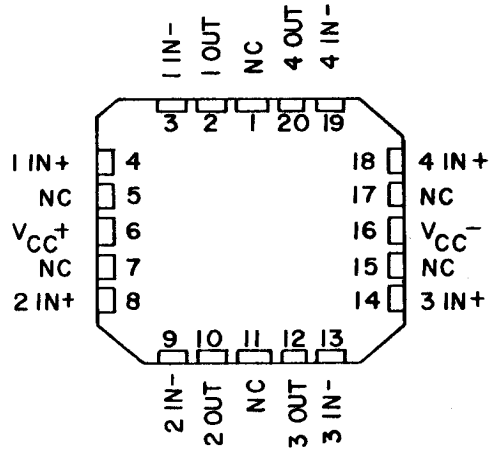


FIGURE 1. Terminal connections - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		81023
		REVISION LEVEL E	SHEET 16

☆ U.S. GOVERNMENT PRINTING OFFICE: 1987—549-096

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
8102301HX	01295	TL061MUB	---
8102301PX	01295	TL061MJGB	M38510/11901BPX
81023012X	01295	TL061MFKB	---
8102302CX 2/	01295	TL062MJB	---
8102302HX	01295	TL062MUB	---
8102302PX	01295	TL062MJGB	M38510/11902BPX
81023022X	01295	TL062MFKB	---
8102303CX	01295	TL064MJB	M38510/11903BCX
8102303DX	01295	TL064MWB	M38510/11903BDX
81023032X	01295	TL064MFKB	---
8102304HX	01295	TL071MUB	---
8102304PX 3/	01295	TL071MJGB	M38510/11904BPX
81023042X	01295	TL071MFKB	---
8102305CX 2/	01295	TL072MJB	---
8102305HX	01295	TL072MUB	---
8102305PX 3/	01295	TL072MJGB	M38510/11905BPX
81023052X	01295	TL072MFKB	---
8102306CX 3/	01295	TL074MJB	M38510/11906BCX
8102306CX 3/	27014	LF147D/883	M38510/11906BCX
8102306DX	01295	TL074MWB	M38510/11906BDX
81023062X	01295	TL074MFKB	---

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Not available from an approved source.

3/ Inactive for new design, use applicable M38510 device.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. P. O. Box 6448 Midland, TX 79701
27014	National Semiconductor P.O. Box 58090 Santa Clara, CA 95052-8090