P4C422
ULTRA HIGH SPEED 256 x 4 CMOS STATIC RAM

T-46-23-08

FEATURES

- **Fast Access Time**
  - **—8, 10, 12, 15, 25 ns (Commercial)**
  - **—15, 20, 25 ns (Military)**
- **PACE Technology™ for High Performance/Low Power**
- **CMOS for Low Power**
  - **—495 mW Maximum (-8, -10, -12, -15 Commercial)**
  - **—330 mW Maximum (-25 Commercial)**
  - **—495 mW Maximum (Military)**
- **Standard 400 mil DIP, 300 mil 24-pin SOIC, and Chip Carrier Packages**
- **5 V Power Supply ±10% for both commercial and military temperature ranges**
- **Separate I/O**
- **Fully static operation with equal access and cycle time**
- **Resistant to single event upset and latchup due to advanced process and design improvements**
- **Capable of withstanding greater than 2000V static discharge**

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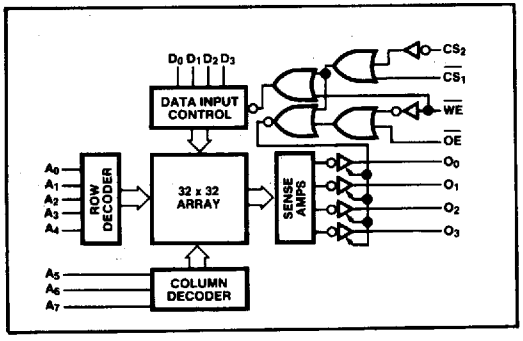
DESCRIPTION

The P4C422 is a 1,024-bit ultra high speed (8ns) Static RAM with a 256 x 4 organization. The memory requires no clocks or refreshing and has equal access and cycle times. Inputs and outputs are fully TTL compatible. Operation is from a single 5 Volt supply. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS}_1$) and active HIGH chip select two (CS_2) as well as 3-state outputs.

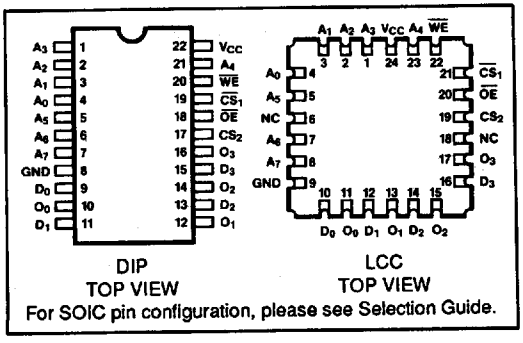
The P4C422 is part of The PACE RAM™ family of static RAM products offering super fast access times never before available, at this complexity level, in TTL compatible bipolar or CMOS technologies. These high performance static RAMs are manufactured using PACE Technology™. PACE Technology is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths to give 500 picoseconds loaded* internal gate delays. PACE Technology™ includes two level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a class 1 environment volume production facility.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V. For a fan-in/fan-out of 1, the internal gate delay is 200 picoseconds at room temperature and 5.0V.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP TOP VIEW

LCC TOP VIEW

For SOIC pin configuration, please see Selection Guide.

PERFORMANCE SEMICONDUCTOR CORPORATION

Means Quality, Service and Speed

MAXIMUM RATINGS[1,2]

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(Above which the useful life may be impaired.)

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 22 to Pin 8)	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5 to V_{CC} + 0.5V

DC Input Voltage	−0.5 to V_{CC} + 0.5V
Output Current, Into Outputs (Low)	20mA
Static Discharge Voltage (per MIL-STD-883 Method 3015.2)	>2000V
Latchup Current	>200mA

Note: Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
Commercial	5V ±10%	0°C to +70°C

Range[5]	V_{CC}	Ambient Temperature
Military	5V ±10%	−55°C to +125°C

DC ELECTRICAL CHARACTERISTICS

(Over the Operating Range[5])

Parameters	Description	Test Conditions			P4C422 Min.	P4C422 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −5.2 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage				2.1		V
V_{IL}	Input LOW Voltage					0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}			−10	10	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −10 mA				−1.5	V
I_{OZ}	Output Current (HIGH-Z)	V_{OL} ≤ V_{OUT} ≤ V_{OH} Output Disabled			−10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max. V_{OUT} = GND	Commercial	-8,-10,-12,-15		90	mA
				-25		70	mA
			Military	-15,-20,-25		90	mA
I_{CC}	Power Supply Current	V_{CC} = Max. Outputs Open	Commercial	-8,-10,-12,-15		90	mA
				-25,		60	mA
			Military	-15,-20,-25		90	mA

CAPACITANCE[4]

Parameters	Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V	7	

Notes:

1) These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields, however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.
2) Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3) For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4) Tested on a sample basis.
5) Extended temperature operation guaranteed with 400 linear feet per minute of air flow.

FUNCTIONAL DESCRIPTION

An active LOW write enable ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS_1}$) and the write enable ($\overline{WE}$) are LOW and the chip select two (CS_2) is HIGH, the information on data inputs (D_0 through D_3) is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch." Reading is performed with chip select one ($\overline{CS_1}$) LOW, chip select two (CS_2) HIGH, write enable ($\overline{WE}$) HIGH and output enable ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the non-inverting outputs (O_0 through O_3). The outputs of the memory go to an inactive high impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

MODE SELECT TABLE

Input					Output	Mode
CS_2	$\overline{CS_1}$	$\overline{WE}$	$\overline{OE}$	D_n	O_n	
L	X	X	X	X	*HIGH Z	Not Selected
X	H	X	X	X	*HIGH Z	Not Selected
H	L	X	H	X	*HIGH Z	Output Disable
H	L	H	L	X	Selected Data	Read Data

Input					Output	Mode
CS_2	$\overline{CS_1}$	$\overline{WE}$	$\overline{OE}$	D_n	O_n	
H	L	L	X	L	*HIGH Z	Write "0"
H	L	L	X	H	*HIGH Z	Write "1"

Notes: H = HIGH L = LOW X = Don't Care
* HIGH Z implies outputs are disabled or off. This condition is defined as high impedance state for the P4C422.

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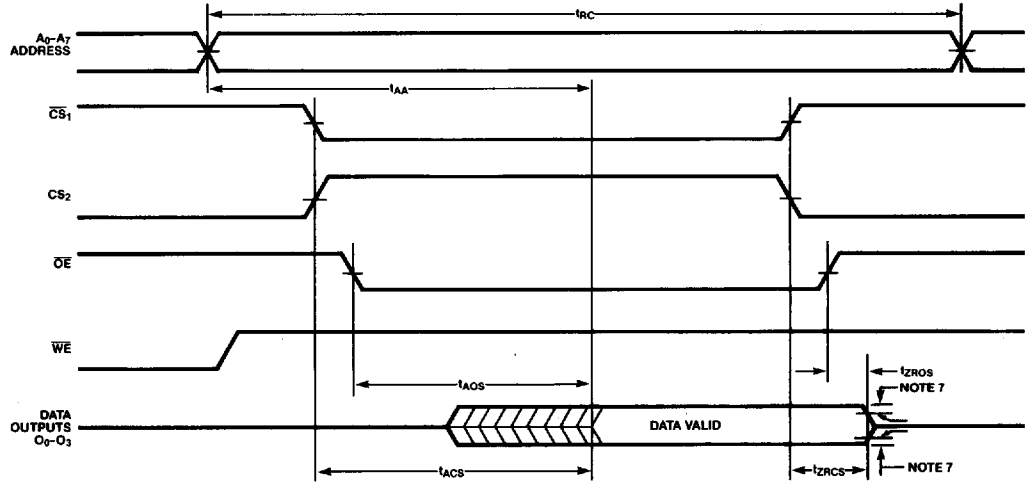
SWITCHING CHARACTERISTICS—READ CYCLE

(Over the Operating Range)[5]

Symbol	Parameter	-8*		-10*		-12		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time[6]	8		10		12		15		20		25		ns
t_{ACS}	Chip Select Time[6]		7		7.5		8		8		12		15	ns
t_{ZRCS}	Chip Select to High-Z[7]		7		8		10		12		15		20	ns
t_{AOS}	Output Enable Time		7		7.5		8		8		12		15	ns
t_{ZROS}	Output Enable to High-Z[7]		7		8		10		12		15		20	ns
t_{AA}	Address Access Time[6]		8		10		12		15		20		25	ns

* V_{CC} = 5V ± 5% for -8, -10.

READ CYCLE WAVEFORMS



SWITCHING CHARACTERISTICS—WRITE CYCLE

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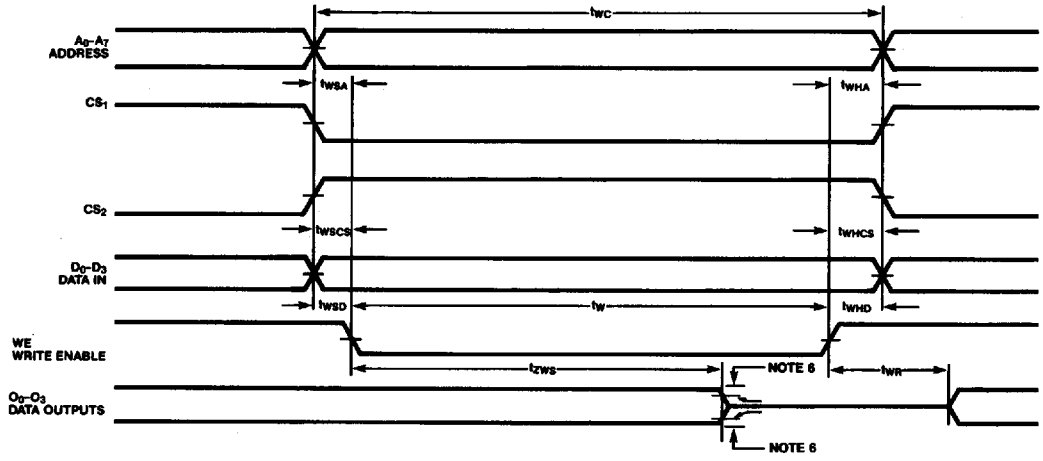
(Over the Operating Range)[5]

Symbol	Parameter	-8*		-10*		-12		-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time[6]	8		10		12		15		20		25		ns
t_{ZWS}	Write Enable to High-Z[7]		7		8		10		12		15		20	ns
t_{WR}	Write Recovery Time		7		8		10		12		15		20	ns
t_W	Write Pulse Width[6,8]	7		8		9		11		13		15		ns
t_{WSD}	Data Setup Time Prior to Write[6]	0		0		0		0		2		5		ns
t_{WHD}	Data Hold Time After Write[6]	1		2		2		2		5		5		ns
t_{WSA}	Address Setup Time[6,8]	0		0		0		0		2		5		ns
t_{WHA}	Address Hold Time[6]	1		2		2		4		5		5		ns
t_{WSCS}	Chip Select Setup Time[6]	0		0		0		0		2		5		ns
t_{WHCS}	Chip Select Hold Time[6]	1		2		2		2		5		5		ns

* V_{CC} = 5V ±5% for -8, -10

WRITE CYCLE WAVEFORMS



Notes:

6) Test conditions assume signal transition times of 3ns or less for the -8, -10, -12, and -15 products and 5ns or less for the -20, -25 and -35 products, see Figure 1d. Timing is referenced at input and output levels of 1.5V. The output loading is equivalent to the specified I_{OL}/I_{OH} with a load capacitance of 15 pF (-8, -10, -12) or 30 pF (-15, -20, -25, -35) as in Figures 1a and 1b respectively.

7) Test conditions assume signal transition times of 3ns or less for the -8, -10, -12, and -15 products and 5ns or less for the -20, -25 and -35 products, see Figure 1d. Transition is measured at steady state HIGH level -500mV or steady state LOW level +500mV on the output from a 1.5V level on the input with load shown in Figure 1c.

8) t_W measured at t_{WSA} = min.; t_{WSA} measured at t_W = min.

AC TEST LOADS & WAVEFORMS

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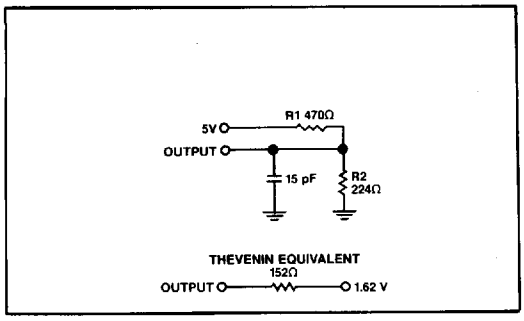

Figure 1a

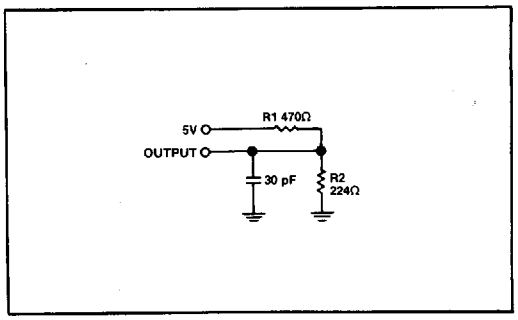

Figure 1b

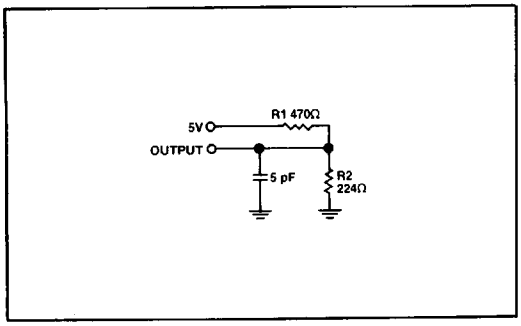

Figure 1c

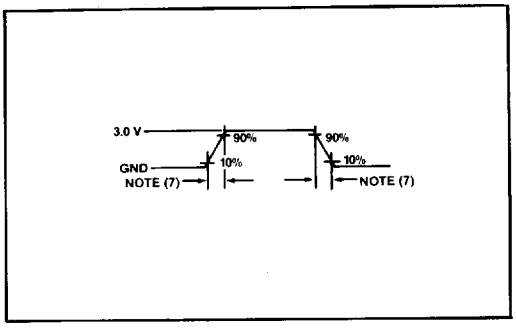

Figure 1d

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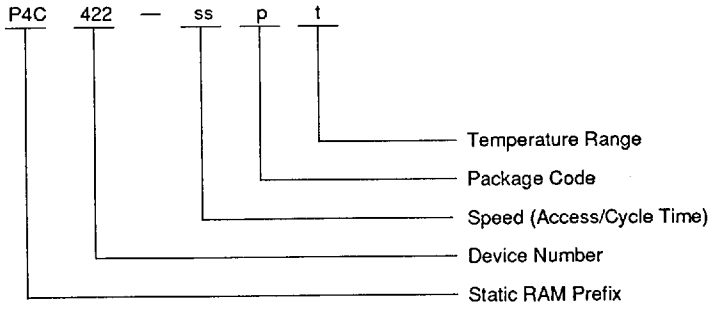
ORDERING INFORMATION



ss = Speed (access/cycle time in ns), e.g., 10, 15
p = Package code, i.e., P, D, S, L
t = Temperature range, i.e., C, M, MB.

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SELECTION GUIDE

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The P4C422 is available in the following temperature range, speed and package options.

Temperature Range	Package \ Speed (ns)	8	10	12	15	20	25
Commercial	Plastic DIP	-8PC	-10PC	-12PC	-15PC	N/A	-25PC
	CERDIP	N/A	-10DC	-12DC	-15DC	N/A	-25DC
	LCC	N/A	-10LC	-12LC	-15LC	N/A	-25LC
Military Temp.	CERDIP	N/A	N/A	N/A	-15DM	-20DM	-25DM
	LCC	N/A	N/A	N/A	-15LM	-20LM	-25LM
Military Processed*	CERDIP	N/A	N/A	N/A	-15DMB	-20DMB	-25DMB
	LCC	N/A	N/A	N/A	-15LMB	-20LMB	-25LMB

* Military temperature range with MIL-STD-883 Revision D, Class B processing.
N/A = Not available

To order these parts, refer to the section on Ordering Information.