REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D	Change to Military drawing format. Add new vendor CAGE 61394. Add 2 new device types. Editorial changes throughout. Change drawing CAGE to 67268.	31 Aug. 1987	M. A. Frye

CURRENT CAGE CODE 67268

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PAGE	24																								
REV STATUS OF PAGES	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
26 May 1982

AMSC N/A

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SIZE: A

CODE IDENT. NO.: 14933

REV: D

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, 65,536 (8KX8), UV ERASABLE PROM, MONOLITHIC SILICON

DWG NO. 82005

PAGE 1 OF 24

5962-E391

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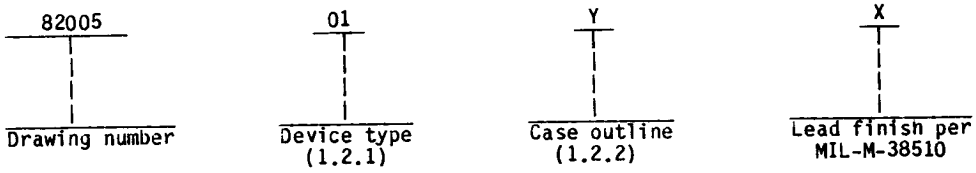
DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access	Program method
01	2764-450	8192 x 8 - Bit UV EPROM	450 ns	A,C
02	2764-250	8192 x 8 - Bit UV EPROM	250 ns	A,C
03	2764A-35	8192 x 8 - Bit UV EPROM	350 ns	B
04	2764A-25	8192 x 8 - Bit UV EPROM	250 ns	B
05	2764A-20	8192 x 8 - Bit UV EPROM	200 ns	B
06	2764-150	8192 x 8 - Bit UV EPROM	150 ns	C
07	2764-200	8192 x 8 - Bit UV EPROM	200 ns	C

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Y	D-10 (28-pin, 1/2" x 1-3/8"), dual-in-line package 1/
Z	C-12 (32-terminal, .450" x .550"), chip carrier package 1/

1.3 Absolute maximum ratings.

Supply voltage, V_{CC}	-0.3 to 7.0 V 2/
Storage temperature range	-65°C to +150°C
Maximum power dissipation, P_D	1.0 W
Lead temperature (soldering, 10 seconds)	300°C.
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	
Device types 03 - 05	+150°C
Device types 01, 02, 06, 07	+175°C
All input or output voltages with respect to ground for device types 03 - 05	-0.6 V to 6.25 V
Input voltage range for device types 01, 02, 06, 07	-0.3 V dc to 7.0 V dc
V_{PP} Supply Voltage (methods A and C)	-0.3 V to 22 V
(method B)	-0.6 V to 13 V

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ All voltages referenced to V_{SS}.

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Input low voltage, V_{IL}	-0.1 V to 0.8 V
Input high voltage, V_{IH}	2.0 to V_{CC} +1
Supply voltage, V_{CC}	4.5 V to 5.5 V
High level program input voltage $V_{IN(PR)}$	21.0 V ±.5 V (Program methods A and C)
High level program input voltage $V_{IN(PR)}$	12.5 V ±0.3 V (Program method B)

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \ge 125°C$		Group A subgroups	Device type	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	I_{OH} = -400 µA	V_{CC} = 4.5 V	1, 2, 3	01,02 06,07	2.4		V
			V_{CC} = 5.25 V		03-05	2.4		
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA	V_{CC} = 5.5 V	1, 2, 3	01,02 06,07		0.4	V
			V_{CC} = 5.25 V		03-05		0.45	
High level output leakage current 2/	I_{OH}	V_{CC} = 5.5 V V_{OUT} = 5.5 V	1/	1, 2, 3	All		10	µA
High level input current 2/	I_{IH}	V_{CC} = 5.25 V V_{IN} = 5.25 V	Outputs deselected	1, 2, 3	All		10	µA
Low level input current 2/	I_{IL}	V_{CC} = 5.25 V V_{IN} = 0.4 V	Output deselected	1, 2, 3	All		-10	µA
V_{PP} supply current read	I_{PP}	V_{PP} = 5.5 V		1, 2, 3	All		5	mA
Supply current (standby)	I_{SB}	Output open $\overline{CE}$ = V_{IH}	V_{CC} = 5.5 V	1, 2, 3	01,02 06,07		60	mA
			V_{CC} = 5.25 V		03-05		40	
Supply current	I_{CC}	Outputs open $\overline{OE}$ = $\overline{CE}$ = V_{IL}	V_{CC} = 5.5 V	1, 2, 3	01,02 06,07		120	mA
			V_{CC} = 5.25 V		03-05		100	
Low level output leakage current	I_{OL}	V_{CC} = 5.5 V V_{OUT} = 0.1 V	1/	1, 2, 3	All		10	µA
High level input leakage current	I_{IH}	V_{CC} = 5.5 V V_{IN} = 5.5 V		1, 2, 3	01,02 06,07		1	µA
					03,04, 05		10	
Low level input leakage current	I_{IL}	V_{CC} = 5.5 V V_{IN} = 0.1 V		1, 2, 3	01,02 06,07		1	µA
					03,04, 05		-10	
High level input voltage	V_{IH}	V_{CC} = 4.5 V	3/	1, 2, 3	All	2.0	6.5	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \ge 125°C$	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Low level input voltage	V_{IL}	V_{CC} = 5.5 V 3/	1, 2, 3	All	-0.1	0.8	V
V_{PP} read voltage	V_{PP}		1, 2, 3	All	V_{CC} -0.7	V_{CC} +1	V
Input capacitance 2/ 4/	C_{IN}	V_{IN} = 0 V, f = 1 MHz T_C = 25°C	4	All		6	pF
Output capacitance 4/	C_O	V_{OUT} = 0 V, f = 1 MHz T_C = 25°C	4	All		12	pF
Address access time	t_{AA}	V_{CC} = 5.25 V 2/ 5/ See figure 5	9, 10, 11	06		150	ns
				05,07		200	
				01		450	
				02,04		250	
				03		350	
Chip enable access time	t_{CE}		9, 10, 11	06		150	ns
				05,07		200	
				01		450	
				02,04		250	
				03		350	
Output enable access time	t_{OE}		9, 10, 11	03	15	130	ns
				01	15	200	
				02,04, 06	10	100	
				05,07	0	150	
$\overline{CE}$ or $\overline{OE}$ to high Z	t_{DF} 6/		9, 10, 11	03	0	115	ns
				01	5	150	
				02	0	90	
				04	0	60	
				05,07	0	150	
				06	0	80	
Output hold from address change	t_{OH} 6/		9, 10, 11	All	0		ns

1/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{OL} and I_{OH} with the output under test connected to V_{OUT}.
2/ Outputs shall be loaded per figure 4.
3/ Tests for all inputs and control pins.
4/ All pins not being tested are to be grounded.
5/ Equivalent ac test conditions (actual load conditions vary by tester):
Output load: 1 TTL gate and C_L = 100 pF.
Input rise and fall times $\le$ 20 ns.
Input pulse levels: 0.4 V and 2.4 V.
6/ Tested initially and after any design changes.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.5.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.5.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 and 4.6.

3.5.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A

1. Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2).
2. Bake, unbiased, for 12 hours at 200°C.
3. Perform a margin test using $V_M = V_{CC} = 6.0$ V at +25°C using loose timing.
4. Erase device, then program 45 percent-50 percent of the bits to a worst case speed pattern.
5. Perform dynamic burn-in (see 4.2a).
6. Perform a margin test using $V_M = V_{CC} = 6.0$ V at +25°C.
7. Perform 100 percent electrical testing at +125°C and -55°C. Perform 100 percent ac and dc electricals at +25°C.
8. Erase device (see 3.5.1), except devices submitted for groups A, B, C, and D.
9. Verify erasure (see 3.5.3).

Margin test method B

1. Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2). The remaining cells shall provide a worst case speed pattern.
2. Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.
3. Perform a margin test using $V_M = +5.9$ V at +25°C using loose timing (i.e., $t_{ACC} = 1$ µs).
4. Perform dynamic burn-in (see 4.2a).
5. Margin at $V_M = +5.9$ V.
6. Perform electrical tests (see 4.2).
7. Erase (see 3.5.1), except devices submitted for groups A, B, C, and D testing.
8. Verify erasure (see 3.5.3).

Margin test method C

1. Program at 25°C with a greater than 95 percent pattern (ex. diagonal "1's") (see 3.5.2).
2. Unbiased bake for 8 hours at 200°C or 24 hours at 170°C or 72 hours at 150°C.
3. Test at 95°C (see 3.5.3), including a margin test at $V_M = +6$ V and loose timing (i.e. $T_{ACC} = 1$ µs).
4. Erase (see 3.5.1).
5. Program at 25°C with a 50 percent pattern (ex. checkboard bar) (see 3.5.2) (Programmed with checkboard at wafer sort).

6. Test at 125°C (see 3.5.3).

7. Burn-in (see 4.2a).

8. Test at 125°C (see 3.5.3).

9. Test at -55°C (see 3.5.3).

10. Erase (see 3.5.1). Devices may be submitted for groups A, B, C, and D testing at this point.

11. Verify erasure at 25°C (see 3.5.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_O measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

4.4 Erasing procedure. The device is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 253.7 mm. The recommended integrated dose (i.e., UV intensity X exposure time) is 15 W-s/cm^2. An example of an ultraviolet source which can erase the device in 30 minutes is the Model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the EPROM should be placed about 1 inch away from the lamp tubes. After erasure, all bits are in the high state.

4.5 Programming procedures for methods A and C. The programming characteristics in tables IIIa and IIIc and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming. The waveforms of figure 6 and programming characteristics of tables IIIa and IIIc shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.4).

c. Programming occurs when Vpp is 21.0 ±0.5 V and chip enable and $\overline{PGM}$ are brought low.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 8, 9 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 9 or 2, 8(hot), 10
Additional electrical subgroups for group C periodic inspections	---

NOTES:
1. (*) Indicates PDA applies to subgroup 1 (see 4.2).
2. Any or all subgroups may be combined when using a high speed tester.
3. Subgroup 8 shall consist of verifying the pattern specified.
4. For all electrical tests, the device shall be programmed to the pattern specified.

4.6 Programming procedures for method B. The programming characteristics in table IIIb and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration for programming. The waveforms of figure 6 and programming characteristics of table IIIb shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.4).

c. Programming occurs when V_{pp} is 12.5 ±0.3 V and chip enable and $\overline{PGM}$ are brought low.

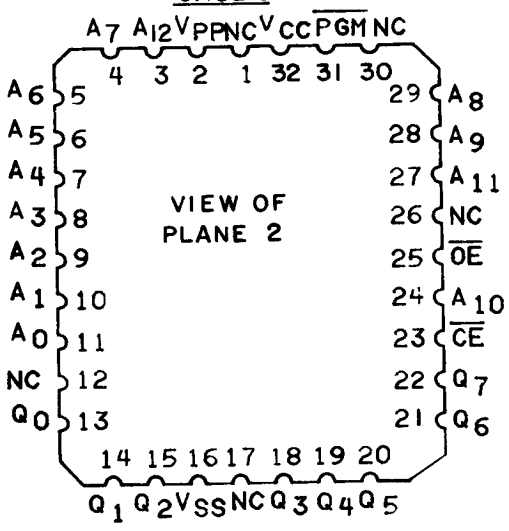
5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

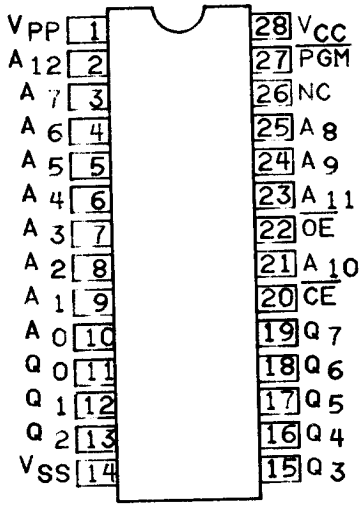
6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

CASE Z



CASE Y



OPTION A WITH ACTIVE TERMINALS ON PLANE 1.

Pin Names

A_0 - A_{12}	Addresses
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
Q_{0-7}	Outputs
$\overline{PGM}$	Program pin

FIGURE 1. Terminal connections.

Device types 01, 02, 06 and 07

Mode / Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
Silicon signature * (Intelligent identifier)	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Encoded data

X can be either V_{IL} or V_{IH}.
* For silicon signature (tm) (intelligent identifier) A0 is toggled. A9 = 12 ±0.5 V., and all other addresses are at a TTL low (V_{IL}).

Device types 03, 04, and 05

Mode/pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs	V_{PP}
Programming method	A, B	A, B	A, B	A	A, B	B
Deselect	V_{IL}	V_{IH}	V_{IH}	V_{CC}	High Z	V_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}	V_{CC}
Standby	V_{IH}	X	X	V_{CC}	High Z	V_{CC}
Program	V_{IL}	V_{IH}	V_{IL}	+21 V	D_{IN}	+12.5 V
Program inhibit	V_{IH}	X	X	+21 V	High Z	+12.5 V
Program verify	V_{IL}	V_{IL}	V_{IH}	+21 V	D_{OUT}	+12.5 V

NOTES:
1. It is recommended that verification for method A & B devices be performed after the completion of programming all bytes.
2. X means input is a "don't care".

FIGURE 2. Truth table.

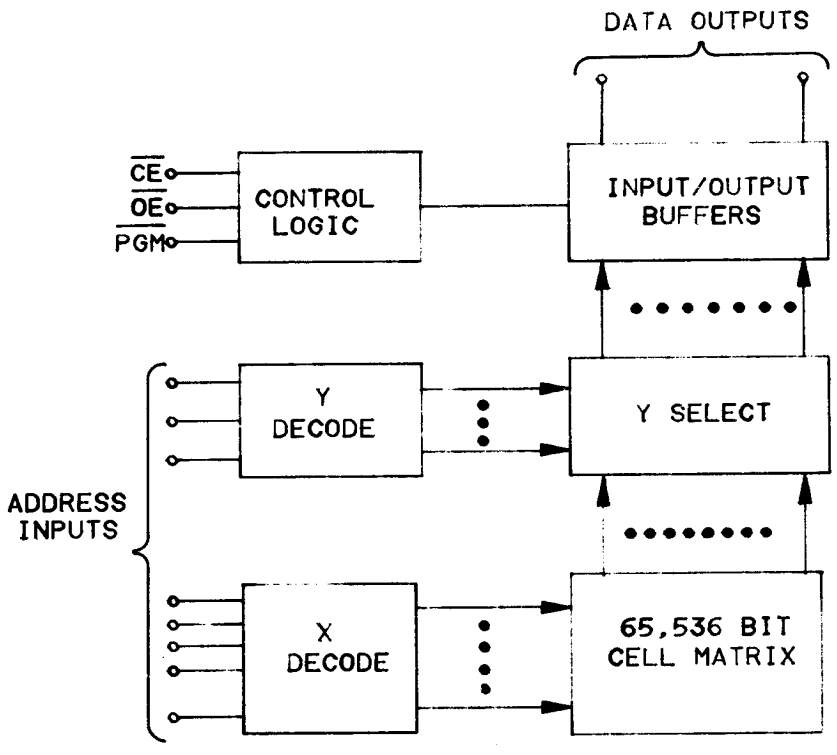


FIGURE 3. Logic diagram.

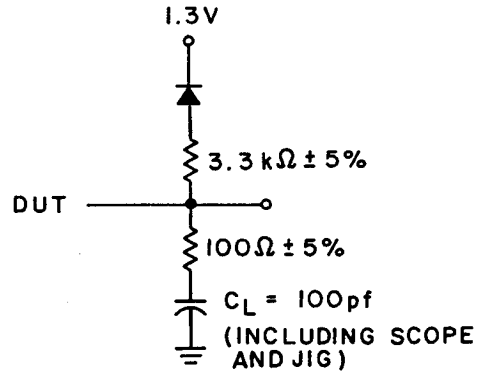
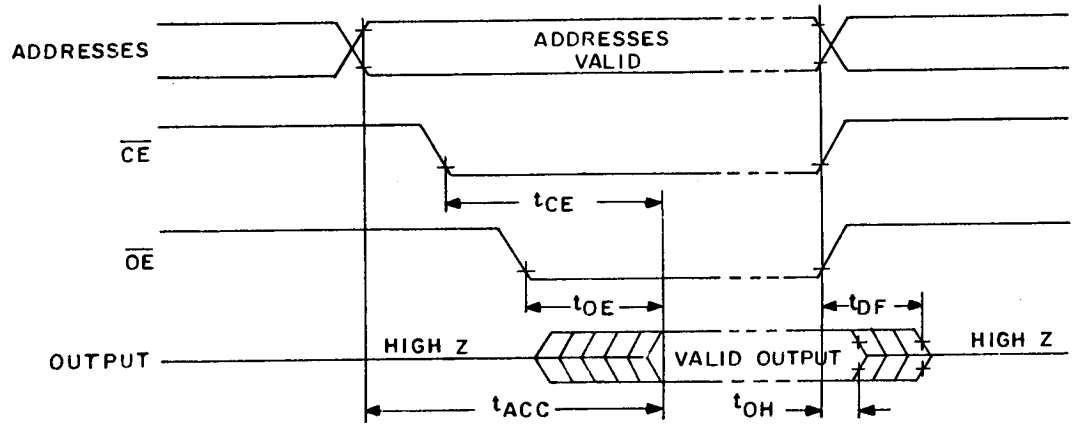


FIGURE 4. Output load. (suggested)

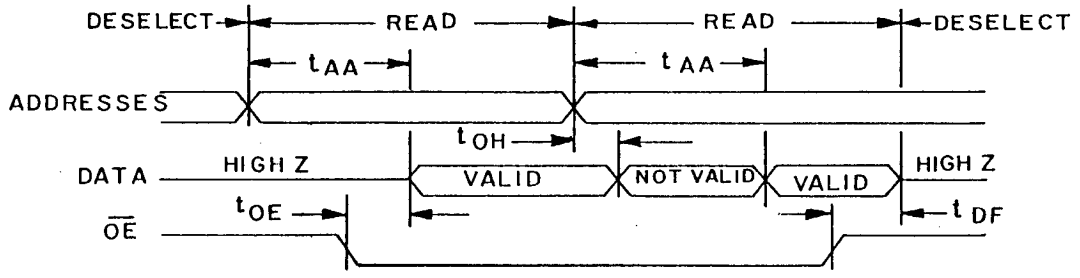
Device types 01, 02, 06, and 07.



NOTES:
1. Tdf is specified from OE or CE, whichever occurs first.
2. OE may be delayed up to Tacc - Toe after the falling edge of CE without impact on Tacc.

FIGURE 5. Read cycle timing diagram.

READ WITH $\overline{CE}$ = V_{IL} USING $\overline{OE}$ CONTROL



READ USING THE $\overline{CE}$ AND $\overline{OE}$ CONTROL

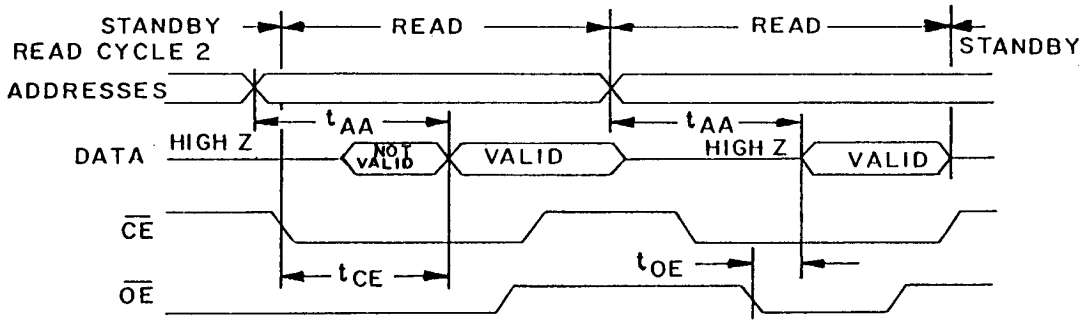


FIGURE 5. Read cycle timing diagram - Continued.

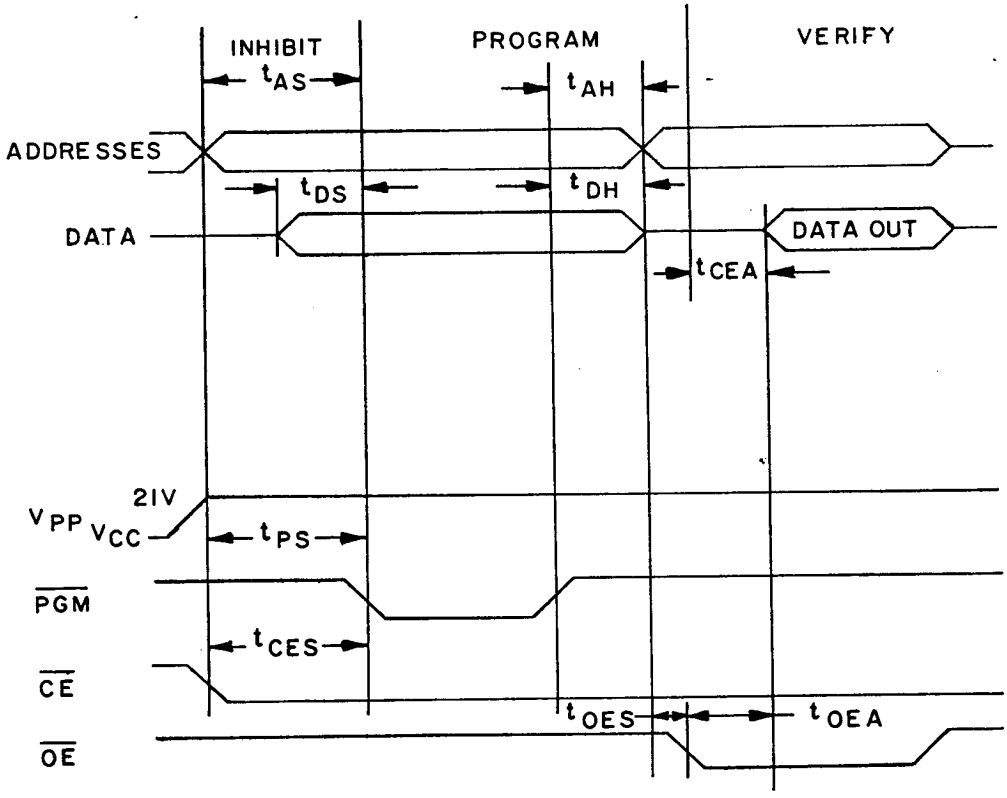


FIGURE 6. Programming timing diagram for method A.

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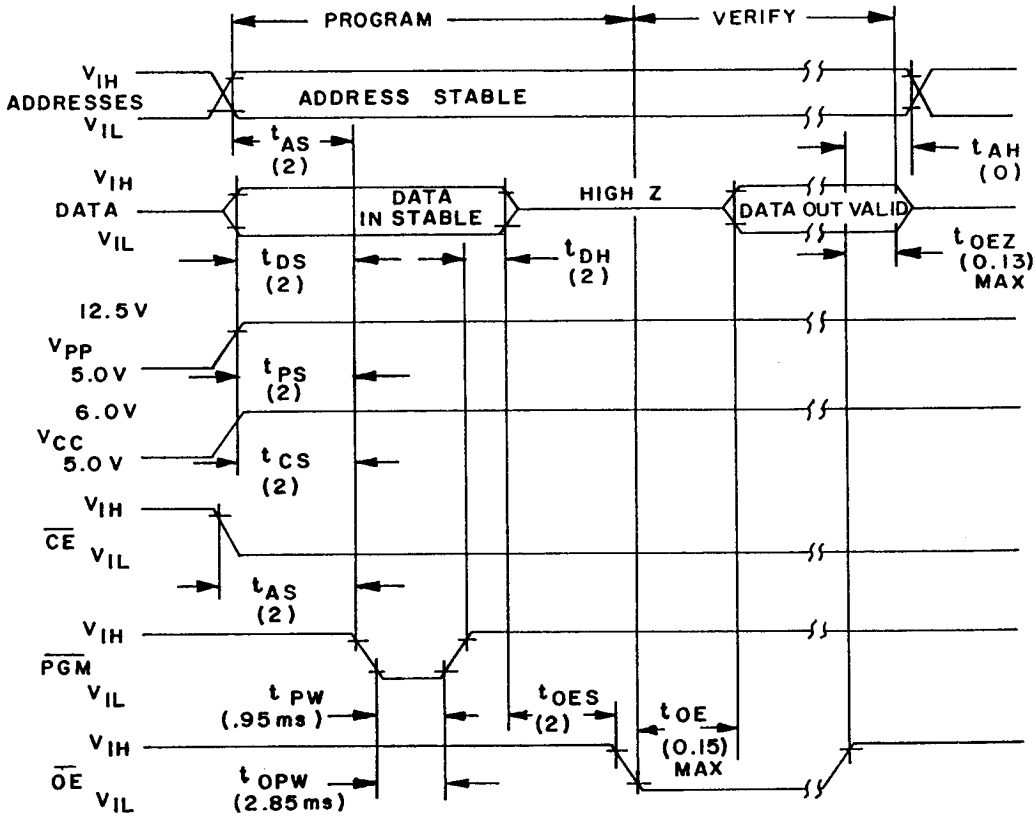
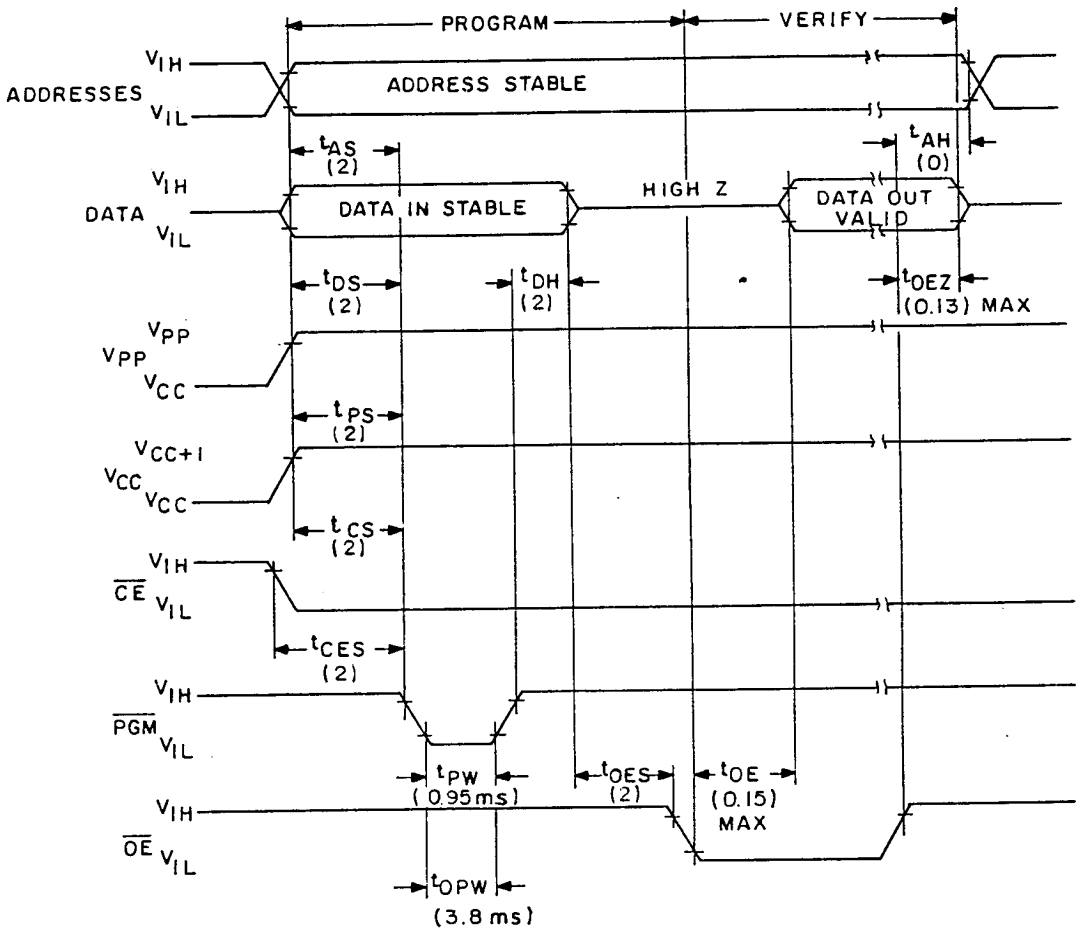


NOTES:

1. All times shown in ( ) are minimum and in µsec unless otherwise specified.
2. The input timing reference level is .8 V for V_{IL} and 2 V for a V_{IH}
3. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
4. When programming, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

FIGURE 6. Programming timing diagram for method B — Continued.



NOTES:
1. All times shown are minimum and in us unless otherwise specified.
2. The input timing reference level is 0.8 V for a V_{IL} and 2 V for a V_{IH}.
3. T_{oe} and T_{ofp} are characterisitics of the device but must be accommodated by the programmer.
4. When programming the device, a 0.1 µF ceramic capacitor is required across V_{pp} and ground to suppress spurious voltage transients which can damage the device.

FIGURE 6. Programming timing diagram for method C - Continued.

TABLE IIIa. Programming characteristics for method A.

Test	Symbol	Conditions 1/	Group A subgroups	Limits		Unit
				Min	Max	
Input low voltage	V_{IL}				0.8	V
Input high voltage	V_{IH}			2.2	$V_{CC}+1$	V
Input leakage current	I_{IL}	Except $\overline{OE}/V_{PP}$ 0.4 V $\leq V_{IN} \leq$ 5.25 V		-10	+10	µA
Programming voltage	V_{PP}			20.5	21.5	V
Programming supply current	I_{PP2}	$\overline{CE} = \overline{PGM} = V_{IL}$			30	mA
V_{CC} power supply current	I_{CC}				150	mA
Address setup time	t_{AS}			2		µs
Data setup time	t_{DS}			2		µs
Address hold time	t_{AH}			0		µs
Data hold time	t_{DH}			2		µs
Program pulse width	t_{PW}			45	55	ms
Vpp setup time	t_{PS}			2		µs
Output enable setup time	t_{OES}			2		µs
Chip enable setup time	t_{CES}			2		µs

1/ t_{CEH} is measured from $\overline{OE}/V_{PP}$.

TABLE IIIb. Programming characteristics for method B.

Test	Symbol	Conditions 1/ V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.3 V	Limits Min	Limits Max	Unit
Input current (all inputs)	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
Input low level (all inputs)	V_{IL}		-0.1	0.8	V
Input high level	V_{IH}		2.0	V_{CC}+1	V
Output low voltage during verify	V_{OL}	I_{OL} = 2.1 mA		0.45	V
Output high voltage during verify	V_{OH}	I_{OH} = -400 µA	2.4		V
V_{CC} supply current (program and verify)	I_{CC}			100	mA
V_{PP} supply current (program)	Ipp	$\overline{CE} = V_{IL}$		50	mA
A_9 intelligent identifier voltage	V_{ID}		11.5	12.5	V
Address setup time	t_{AS}		2		µs
$\overline{OE}$ setup time	t_{OES}		2		µs
Data setup time	t_{DS}		2		µs
Address hold time	t_{AH}		0		µs
Data hold time	t_{DH}		2		µs
Output enable to output float delay	t_{OEZ}	2/	0	130	ns
V_{PP} setup time	t_{PS}		2		µs
V_{CC} setup time	t_{CS}		2		µs

See footnotes at end of table.

TABLE IIIb. Programming characteristics for method B - Continued.

Test	Symbol	Conditions 1/ V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.3 V	Limits		Unit
			Min	Max	
$\overline{PGM}$ initial program pulse width	t_{PW}	3/	0.95	1.05	ms
$\overline{PGM}$ overprogram pulse width	t_{OPW}	4/	2.85	78.75	ms
Data valid from $\overline{OE}$	t_{OE}			150	ns

1/ V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

2/ This parameter is only sampled and is not 100 percent tested. Output float is defined as the point where data is no longer driven--see timing diagram for method B.

3/ Initial program pulse width tolerance is 1 ms ±5 percent.

4/ The length of the overprogram pulse may vary from 2.85 ms to 78.75 ms as a function of the iteration counter value X.

TABLE IIIc. Programming characteristics for method C.

Test	Symbol	Conditions 1/ $5.75\ V \le V_{CC} \le 6.25\ V$, $20.5\ V \le V_{PP} \le 21.5\ V$, $T_A = +25°C \pm 5°C$	Limits Min	Limits Max	Unit
Input current (all inputs)	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
Input low level (all inputs)	V_{IL}			0.8	V
Input high level	V_{IH}		2.0	$V_{CC}+1$	V
Output low voltage during verify	V_{OL}	$I_{OL} = 2.1$ mA		0.45	V
Output high voltage during verify	V_{OH}	$I_{OH} = 400$ µA	2.4		V
V_{CC} supply current (program and verify)	I_{CC}			120	mA
V_{PP} supply current (program)	I_{PP}	$\overline{CE} = V_{IL}$		50	mA
A9 voltage silicon signature (tm)	V_{ID}		11.5	12.5	V
Address setup time	t_{AS}		2		µs
$\overline{OE}$ setup time	t_{OES}		2		µs
Data setup time	t_{DS}		2		µs
Address hold time	t_{AH}		0		µs
Data hold time	t_{DH}		2		µs
Output enable to output float delay	t_{OEZ}	2/	0	130	ns
V_{PP} setup time	t_{PS}		2		µs
V_{CC} setup time	t_{CS}		2		µs

See footnotes at end of table.

TABLE IIIc. Programming characteristics for method C - Continued.

Test	Symbol	Conditions 1/ 5.75 V ≤ V_{CC} ≤ 6.25 V, 20.5 V ≤ V_{PP} ≤ 21.5 V, T_A = +25°C ±5°C	Limits		Unit
			Min	Max	
$\overline{PGM}$ initial program pulse width	t_{PW}		0.95	1.05	ms
$\overline{PGM}$ overprogram pulse width	t_{OPW}		2.85	78.75	ms
Data valid from $\overline{OE}$	t_{OE}			150	ns
CE setup time	t_{CES}		2		µs

1/ V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.

2/ Tested by inference only.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Programming method	Margin test method
8200501YX	61394	DM2764-450	C	C
8200501ZX	2/	AM2764-45/BUA	A	A
8200502YX	61394	DM2764-250	C	C
8200502ZX	2/	AM2764-25/BUA	A	A
8200503YX	34335	AM2764A-35/BXA	B	A
	34649	MD2764A-35/B	B	B
8200503ZX	34335	AM2764A-35/BUA	B	A
	34649	MR2764A-35/B	B	B
8200504YX	34335	AM2764A-25/BXA	B	A
	34649	MD2764A-25/B	B	B
8200504ZX	34335	AM2764A-25/BUA	B	A
	34649	MR2764A-25/B	B	B
8200505YX	34335	AM2764A-20/BXA	B	A
8200505ZX	34335	AM2764A-20/BUA	B	A
8200506YX	61394	DM2764-150	C	C
8200507YX	61394	DM2764-200	C	C

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ Not avaliable from an approved source of supply.

Vendor CAGE number	Vendor name and address	Intelligent identifier manufacturer	Device
34335	Advanced Micro Devices, Incorporated 901 Thompson Place Sunnyvale, CA 94088	01	08
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051	89	08
61394	SEEQ Technology 1849 Fortune Drive San Jose, CA 95131	94	01

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