REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table I: Add V_{OL} parameters. 1.3: Change P_D from 1.5 mW to 1.75 mW.	1984 MAR 2	M.A. Frye
B	Revise table I limits, add 10 MHz device, revise operating temperature range, and revise waveforms.	1985 DEC 16	M.A. Frye
C	Convert to military drawing format, inactivate parts which have a QPL source, change parameters 28, 57, and 58 in table I and the corresponding waveforms on figure 6. Add vendor CAGE number 50088 to drawing. Editorial changes throughout.	1987 APR 23	M.A. Frye
D	Add device type 04. Changes to 1.3 and 1.4. Changes to tables I and II. Delete figures 2 and 3. Change CAGE number to 67268. Delete vendor CAGE number 04713 as approved source for 01 device. Editorial changes throughout document.	1988 APR 1	M.A. Frye
E	Add case outline U. Change case T dimensions on figure 1. Add vendor CAGE 18324 as supplier for device 01. Editorial changes throughout.	1989 NOV 16	M.A. Frye

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV	E	E	E	E	E	E	E	E	E	E	E													
SHEET	22	23	24	25	26	27	28	29	30	31	32													

REV STATUS OF SHEETS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Christopher A Rauch

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APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 28 SEPTEMBER 1983

REVISION LEVEL: E

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MICROPROCESSOR, 16-BIT, N-CHANNEL, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	82021

SHEET 1 OF

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1242

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

82021	01	T	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit
01	68000-6	16-bit fixed instruction microprocessor
02	68000-8	16-bit fixed instruction microprocessor
03	68000-10	16-bit fixed instruction microprocessor
04	68000-12	16-bit fixed instruction microprocessor

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
T	See figure 1 (68-terminal 1.080" x 1.080" x .102") pin grid array
U	See figure 1 (68-terminal 0.960" x 0.960" x .097") leaded chip carrier package)
X	C-7 (68-terminal .962" x .962" x .120") square chip carrier package with thermal pad
Y	D-13 (64-lead, 3.240" x .920" x .225") dual-in-line package
Z	C-7 (68-terminal .962" x .962" x .120") square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.3 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation, (P_D)	1.75 W
Lead temperature (soldering 5 seconds)	270°C
Junction temperature (T_J)	150°C
Thermal resistance, junction to case (θ_{JC}):	
Case T	15°C/W
Case U	20°C/W
Cases X, Y and Z	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage:	
V_{CC}	4.75 V dc to 5.25 V dc
High level input voltage (logic inputs)(V_{IH})	2.0 V to V_{CC}
Low level input voltage (logic inputs)(V_{IL})	GND to 0.8 V dc
Minimum high level output voltage	2.4 V dc
Maximum low level output voltage	0.5 V dc
Frequency of operation:	
Device type 01	4.0 to 6.0 MHz
Device type 02	4.0 to 8.0 MHz

Device type 03	4.0 to 10.0 MHz
Device type 04	4.0 to 12.0 MHz
Case operating temperature range (T_C)	-55°C to +110°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +110°C$ 4.75 V $\le V_{CC} \le$ 5.25 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
High-level output voltage all outputs	V_{OH1}	I_{OH} = -400 µA	1, 2, 3	2.4		V
High-level output voltage enable only	V_{OH2}	I_{OH} = -400 µA, R pullup = 1.1 kΩ		V_{CC} -.75		V
Low-level output voltage A23-1, FC0-2, $\overline{BG}$	V_{OL1}	V_{CC} = 4.75 V, I_{OL} = 3.2 mA	1, 2, 3		0.5	V
Low-level output voltage $\overline{HALT}$	V_{OL2}	I_{OL} = 1.6 mA				
Low-level output voltage $\overline{AS}$, R/$\overline{W}$, D15-0, $\overline{VDS}$, $\overline{LDS}$, $\overline{VMA}$, E	V_{OL3}	I_{OL} = 5.3 mA				
Low-level output voltage $\overline{RESET}$	V_{OL4}	I_{OL} = 5.0 mA				
High-impedance (off-state) output current (HIGH)	I_{OHZ}	V_O = 2.4 V	1, 2, 3		20	µA
High-impedance (off-state) output current (LOW)	I_{OLZ}	V_O = 0.4 V	1, 2, 3	-20		µA
High-level input current; all inputs 2/	I_{IH1}	V_{IN} = 5.25 V	1, 2, 3		2.5	µA
High-level input current $\overline{HALT}$, $\overline{RESET}$	I_{IH2}				20	µA
Low-level input current; all inputs 2/	I_{IL1}	V_{IN} = 0 V	1, 2, 3	-2.5		µA
Low-level input current $\overline{HALT}$, $\overline{RESET}$	I_{IL2}			-20		
Supply current	I_{CC}	V_{CC} = 5.25 V 3/	1, 2, 3		333	mA
Capacitance	C_{IN}	V_{IN} = 0 V, frequency = 1 MHz (see 4.3.1c)	4		20	pF
Functional tests		See 4.3.1d	7, 8			

See footnotes at end of table.

★ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +110°C$ 4.75 V $\le V_{CC} \le$ 5.25 V unless otherwise specified	Waveform number (see figure 3)	Group A subgroups	Device type 01 6 MHz		Device type 02 8 MHz		Device type 03 10 MHz		Device type 04 12.0 MHz		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
Clock period	t_{cyc}	GND = 0 V C_L = 130 pF	1	9, 10, 11	167	250	125	250	100	250	80	250	ns
Clock width low	t_{CL}	See figure 3	2	9, 10, 11	75	125	55	125	45	125	35	125	ns
Clock width high	t_{CH}		3	9, 10, 11	75	125	55	125	45	125	35	125	ns
Clock fall time	t_{Cf}		4	9, 10, 11		10		10		10		5	ns
Clock rise time	t_{Cr}		5	9, 10, 11		10		10		10		5	ns
Clock low to address	t_{CLAV}		6	9, 10, 11		80		70		60		55	ns
Clock high to FC valid	t_{CHFCV}		6A	9, 10, 11		80		70		60		55	ns
Clock high to address data high impedance (maximum)	t_{CHADZ}		7 4/	9, 10, 11		100		80		70		60	ns
Clock high to address/FC invalid (minimum)	t_{CHAFI}		8 5/	9, 10, 11	0		0		0		0		ns
Clock high to $\overline{AS}$, $\overline{DS}$ low (maximum)	t_{CHSL}		9 6/	9, 10, 11	7/ 0	70	7/ 0	60	7/ 0	55	7/ 0	55	ns
Clock high to $\overline{AS}$, $\overline{DS}$ high (minimum)	t_{CHSLn}		8/	9, 10, 11									ns
Address to $\overline{AS}$, $\overline{DS}$ (read) low/$\overline{AS}$ write	t_{AVSL}		11 9/	9, 10, 11	35		30		20		0		ns
FC valid to $\overline{AS}$, $\overline{DS}$ (Read) low/$\overline{AS}$ write	t_{FCVSL}		11A 9/ 10/	9, 10, 11	70		60		50		40		ns
Clock low to $\overline{AS}$, $\overline{DS}$ high	t_{CLSH}		12 6/	9, 10, 11		80		70		55		50	ns
$\overline{AS}$, $\overline{DS}$ high to address/FC invalid	t_{SHAFI}		13 9/ 10/	9, 10, 11	40		30		20		10		ns

See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C<T_C<+110°C$ 4.75 V $\leq V_{CC} \leq$ 5.25 V unless otherwise specified	Waveform number (see figure 3)	Group A subgroups	Device type 01 6 MHz		Device type 02 8 MHz		Device type 03 10 MHz		Device type 04 12.0 MHz		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
$\overline{AS}$, $\overline{DS}$ width low (read)/$\overline{AS}$ write	t_{SL}	GND = 0 V C_L = 130 pF See figure 3	14 9/ 10/	9, 10, 11	337		240		195		160		ns
$\overline{DS}$ width low (write)	t_{DSL}		14A 9/ 10/	9, 10, 11	170		115		95		80		ns
$\overline{AS}$, $\overline{DS}$ width high	t_{SH}		15 9/ 10/	9, 10, 11	180		150		105		65		ns
clock high to $\overline{AS}$, $\overline{DS}$ high impedance	t_{CHCZ}		16 4/	9, 10, 11		100		80		70		60	ns
$\overline{AS}$, $\overline{DS}$ high to R/$\overline{W}$ high	t_{SHRH}		17 9/ 10/	9, 10, 11	50		40		20		10		ns
Clock high to R/$\overline{W}$ high (maximum)	t_{CHRH}		18 6/	9, 10, 11		80		70		60		60	ns
Clock high to R/$\overline{W}$ high (minimum)	t_{CHRHn}		8/	9, 10, 11									
Clock high to R/$\overline{W}$ low	t_{CHRL}		20 6/	9, 10, 11		80		70		60		60	ns
$\overline{AS}$ low to R/$\overline{W}$ valid	t_{ASRV}		20A 10/ 11/	9, 10, 11		20		20		20		20	ns
Address valid to R/$\overline{W}$ low (write)	t_{AVRL}		21 9/ 10/	9, 10, 11	25		20		0		0		ns
FC valid to R/$\overline{W}$ low (write)	t_{FCVRL}		21A 9/ 10/	9, 10, 11	70		60		50		30		ns
R/$\overline{W}$ low to $\overline{DS}$ low (write)	t_{RLSL}		22 9/ 10/	9, 10, 11	140		80		50		30		ns
Clock low to data out valid (write)	t_{CLDO}		23	9, 10, 11		80		70		55		55	ns
Clock high to R/$\overline{W}$ $\overline{VMA}$ high impedance	t_{CHRZ}		12/	9, 10, 11									ns

See footnotes at end of table.

★ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C<T_C<+110°C$ $4.75\ V<V_{CC}<5.25\ V$ unless otherwise specified	Waveform number (see figure 3)	Group A subgroups	Device type 01 6 MHz		Device type 02 8 MHz		Device type 03 10 MHz		Device type 04 12.0 MHz		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
$\overline{AS}$, $\overline{DS}$ high to data out invalid (write)	t_{SHDOI}	GND = 0 V C_L = 130 pF See figure 3	25 9/ 10/	9, 10, 11	40		30		20		15		ns
Data out valid to $\overline{DS}$ low (write)	t_{DOSL}		26 9/	9, 10, 11	35		30		20		15		ns
Data in to clock low (setup time) (read)	t_{DICL}		27 10/ 13/	9, 10, 11	25		15		10		10		ns
$\overline{AS}$, $\overline{DS}$ high to $\overline{DTACK}$ high	t_{SHDAH}		28 9/ 10/	9, 10, 11	0	325	0	245	0	190	0	150	ns
$\overline{DS}$ high to data (read) invalid (hold time)	t_{SHDII}		29 10/	9, 10, 11	0		0		0		0		ns
$\overline{AS}$, $\overline{DS}$ high to $\overline{BERR}$ High	t_{SHBEH}		30 10/	9, 10, 11	0		0		0		0		ns
$\overline{DTACK}$ low to data in (setup time)	t_{DALDI}		31 9/ 10/ 13/	9, 10, 11		120		90		65		50	ns
$\overline{HALT}$ and $\overline{RESET}$ input transition time	$t_{RHr,f}$		32 4/	9, 10, 11	0	200	0	200	0	200	0	200	ns
Clock high to $\overline{BG}$ low	t_{CHGL}		33	9, 10, 11		80		70		60		50	ns
Clock high to $\overline{BG}$ high	t_{CHGH}		34 10/	9, 10, 11		80		70		60		50	ns
$\overline{BR}$ low to $\overline{BG}$ low	t_{BRLGL}		35 10/	9, 10, 11	1.5	3.5 +100 ns	1.5	3.5 +90 ns	1.5	3.5 +80 ns	1.5	3.5 +70 ns	Clk. Per.
$\overline{BR}$ high to $\overline{BG}$ high	t_{BRHGH}		36 10/ 14/	9, 10, 11	1.5	3.5 +100 ns	1.5	3.5 +90 ns	1.5	3.5 +80 ns	1.5	3.5 +70 ns	Clk. Per.
$\overline{BGACK}$ low to $\overline{BG}$ high	t_{GALGH}		37 10/	9, 10, 11	1.5	3.5 +100 ns	1.5	3.5 +90 ns	1.5	3.5 +80 ns	1.5	3.5 +70 ns	Clk. Per.
$\overline{BGACK}$ low to $\overline{BR}$ high (to prevent rearbitration)	t_{GALBRH}		37A 10/	9, 10, 11	20 ns	1.5	20 ns	1.5	20 ns	1.5	20 ns	1.5	Clk. Per.

See footnotes at end of table.

★ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C < T_C < +110°C$ 4.75 V $\leq V_{CC} \leq$ 5.25 V unless otherwise specified	Waveform number (see figure 3)	Group A subgroups	Device type 01 6 MHz		Device type 02 8 MHz		Device type 03 10 MHz		Device type 04 12.0 MHz		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
$\overline{BG}$ low to bus high impedance (with $\overline{AS}$ high)	t_{GLZ}	GND = 0 V C_L = 130 pF See figure 3	38 4/	9, 10, 11		100		80		70		60	ns
$\overline{BG}$ width high	t_{GH}		39 10/	9, 10, 11	1.5		1.5		1.5		1.5		Clk. Per.
Clock low to $\overline{VMA}$ low	t_{CLVML}		40	9, 10, 11		80		70		70		70	ns
Clock low to E transition	t_{CLET}		41	9, 10, 11		85		70		55		45	ns
E output rise and fall time	$t_{Er,f}$		42 10/	9, 10, 11		25		25		25		25	ns
$\overline{VMA}$ low to E high	t_{VMLEH}		43 10/	9, 10, 11	240		200		150		90		ns
$\overline{AS}$, $\overline{DS}$ high to $\overline{VPA}$ high	t_{SHVPH}		44 10/	9, 10, 11	0	160	0	120	0	90	0	90	ns
E Low to address/$\overline{VMA}$/FC invalid	t_{ELCAI}		45 10/	9, 10, 11	35		30		10		10		ns
$\overline{BGACK}$ width low	t_{GAL}		46 10/	9, 10, 11	1.5		1.5		1.5		1.5		Clk. Per.
Asynchronous input setup/hold time	t_{ASI}		47 13/	9, 10, 11	25		20		20		20		ns
$\overline{BERR}$ low to $\overline{DTACK}$ low	t_{BELDAL}		48 10/ 15/	9, 10, 11	25		20		20		20		ns
E low to $\overline{AS}$, $\overline{DS}$ invalid	t_{SHEL}		49 10/	9, 10, 11	-80	+80	-70	+70	-55	+55	-45	45	ns
E width high	t_{EH}		50 10/	9, 10, 11	600		450		350		280		ns
E width low	t_{EL}		51 10/	9, 10, 11	900		700		550		440		ns
E executed rise time	t_{EICHX}		10/ 16/	9, 10, 11									ns

See footnotes at end of table.

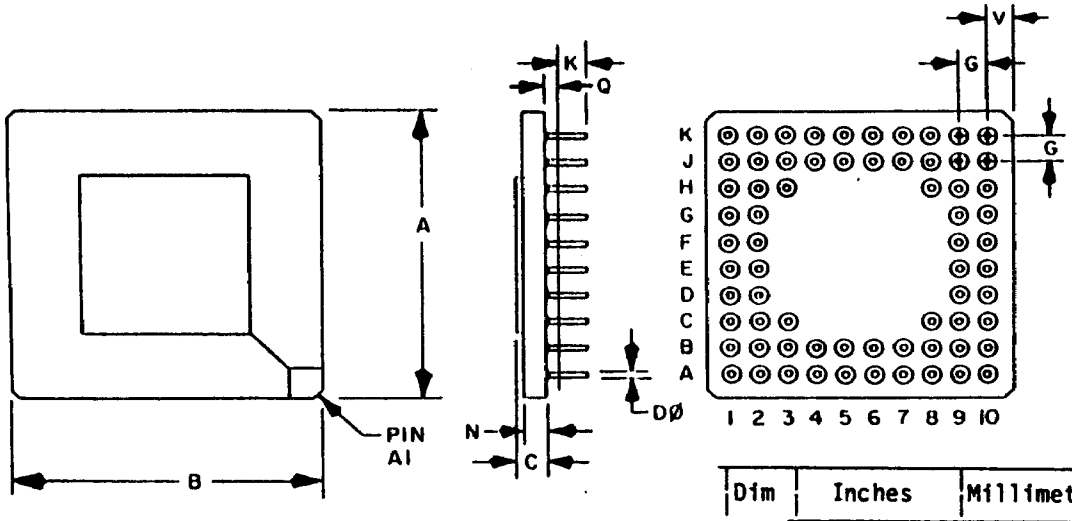
☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +110°C$ 4.75 V $\le V_{CC} \le$ 5.25 V unless otherwise specified	Waveform number (see figure 3)	Group A subgroups	Device type 01 6 MHz		Device type 02 8 MHz		Device type 03 10 MHz		Device type 04 12.0 Hz		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
Clock high to data out invalid	t_{CHDOI}	GND = 0 V C_L = 130 pF	53 10/	9, 10, 11	0		0		0		0		ns
E low to data out invalid	t_{ELDOI}	See figure 3	54 2/ 10/	9, 10, 11	40		30		20		15		ns
R/W to data bus impedance	t_{RLDBD}		55 10/	9, 10, 11	35		30		20		10		ns
HALT/RESET pulse width	t_{HRPW}		56 10/ 15/ 17/	9, 10, 11	10		10		10		10		Clk. Per.
BGACK high to AS, DS and R/W driven	t_{GASD}		57 10/	9, 10, 11	1.5		1.5		1.5		1.5		Clk. Per.
BGACK high to FC, VMA driven	t_{GAFCD}		57A 10/	9, 10, 11	1.0		1.0		1.0		1.0		Clk. Per.
BR high to AS, DS and R/W driven	t_{BRHSD}		58 10/ 14/	9, 10, 11	1.5		1.5		1.5		1.5		Clk. Per.
BR high to FC, VMA driven	t_{BRHFD}		58A 10/ 15/	9, 10, 11	1.0		1.0		1.0		1.0		Clk. Per.

1/ V_{CC} = 5 V ±5%.
2/ After V_{CC} has been applied for 100 ms.
3/ All outputs unloaded except for load capacitance. Clock should be either 4 MHz or F_{MAX}. Low; HALT, RST, (Part is held in reset). High; DTACK, BR, BGACK, IPL0-2, VPA, BERR.
4/ Guaranteed to the limits specified in table I, if not tested.
5/ FC invalid, as a minimum, tested initially and for process and design changes only.
6/ For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the values given in the maximum column.
7/ Not tested, for system design purposes only.
8/ Combined with the above parameter. Previous specification of 0 ns was theoretical and not attainable.
9/ Actual value depends on clock period.
10/ As a minumum, tested initially and for process or design changes only.
11/ When AS and R/W are equally loaded (±20%), subtract 10 nanoseconds from the values given in these columns.
12/ Combined with 16, control bus specification.
13/ If the asynchronous setup time (47) requirements are satisfied, the DTACK low to data setup time (31) requirement can be ignored. The data must only satisfy the data-in to clock-low setup time (27) for the following cycle.
14/ The processor will negate BG and begin driving the bus again if external arbitration logic negates BR before asserting BGACK.
15/ If 47 is satisfied for both DTACK and BERR, 48 may be 0 ns.
16/ Deleted, useful only if E clock used to drive clock input on MC6809 Microprocessor.
17/ For power up, the MPU must be held in RESET state for 100 ms to all stabilization of on chip circuitry. After the system is powered up, 56 refers to the minimum pulse width required to reset the system.

Device types 01, 02, 03, and 04



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	1.040	1.080	26.41	27.43
B	1.040	1.080	26.41	27.43
C	.083	.102	2.10	2.59
DØ	.017	.024	0.43	0.60
G	.100 BSC		2.54 BSC	
K	.120	.140	3.05	3.55
N	.072	.088	1.83	2.23
V	.070	.090	1.79	2.28
Q	.040	.060	1.02	1.52

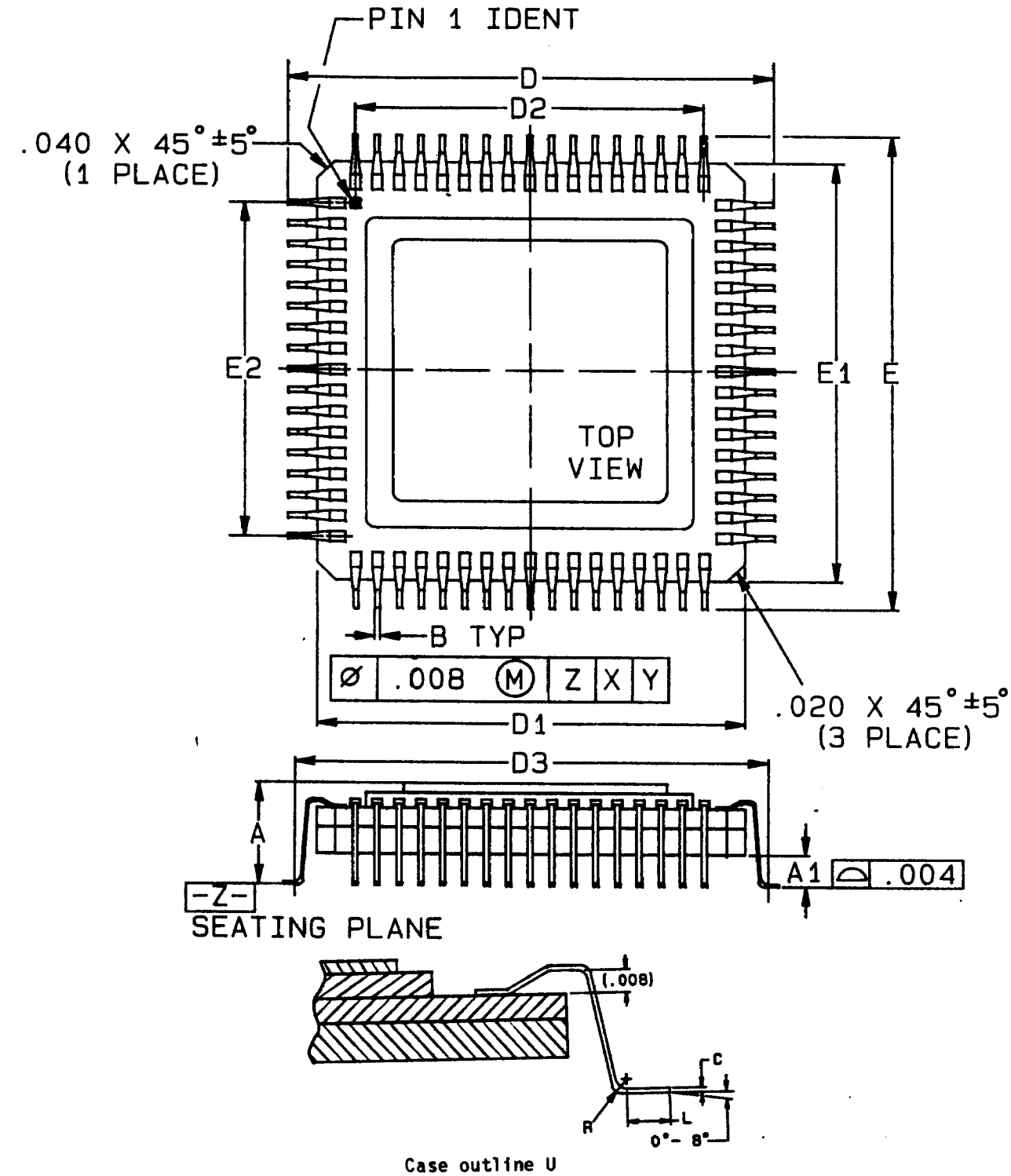
Case outline T

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Positional tolerance for leads (68 places):

⌖	Ø.005 (0.13 mm) Ⓜ

4. Manufacturers option, chamfer 0.15 max at 45°, all edges.
5. There shall be a 0.20 inch minimum spacing between any 2 metallized areas on the surfaces of the package.
6. Increase maximum limit of pin diameter (DØ) by 0.003 inches when lead finish A is applied.

FIGURE 1. Dimensions and configurations.



Case outline U

FIGURE 1. Dimensions and configurations - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		82021
		REVISION LEVEL E	SHEET 11

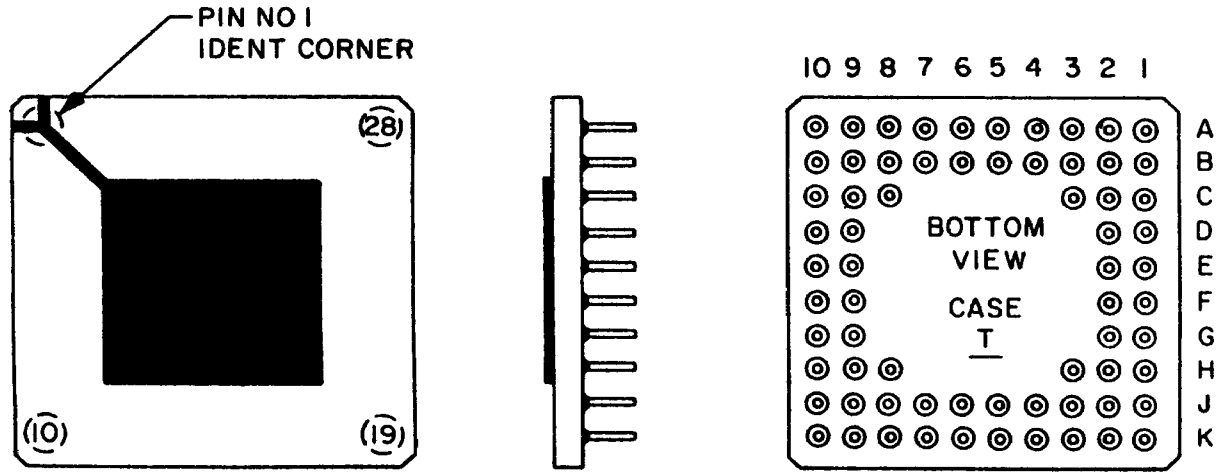
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.135	---	3.42
A1	0.015	0.038	0.38	0.96
B	0.013	0.025	0.33	0.63
C	0.004	0.010	0.10	0.25
D, E	1.130	1.150	28.70	29.21
D1, E1	0.935	0.960	27.74	24.38
D2, E2	.800		20.32	
D3	1.080		27.43	
L	.022	.038	0.55	0.96
R	.012		.030	

Case outline U - Continued.

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. D_2 and E1 dimensions do not include particles of package material. Such particles shall not exceed .010 inch.
4. Maximum lead thickness includes all lead finishes. Minimum dimension is base material.
5. A pin one identification mark shall be located adjacent to pin one within the shaded area shown.

FIGURE 1. Dimensions and configurations - Continued.

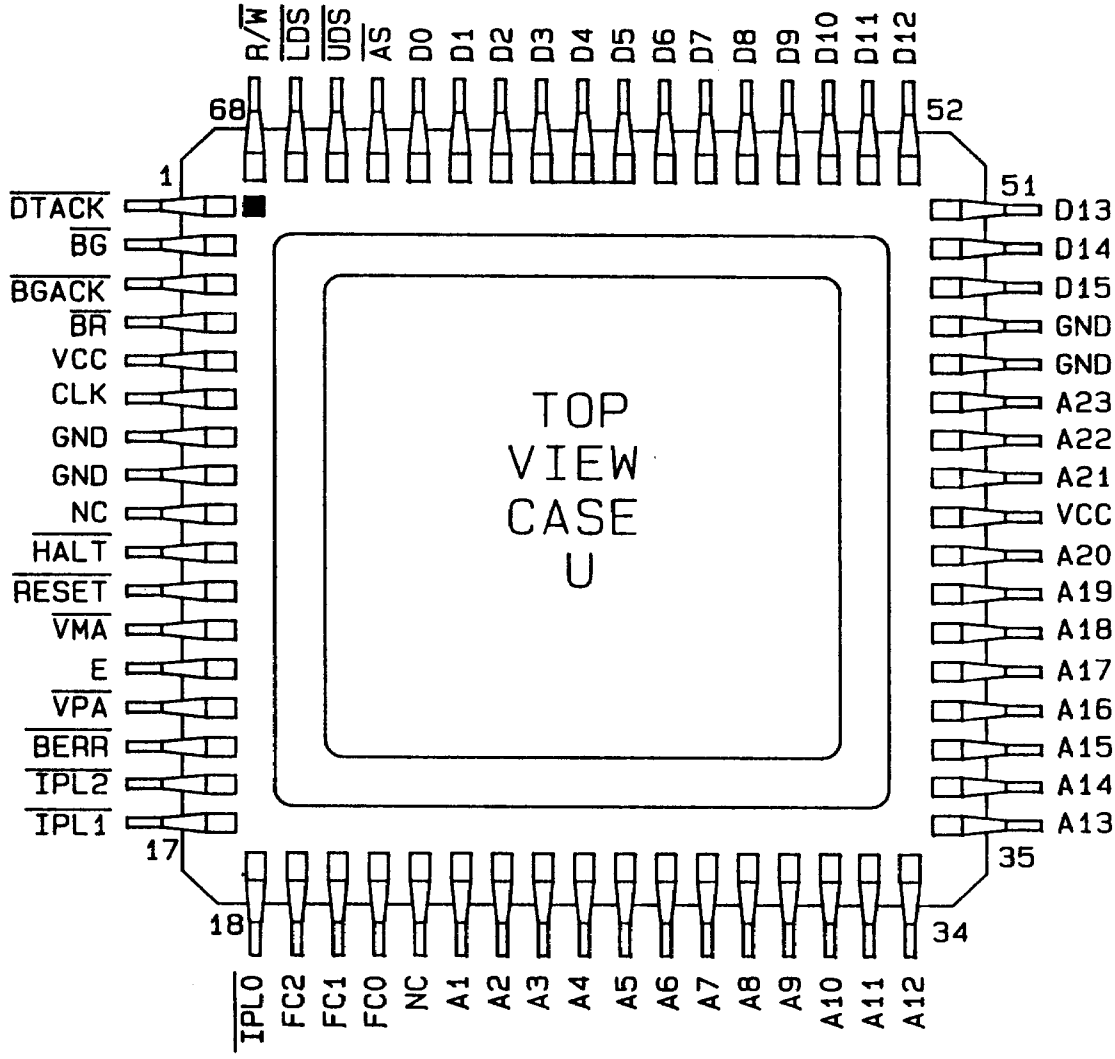
Device types 01, 02, 03, and 04



Pin no.	Function	Pin no.	Function	Pin no.	Function	Pin no.	Function
1A	Do not connect	9K	A9	3A	D1	9H	A12
1B	$\overline{\text{DTACK}}$	10K	Do not connect	2A	$\overline{\text{AS}}$	9G	A15
1C	$\overline{\text{BGACK}}$	10J	A14	2B	$\overline{\text{LDS}}$	9F	A18
1D	$\overline{\text{BR}}$	10H	A16	2C	$\overline{\text{BG}}$	9E	V_{CC}
1E	CLK	10G	A17	2D	V_{CC}	9D	GND
1F	$\overline{\text{HALT}}$	10F	A19	2E	GND	9C	A23
1G	$\overline{\text{VMA}}$	10E	A20	2F	$\overline{\text{RESET}}$	9B	D14
1H	$\overline{\text{E}}$	10D	A21	2G	$\overline{\text{VPA}}$	8B	D11
1J	$\overline{\text{BERR}}$	10C	A22	2H	$\overline{\text{IPL2}}$	7B	D9
1K	Do not connect	10B	D15	2J	$\overline{\text{IPL0}}$	6B	D6
2K	FC2	10A	D12	3J	FC1	5B	D3
3K	FC0	9A	D10	4J	Do not connect	4B	$\overline{\text{DØ}}$
4K	A1	8A	D8	5J	A2	3B	$\overline{\text{UDS}}$
5K	A3	7A	D7	6J	A5	3C	$\overline{\text{R/W}}$
6K	A4	6A	D5	7J	A8	3H	$\overline{\text{IPL1}}$
7K	A6	5A	D4	8J	A10	8H	A13
8K	A7	4A	D2	9J	A11	8C	D13

FIGURE 2. Terminal connections.

Device types 02 and 03



NC = NO connection

FIGURE 2. Terminal connections - Continued.

Device types 01, 02, 03, and 04

TERMINAL ASSIGNMENT

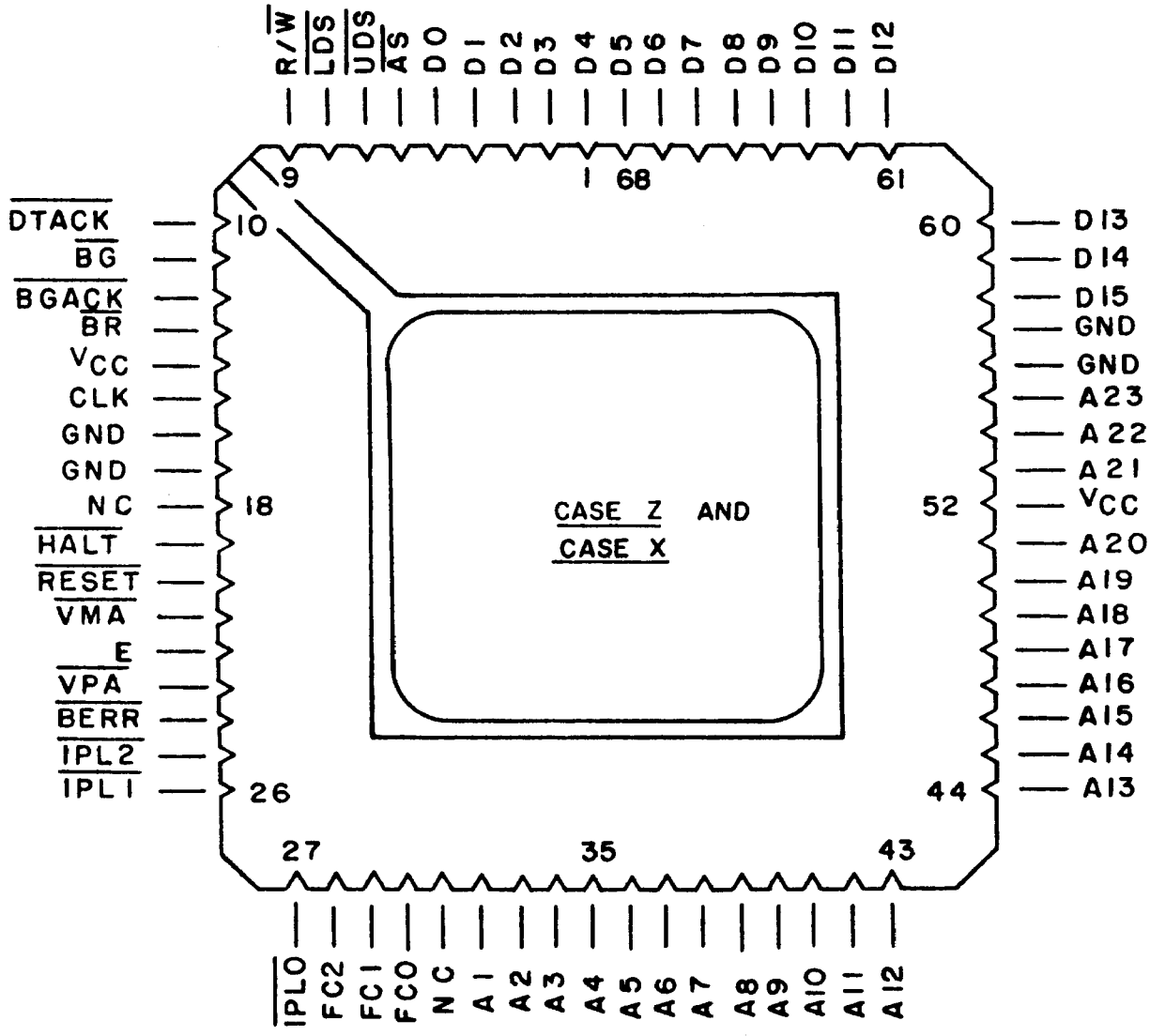


FIGURE 2. Terminal connections (top view) - Continued.

Device types 01, 02, 03, and 04

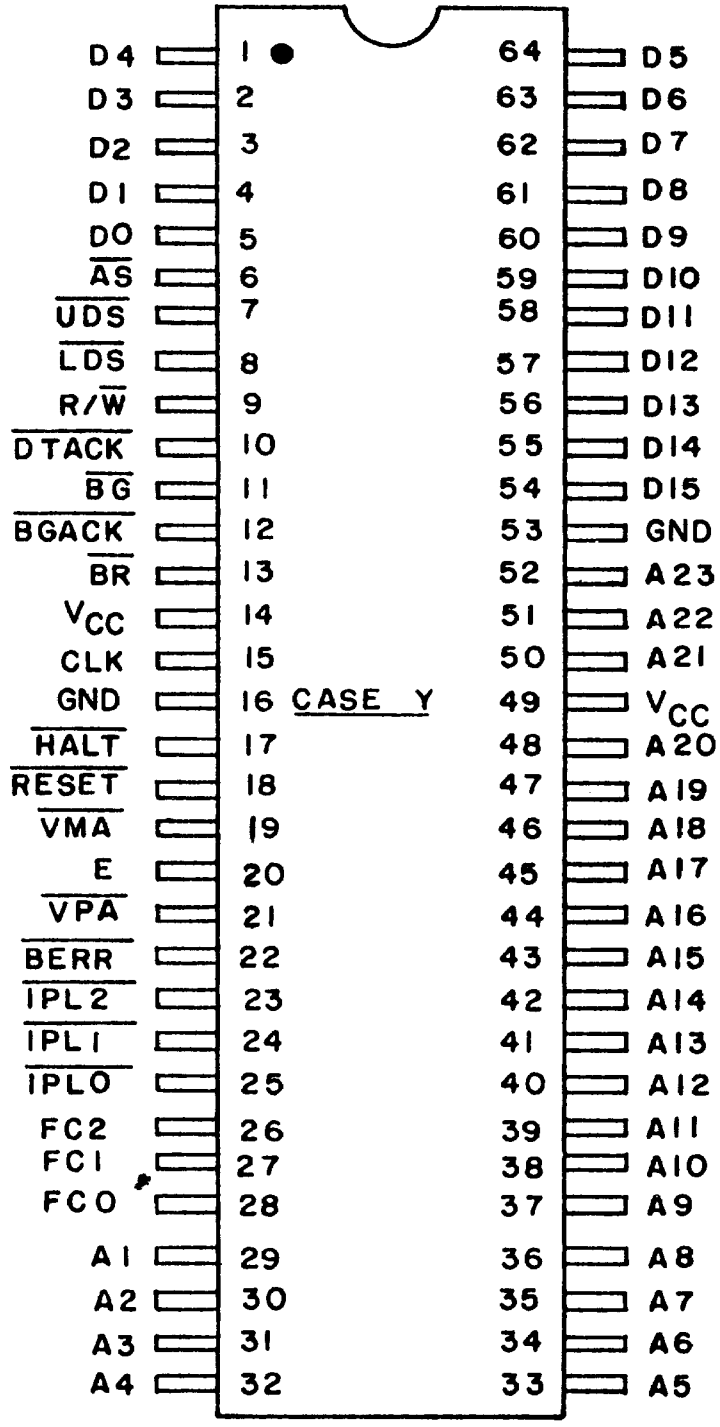
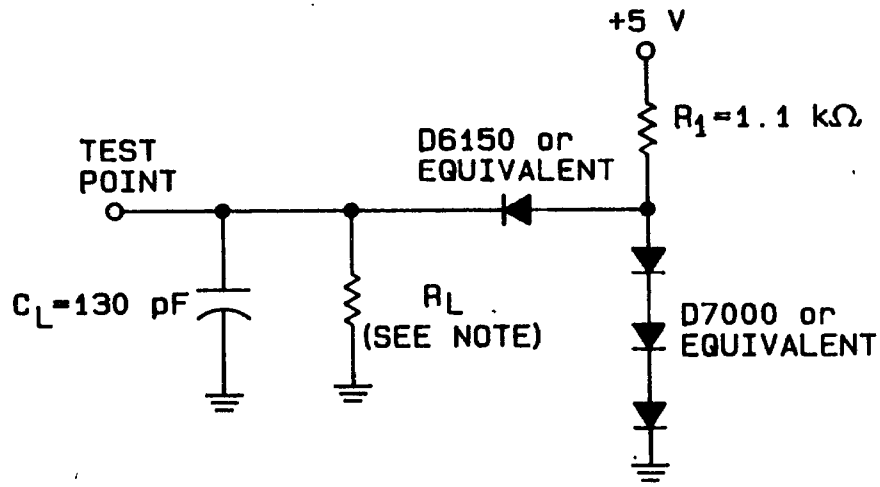
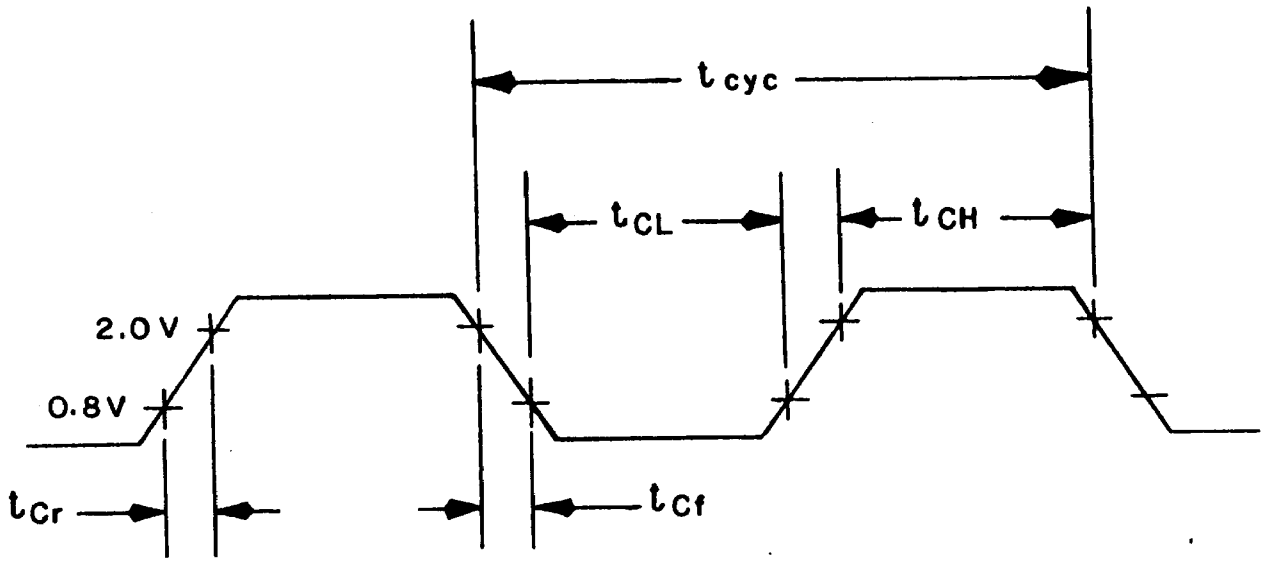


FIGURE 2. Terminal connections (top view) - Continued.



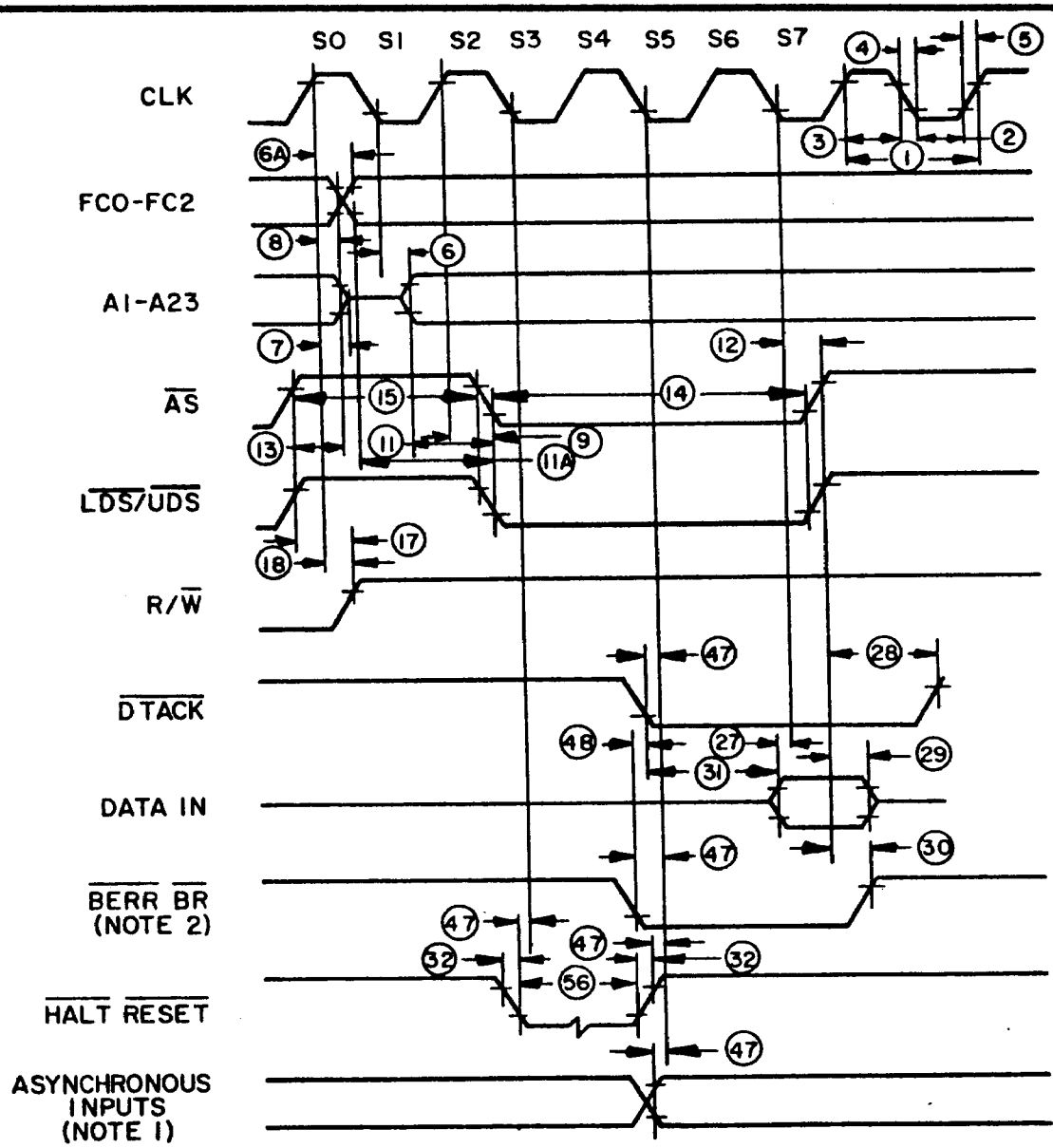
Test circuit

NOTE: R_L = 6.0 kΩ for $\overline{AS}$, A1 - A23, $\overline{BG}$, D0-D15, E, FC0 - FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$



Input clock waveform

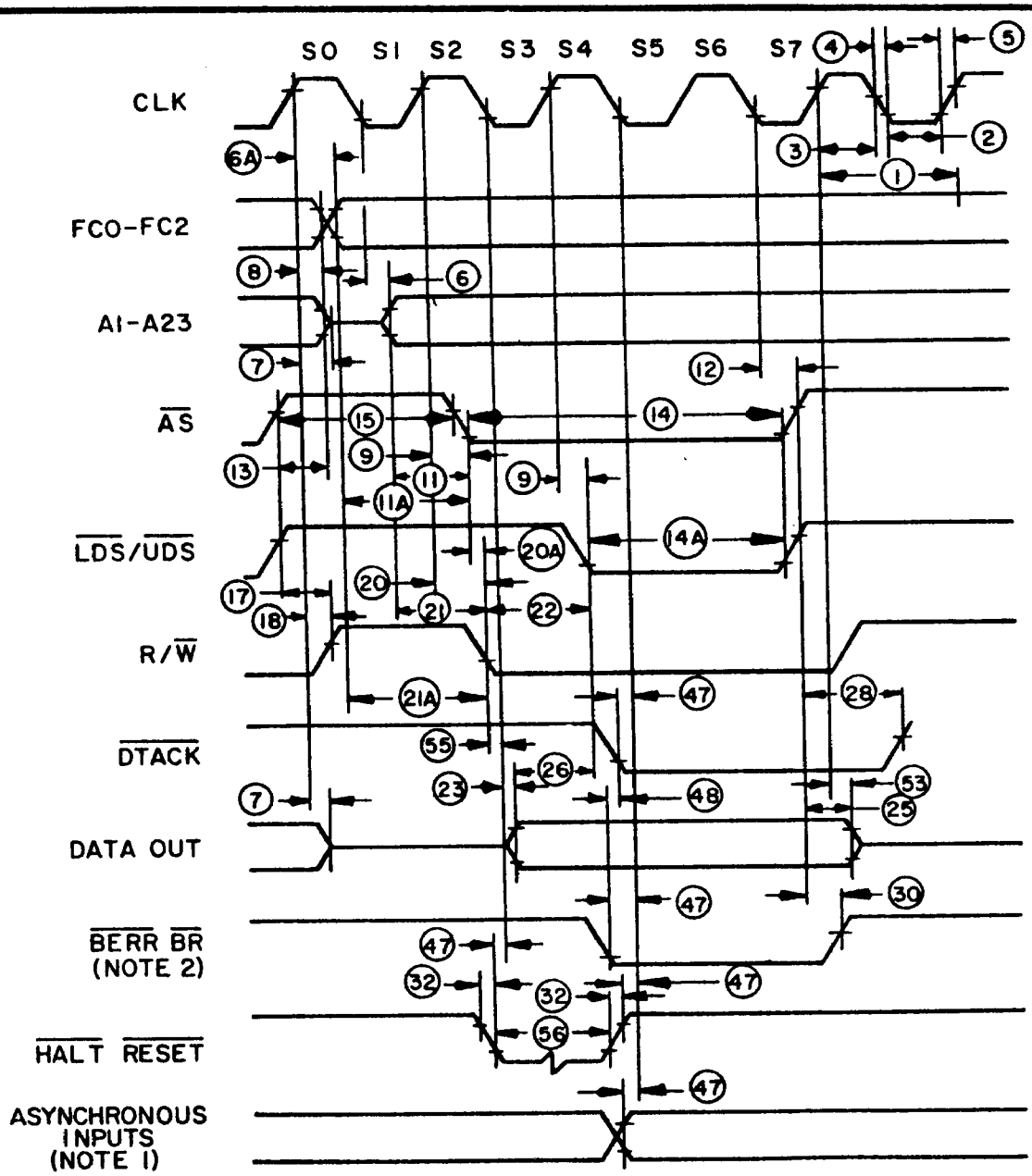
FIGURE 3. Switching test circuit and waveforms.



Read cycle timing diagram.

NOTES:
1. Setup time for the asynchronous inputs BGACK, IPL0-2, and VPA guarantees their recognition at the next falling edge of the clock.
2. BR need fall at this time only to insure being recognized at the end of this bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 and 2.0 volts.

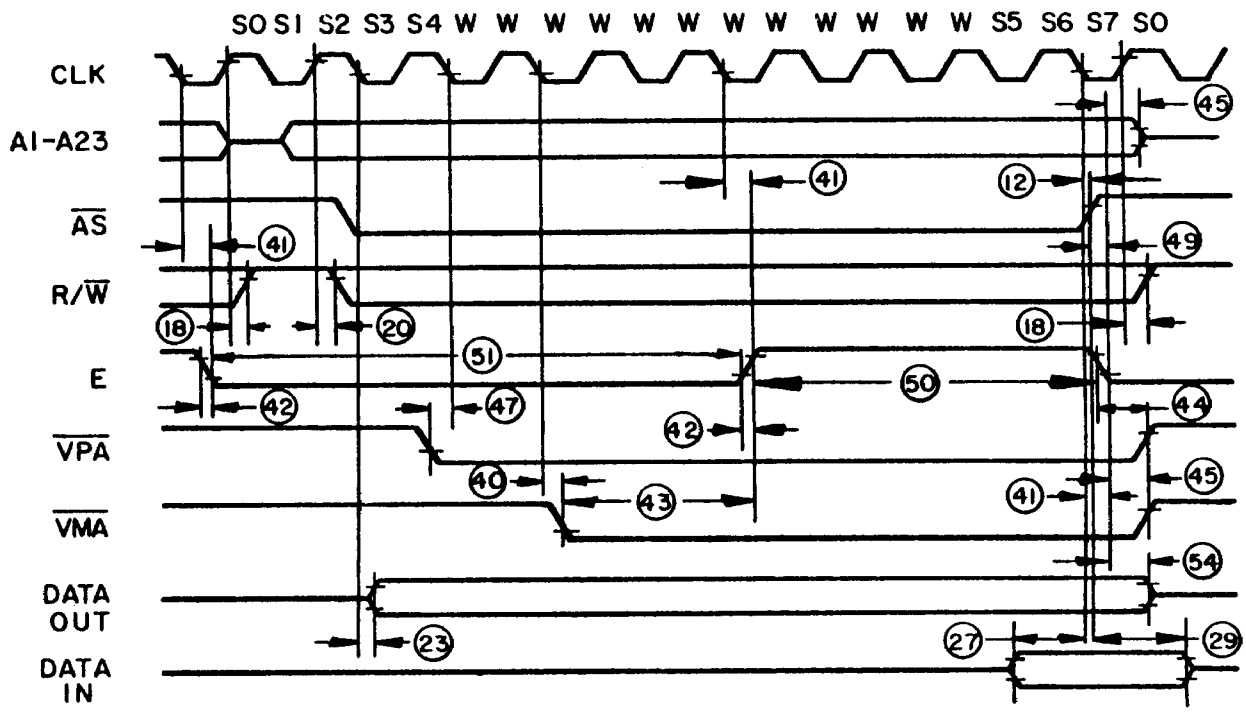
FIGURE 3. Switching test circuit and waveforms - Continued.



Write cycle timing diagram

NOTES:
1. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volts and 2.0 volts.
2. Because of loading variations, R/$\overline{W}$ may be valid after $\overline{AS}$ even though both are initiated by the rising edge of S2 (Specification 20A).

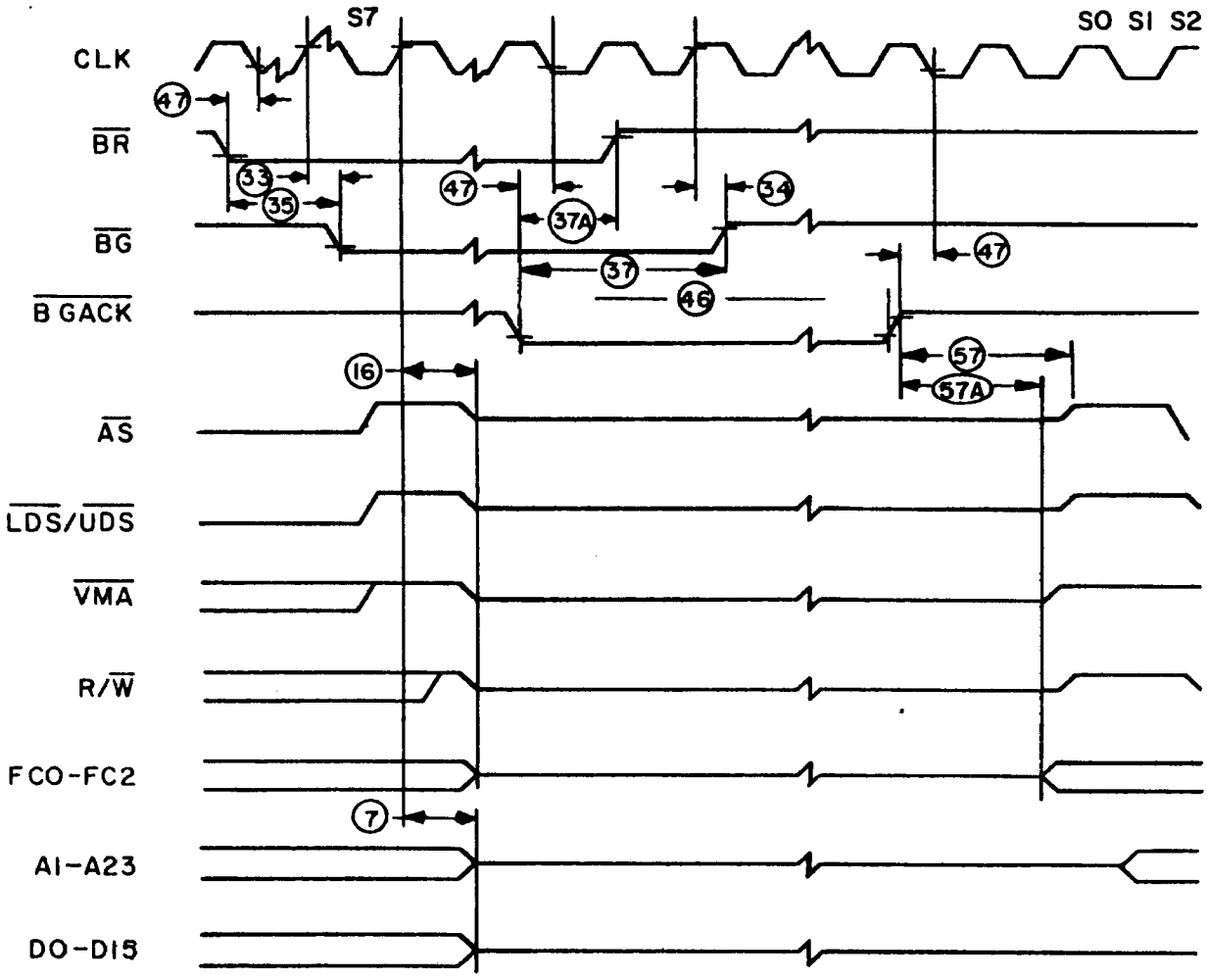
FIGURE 3. Switching test circuit and waveforms - Continued.



M068000 to M6800 peripheral diagram - BPST case

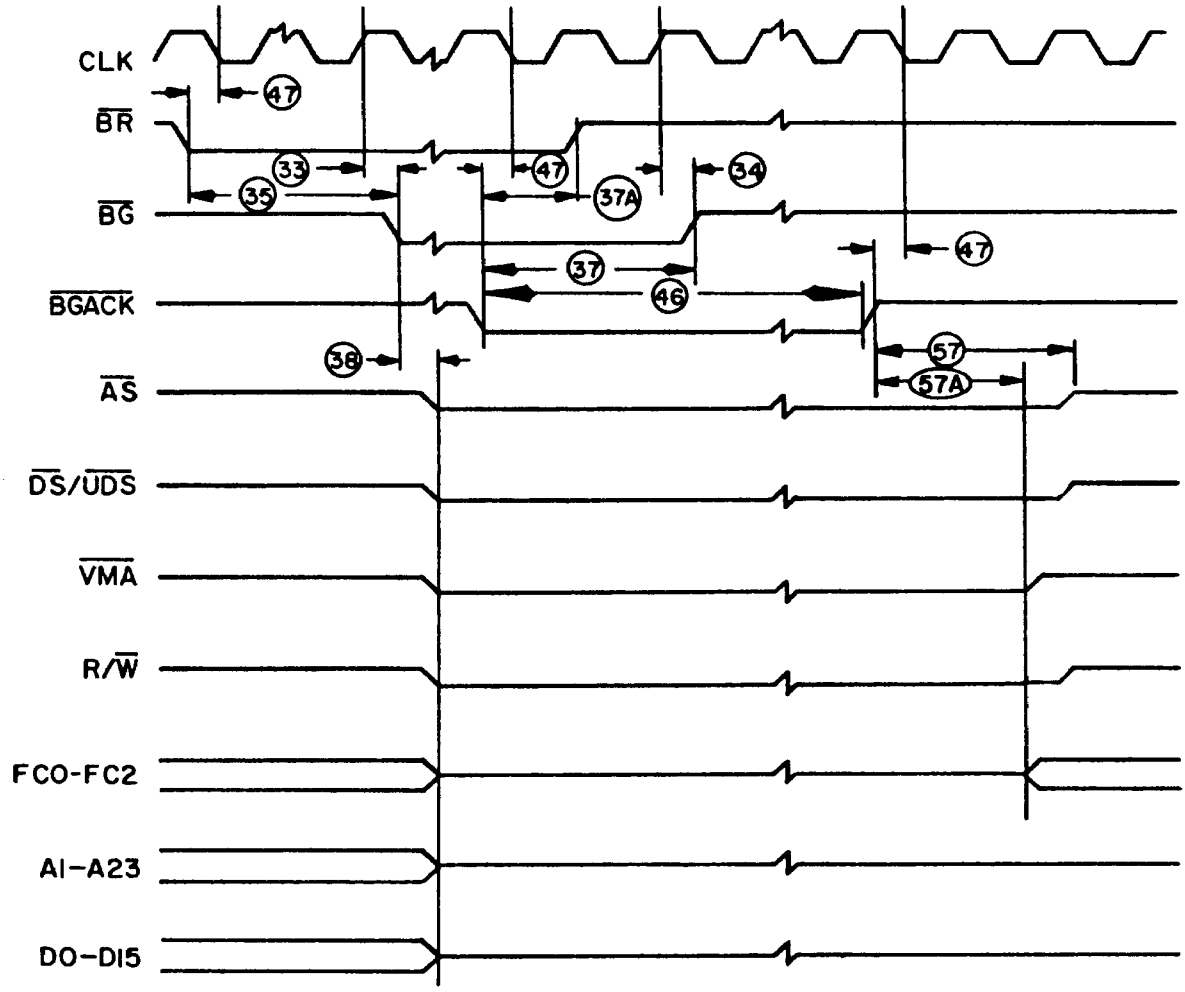
NOTE: This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the best case possibly attainable.

FIGURE 3. Switching test circuit and waveforms - Continued.



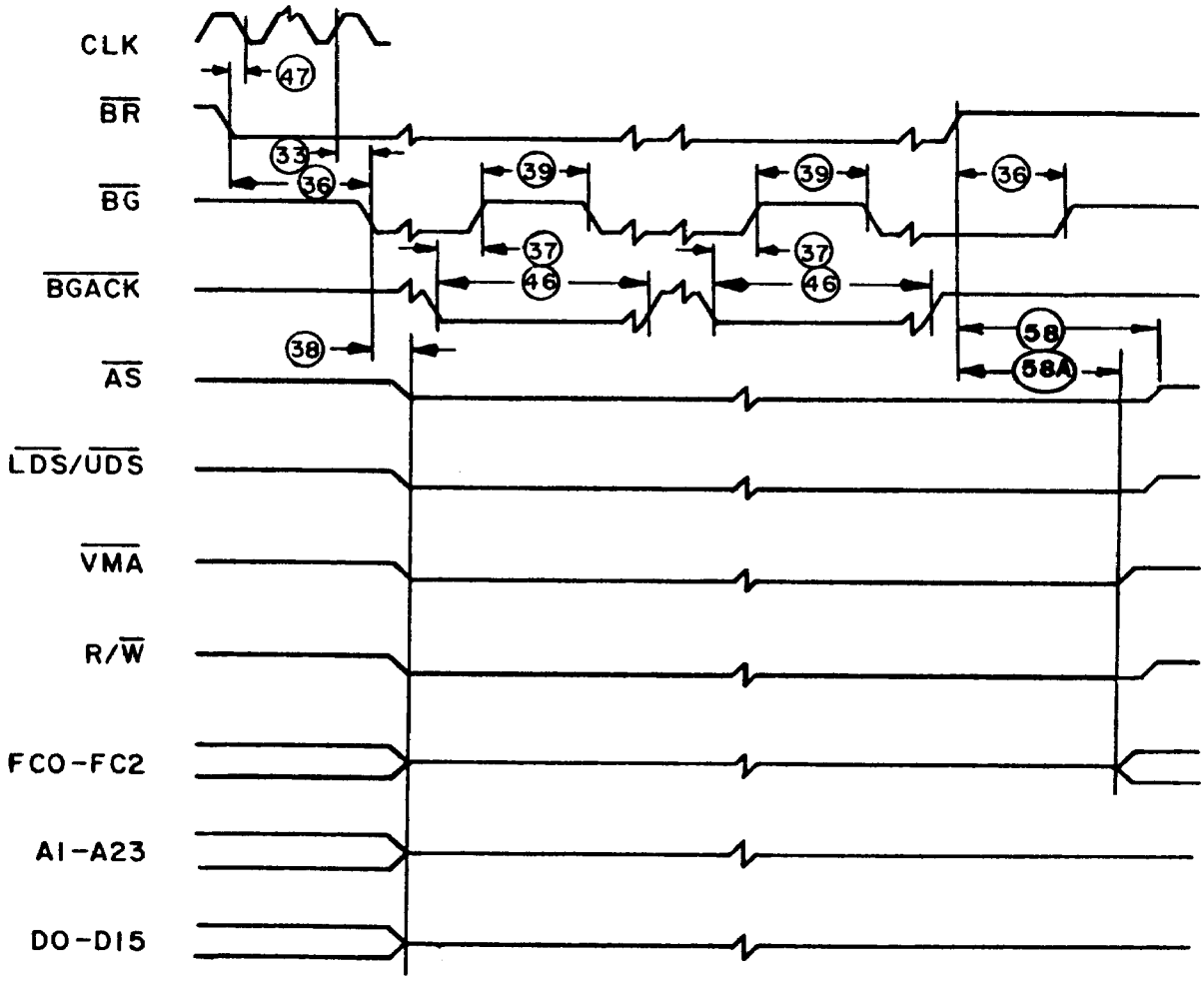
Bus arbitration timing diagram - active bus case

FIGURE 3. Switching test circuit and waveforms - Continued.



Bus arbitration timing diagram - idle bus case

FIGURE 3. Switching test circuit and waveforms - Continued.



Bus arbitration timing diagram - multiple bus requests

FIGURE 3. Switching test circuit and waveforms - Continued.

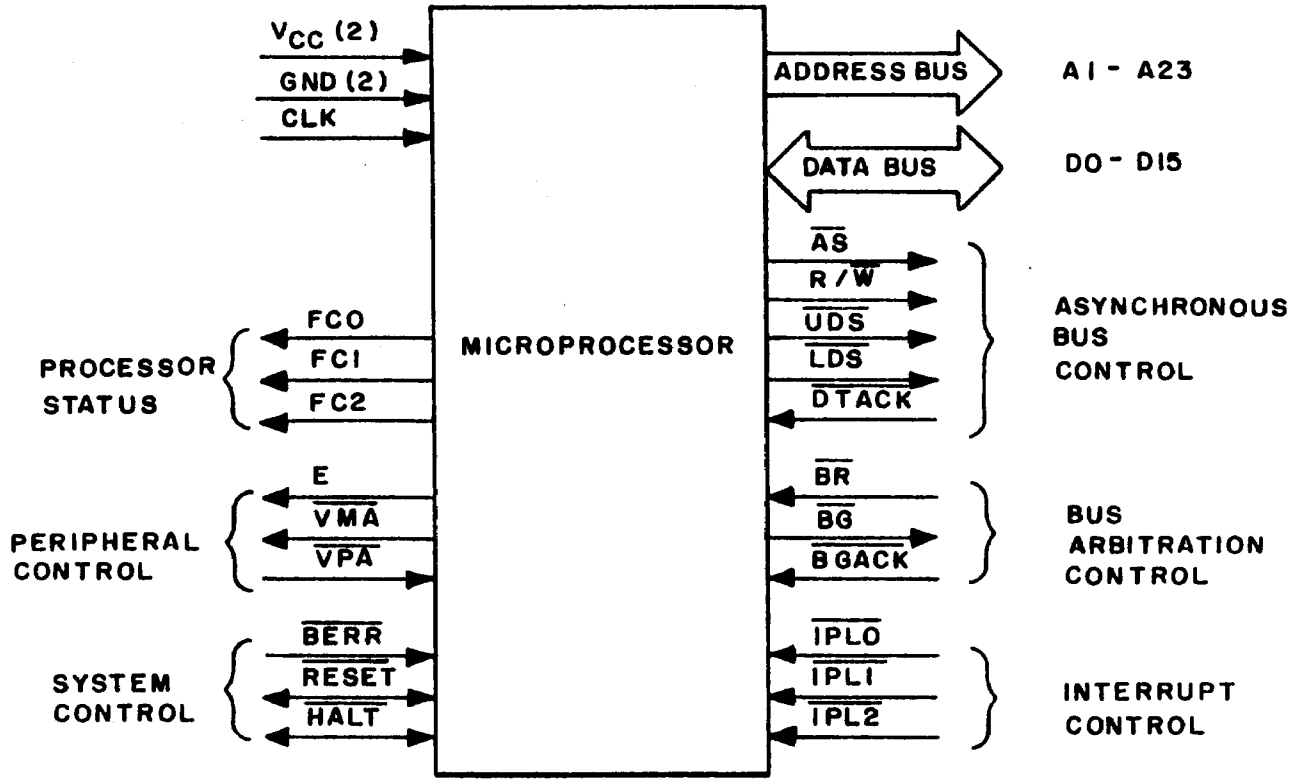


FIGURE 4. Input and output signals.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D, or E using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. Subgroups 7 and 8 functional testing shall include verification of instruction set. The instruction set forms a part of the vendors test tape and shall be maintained and available from the approved sources of supply.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1, 7
Final electrical test parameters (method 5004)	1*, 2*, 7, 8(at 110°C only), 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8(at 110°C only)

* PDA applies to subgroup 1 or 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883,

(1) Test condition A, B, C, D, or E using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/540--B--.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio, 45444, or telephone (513) 296-5375.

6.6 Terminal and pin definitions.

Signal summary. The input and output signals can be functionally organized into groups shown on figure 4 and in table III.

TABLE III. Signal summary.

Signal name	Mnemonic	Input/output	Active state	Hi-Z	
				On $\overline{\text{HALT}}$	On $\overline{\text{BGACK}}$
Address Bus	A1-A23	output	high	yes	yes
Data Bus	D0-D15	input/output	high	yes	yes
Address Strobe	$\overline{\text{AS}}$	output	low	no	yes
Read/Write	R/$\overline{\text{W}}$	output	read-high write-low	no	yes
Upper and Lower Data Strobes	$\overline{\text{UDS}}$, $\overline{\text{LDS}}$	output	low	no	yes
Data Transfer Acknowledge	$\overline{\text{DTACK}}$	input	low	no	no
Bus Request	$\overline{\text{BR}}$	input	low	no	no
Bus Grant	$\overline{\text{BG}}$	output	low	no	no
Bus Grant Acknowledge	$\overline{\text{BGACK}}$	input	low	no	no
Interrupt Priority Level	$\overline{\text{IPL0}}$, $\overline{\text{IPL1}}$, $\overline{\text{IPL2}}$	input	low	no	no
Bus Error	$\overline{\text{BERR}}$	input	low	no	no
Reset	$\overline{\text{RESET}}$	input/output	low	no 1/	no 1/
Halt	$\overline{\text{HALT}}$	input/output	low	no 1/	no 1/
Enable	E	output	high	no	no
Valid Memory Address	$\overline{\text{VMA}}$	output	low	no	yes
Valid Peripheral Address	$\overline{\text{VPA}}$	input	low	no	no
Function Code Output	FC0, FC1, FC2	output	high	no	yes
Clock	CLK	input	high	no	no
Power Input	V_{CC}	input			
Ground	GND	input			

1/ Open drain

Address Bus (A1 through A23). This 23-bit, unidirectional, three-state bus is capable of addressing 8 megawords of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 provide information about what level interrupt is being serviced while address lines A4 through A23 are all set to a logic high.

Data Bus (D0 through D15). This 16-bit, bidirectional, three-state bus is the general purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0 through D7.

Asynchronous Bus Control. Asynchronous data transfers are handled using the following control signals: Address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

Address Strobe ($\overline{AS}$). This signal indicates that there is a valid address on the address bus.

Read/Write ($\overline{R/W}$). This signal defines the data bus transfer as a read or write cycle. The $\overline{R/W}$ signal also works in conjunction with the upper and lower data strobes as explained in the following paragraph.

Upper and Lower Data Strobes ($\overline{UDS}$, $\overline{LDS}$). These signals control the data on the data bus as shown in table IV. When the R/W line is high, the processor will read from the data bus as indicated. When the R/W line is low, the processor will write to the data bus as shown.

TABLE IV. Data strobe control of data bus.

$\overline{UDS}$	$\overline{LDS}$	R/$\overline{W}$	D8-D15	D0-D7
High	High		No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7	Valid data bits 0-7
Low	High	Low	Valid data bits 8-15	Valid data bits 8-15

Data Transfer Acknowledge ($\overline{DTACK}$). This input indicates that the data transfer is completed. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated.

Bus Arbitration Control. These three signals form a bus arbitration circuit to determine which device will be the bus master device.

Bus Request ($\overline{BR}$). This input is wire ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

Bus Grant ($\overline{BG}$). This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

Bus Grant Acknowledge ($\overline{BGACK}$). This input indicates that some other device has become the bus master. This signal cannot be asserted until the following four conditions are met:

a. A bus grant has been received.
b. Address strobe is inactive which indicates that the microprocessor is not using the bus.
c. Data transfer acknowledge is inactive which indicates that either memory or the peripherals are not using the bus.
d. Bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership.

Interrupt Control ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$). These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. The least significant bit is contained in $\overline{IPL0}$ and the most significant bit is contained in $\overline{IPL2}$.

System Control. The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

Bus Error ($\overline{BERR}$). This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

a. Nonresponding devices.
b. Interrupt vector number acquisition failure.
c. Illegal access request as determined by a memory management unit.
d. Other application dependent errors.

The bus error signal interacts with the halt signal to determine if exception processing should be performed or the current bus cycle should be retired.

Reset ($\overline{RESET}$). This bidirectional signal line acts to reset (initiate a system initialization sequence) the processor in response to an external reset signal. An internally generated reset (result of a RESET instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external halt and reset signals applied at the same time.

Halt ($\overline{HALT}$). When this bidirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are put in their impedance state.

When the processor has stopped executing instructions, such as in a double bus fault condition, the halt line is driven by the processor to indicate to external devices that the processor has stopped.

Peripheral Control. These control signals are used to allow the interfacing of synchronous peripheral devices with the asynchronous processor. These signals are explained in the following paragraphs.

Enable (E). This signal is the standard enable signal common to all peripheral devices. The period for this output is ten clock periods (six clocks low; four clocks high).

Valid Peripheral Address ($\overline{VPA}$). This input indicates that the device or region addressed is a family device and that data transfer should coincide with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt.

Valid Memory Address ($\overline{VMA}$). This output is used to indicate to peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal only responds to a valid peripheral address ($\overline{VPA}$) input which indicates that the peripheral is a family device.

Processor Status (FC0, FC1, FC2). These function code outputs indicate the mode (user or supervisor) and the cycle type currently being executed as shown in table V. The information indicated by the function code outputs is valid whenever address strobe ($\overline{AS}$) is active.

TABLE V. Function code outputs.

FC2	FC1	FC0	Cycle type
Low	Low	Low	(Undefined, reserved)
Low	Low	High	User data
Low	High	Low	User program
Low	High	High	(Undefined, reserved)
High	Low	Low	(Undefined, reserved)
High	Low	High	Supervisor data
High	High	Low	Supervisor program
High	High	High	Interrupt acknowledge

Clock (CLK). The clock input is a TTL compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input shall be a constant frequency.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
8202101TX	18324 50088	68000-6/BTA TS68000MRB/C6	M38510/54001BTX
8202101YX 2/	18324 50088	68000-6/BXA TS68000MCB/C6	M38510/54001BYX
8202101ZX 2/	18324 50088	68000-6/BUA TS68000MEB/C6	M38510/54001BZX
8202102TX	04713 18324 50088	68000-8/BZAJC 68000-8/BTA TS68000MRB/C8	M38510/54002BTX

See footnotes at end of table.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
8202102UC	04713	68000-8/BYCJC	
8202102XX	04713	68000-8T/BUXJC	
8202102YX 2/	04713 18324 50088	68000-8/BXAJC 68000-8/BXA TS68000MCB/C8	M38510/54002BYX
8202102ZX 2/	04713 18324 50088	68000-8/BUXJC 68000-8/BUA TS68000MEB/C8	M38510/54002BZX
8202103TX	04713 18324 50088	68000-10/BZAJC 68000-10/BTA TS68000MRB/C10	M38510/54003BTX
8202103UC	04713	68000-10/BYCJC	
8202103XX	04713	68000-10T/BUXJC	
8202103YX	04713 18324 50088	68000-10/BXAJC 68000-10/BXA TS68000MCB/C10	M38510/54003BYX
8202103ZX	04713 18324 50088	68000-10/BUCJC 68000-10/BUA TS68000MEB/C10	M38510/54003BZX
8202104TX	04713 50088	68000-12/BZAJC TS68000MRB/C12	M38510/54004BTX
8202104XX	04713	68000-12T/BUXJC	
8202104YX	04713 50088	68000-12/BXAJC TS68000MCB/C12	M38510/54004BYX
8202104ZX	04713 50088	68000-12/BUXJC TS68000MEB/C12	M38510/54004BZX

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Inactive for new design. Use applicable QPL-M38510 device.

Vendor CAGE number	Vendor name and address
04713	Motorola Semiconductor 7402 South Price Road Tempe, AZ 85283
18324	Signetics Corporation 4130 South Market Court Sacramento, CA 95834
50088	SGS Thompson Components P.O. Box 169 1310 Electronics Dr. Carrollton, TX 75006