

4K-bit TTL bipolar PROM (512 x 8)**82S141****FEATURES**

- Address access time: 90ns max
- Input loading: -150µA max
- On-chip address decoding
- No separate fusing pins
- Fully TTL compatible
- Outputs: 3-State
- Unprogrammed outputs are Low level

- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

APPLICATIONS

- Prototyping/volume production
- Sequential controllers

DESCRIPTION

The 82S141 is field programmable, which means that custom patterns are immediately available by following the Philips Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S141 includes on-chip decoding and four chip enable inputs for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

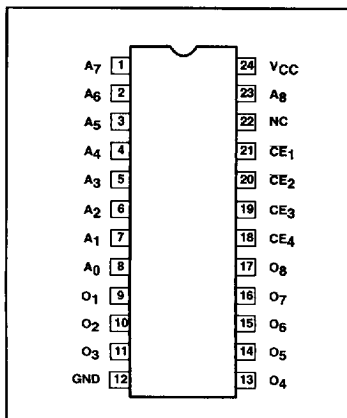
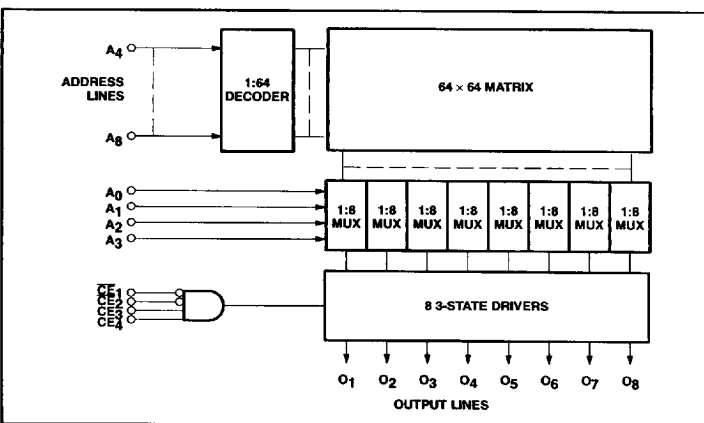
ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24-pin Ceramic DIP (600mil-wide)	82S141/BJA	GDIP1-T24
24-pin Ceramic Flat Pack	82S141/BKA	GDFP2-F24

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	+7	V _{DC}
V _I	Input voltage	+5.5	V _{DC}
V _O	Output voltage Off-State	+5.5	V _{DC}
T _A	Operating temperature range	-55 to +125	°C
T _{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION**BLOCK DIAGRAM**

March 31, 1992

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853-0260 06265

7110826 0085863 002

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82S141

DC ELECTRICAL CHARACTERISTICS

 $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS ^{1, 2}	LIMITS			UNIT
			Min	Typ ⁵	Max	
Input voltage						
V _{IL}	Low	V _{CC} = 4.5V, I _I = -18mA	2.0	-0.8	0.8	V
V _{IH}	High				V	
V _{IK}	Clamp				-1.2	V
Output voltage						
V _{OL}	Low	V _{CC} = 4.5V, CE _{1,2} = Low, CE _{3,4} = High I _O = 9.6mA I _O = -2mA	2.4		0.5	V
V _{OH}	High				V	
Input current						
I _{IL}	Low	V _{CC} = 5.5V V _I = 0.45V V _I = 5.5V			-150	μA
I _{IH}	High				40	μA
Output current						
I _{OZ}	Hi-Z state	V _{CC} = 5.5V CE _{1,2} = High, CE _{3,4} = Low, V _O = 5.5V CE _{1,2} = High, CE _{3,4} = Low, V _O = 0.4V			+40 -40	μA μA
I _{OS}	Short circuit ³	CE _{1,2} = Low, CE _{3,4} = High, V _O = 0V V _{CC} = 5.5V, High Stored	-15		-85	mA
Supply current						
I _{CC}		CE _{1,2} = High, CE _{3,4} = Low V _{CC} = 5.5V		125	185	mA
Capacitance ⁶						
C _{IN}	Input	V _{CC} = 5.0V, CE _{1,2} = High V _I = 2.0V V _O = 2.0V		5	10	pF
C _{OUT}	Output				8	13

AC ELECTRICAL CHARACTERISTICS

 $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ ⁵	Max	
t_{AA}	Access time ⁴	Output	Address		50	90	ns
t_{CE}		Output	Chip enable		20	50	ns
t_{CP}	Disable time	Output	Chip disable		20	50	ns

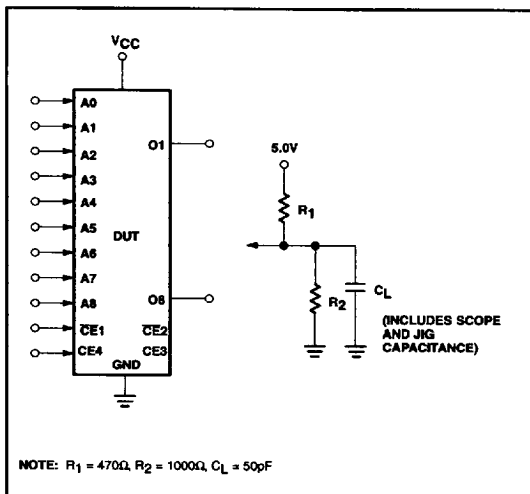
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μs .
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = +25^{\circ}\text{C}$.
6. Guaranteed, but not tested.

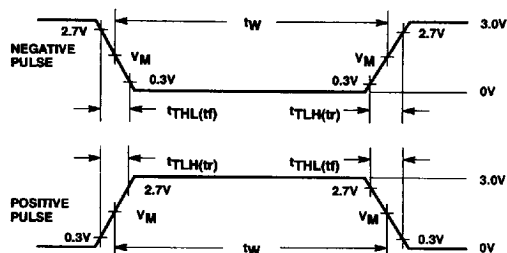
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TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	$\leq 5\text{ns}$	$\leq 5\text{ns}$

TIMING DIAGRAMS

