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Status	Product Specification
Memory Products	

82S185
8K-bit TTL bipolar PROM

DESCRIPTION

The 82S185 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S185 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and one Chip Enable input for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S185 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

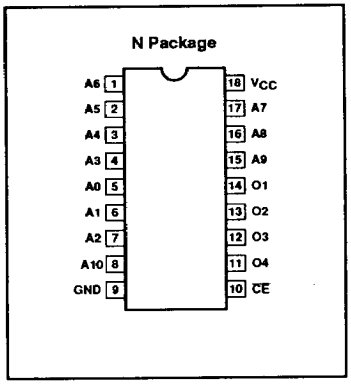
FEATURES

- Low power dissipation: 50μW/bit typ
- Address access time: 100ns max
- Input loading: -100μA max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- One Chip Enable input
- Outputs: 3-State

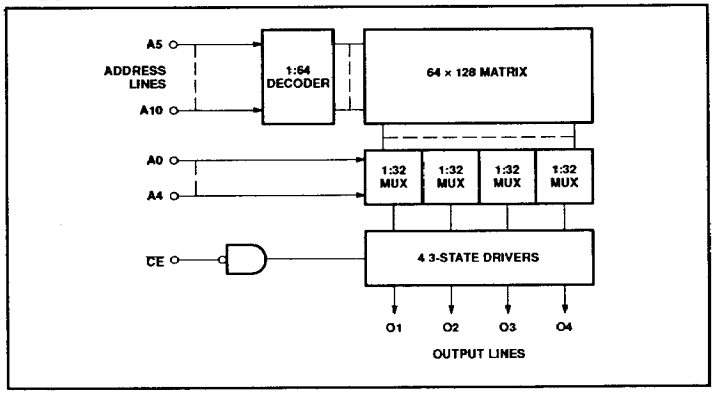
APPLICATIONS

- Sequential controllers
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



8K-bit TTL bipolar PROM (2048 × 4) — 82S185

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-Pin Plastic Dual-In-Line 300mil-wide	N82S185 N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS Min	LIMITS Typ[3]	LIMITS Max	UNIT
Input voltage[1]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	I_{IN} = -12mA		-0.8	-1.2	V
Output voltage[1]						
		$\overline{CE}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.45	V
V_{OH}	High	I_{OUT} = -2mA	2.4			V
Input current[2]						
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
I_{OZ}	Hi-Z state	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40	µA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40	µA
I_{OS}	Short circuit [4]	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	-15		-70	mA
Supply current[5]						
I_{CC}		V_{CC} = 5.25V		90	120	mA
Capacitance						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

NOTES:
1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
4. Duration of short circuit should not exceed 1 second.
5. Measured with all inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS

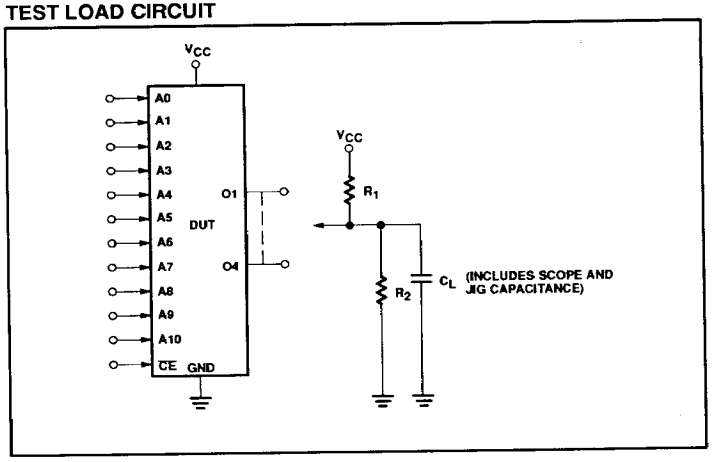
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time[2]							
t_{AA}		Output	Address		70	100	ns
t_{CE}		Output	Chip Enable		30	40	ns
Disable time[3]							
t_{CD}		Output	Chip Disable		30	40	ns

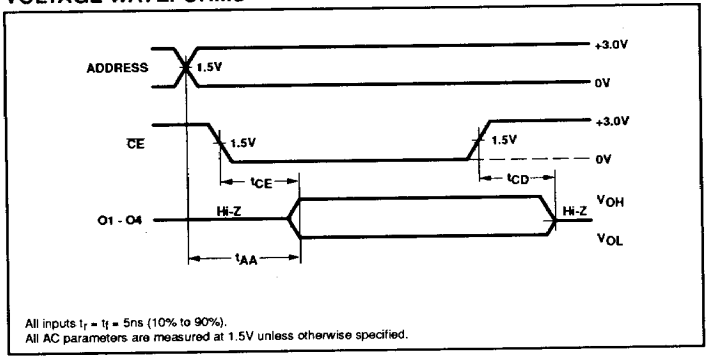
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. Tested at an address cycle time of 1μs.
3. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.