REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Convert to military drawing format. Case E inactive for new design. Change V_{IL}, t_{PLH1}, t_{PHL1}, and t_{PLH2}. Delete minimum limits from I_{IL} and propagation delays.	1986 OCT 02	M.A. Frye
D	Delete f_{MAX} and t_p clock at +25°C. Change f_{MAX} (-55°C and +125°C). Change table I, I_O (Q and RCO outputs) to I_O (Q outputs) and (CCO outputs, all) to (CCO and RCO outputs, 02). In table I, device type 02, change propagation delay times. Figure 2, device type 01, change RCO:L to RCO:H (last two entries). Figure 2; device type 02. For Q outputs disabled and load, under U/D change the X to an H. Figure 3, change $\overline{ACD}$ to $\overline{RCO}$. Delete footnote 2/ from table I. Editorial changes throughout. Case 2, device 01 is inactive for design.	1987 JUN 10	M.A. Frye
E	Split V_{IL} into temperatures. Add figure 5. Add footnotes to table I. Change propagation delays. Editorial changes throughout. Change in Table II.	1988 MAY 16	M.A. Frye

CURRENT CAGE CODE 67268

REV																							
SHEET																							
REV																							
SHEET																							
REV STATUS OF SHEETS	REV	E	E	E	E	E	E	E	E	D	E	E	D	D	D	D	E	E	E	E	E	E	
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Thomas Poelking

CHECKED BY: Ray Monnin

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 1 MARCH 1984

REVISION LEVEL: E

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, BIPOLAR, ADVANCED LOW-POWER SCHOTTKY TTL, 4-BIT UP/DOWN BINARY COUNTER MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	83025

SHEET 1 OF 21

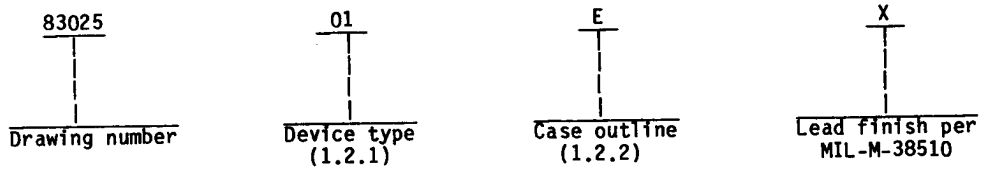
DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912
5962-E898-7

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit
01	54ALS169	Synchronous 4-bit up/down binary counter
02	54ALS569	Synchronous 4-bit up/down binary counter with 3-state outputs

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
F	F-5 (16-lead, .440" x .285" x .085"), flat package
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20-lead, .540" x .300" x .100"), flat package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc minimum to +7.0 V dc maximum
Input voltage range	-1.5 V dc at -18 mA to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation, P_D: 1/	
Device type 01	137.5 mW
Device type 02	176 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1/ Maximum power dissipation is defined as $V_{CC} * I_{CC}$, and must withstand the added P_D due to short-circuit test; e.g., I_O.

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL}):	
V_{IL} = +125°C	0.7 V dc
V_{IL} = +25°C	0.8 V dc
V_{IL} = -55°C	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Width of clock pulse (t_p CLK):	
Device types 01, 02	20 ns minimum
Width of asynchronous clear pulse (t_p $\overline{ACLR}$):	
Device type 02	20 ns minimum
Setup times before clock (t_{su}):	
DATA:	
Device type 01	20 ns minimum
Device type 02	25 ns minimum
Synchronous clear ($\overline{SCLR}$):	
Device type 02 (low)	20 ns minimum
Device type 02 (inactive)	35 ns minimum
Asynchronous clear ($\overline{ACLR}$):	
Device type 02 (inactive)	10 ns minimum
Synchronous $\overline{LOAD}$:	
Device types 01, 02 (low)	20 ns minimum
Device type 02 (inactive)	35 ns minimum
$\overline{ENP}/\overline{ENT}$:	
Device types 01, 02 (low)	25 ns minimum
Device type 01 (high)	25 ns minimum
Device type 02	35 ns minimum
U/$\overline{D}$:	
Device type 01	28 ns minimum
Device type 02	35 ns minimum
Hold time (t_h):	
Device types 01, 02	0 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Counting sequence. The counting sequence shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Switching circuits and waveforms. The switching circuits and waveforms shall be as specified on figure 5.

3.2.6 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified		Device type	Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage	V_{OH1}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} at:	I_{OH} = -0.4 mA 2/ All outputs	01	1, 2, 3	2.5		V
		-55°C = 0.8 V, +25°C = 0.8 V, +125°C = 0.7 V	$\overline{RCO}$ and $\overline{CCO}$	02		2.5		
	V_{OH2}		I_{OH} = -1.0 mA Q outputs	02	1, 2, 3	2.4		V
Low level output voltage	V_{OL1}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} at:	I_{OL} = 4.0 mA 2/ All outputs	01	1, 2, 3		0.4	V
			I_{OL} = 4.0 mA					
		-55°C = 0.8 V, +25°C = 0.8 V, +125°C = 0.7 V	$\overline{RCO}$ and $\overline{CCO}$	02			0.4	V
	V_{OL2}		I_{OL} = 12 mA Q outputs	02			0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA		All	1, 2, 3		-1.5	V
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V, Unused inputs = 4.5 V		All	1, 2, 3		-0.2	mA
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V, Unused inputs = 0.0 V		All	1, 2, 3		20	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 7.0 V, Unused inputs = 0.0 V		All	1, 2, 3		0.1	mA
Output current	I_O	V_{CC} = 5.5 V, V_{OUT} = 2.25 V 3/	Q outputs	All	1, 2, 3	-30	-112	mA
			$\overline{CCO}$ and $\overline{RCO}$ outputs	02		-15	-70	
Off-state output current	I_{OZL}	V_{CC} = 5.5 V, V_{OUT} = 0.4 V	Q outputs	02	1, 2, 3		-20	µA
	I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V	Q outputs	02	1, 2, 3		20	µA
Supply current	I_{CC}	V_{CC} = 5.5 V		01	1, 2, 3		25	mA
Supply current	I_{CCH}	V_{CC} = 5.5 V		02	1, 2, 3		26	mA
	I_{CCL}			02			32	
	I_{CCZ}			02			32	
Functional tests		See 4.3.1c 4/		All	7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$, unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Maximum clock frequency	f_{MAX}	V_{CC} = 4.5 V to 5.5 V C_L = 50 pF R_L = 500Ω 5/ See figures 3 and 5	01	9, 10, 11	25		MHz
			02		22		
Propagation delay time, CLK to Q	t_{PLH1}		01	9, 10, 11	2	15	ns
			02		4	21	
Propagation delay time, CLK to Q	t_{PHL1}		01	9, 10,11	5	20	ns
			02		7	19	
Propagation delay time, CLK to $\overline{RCO}$	t_{PLH2}		01	9, 10, 11	3	20	ns
			02		12	37	ns
	t_{PHL2}		01	9, 10, 11	6	21	ns
			02		10	28	ns
Propagation delay time, CLK to $\overline{CCO}$	t_{PLH3}		02	9, 10, 11	5	17	ns
	t_{PHL3}		02	9, 10, 11	6	30	ns
Propagation delay time, $\overline{ENT}$ to $\overline{RCO}$	t_{PLH4}		01	9, 10, 11	2	14	ns
			02		6	21	
	t_{PHL4}		01	9, 10, 11	3	24	ns
			02		4	20	
Propagation delay time, $\overline{ENT}$ to $\overline{CCO}$	t_{PLH5}		02	9, 10, 11	5	18	ns
	t_{PHL5}		02	9, 10, 11	9	32	ns
Propagation delay time, $\overline{ENP}$ to $\overline{CCO}$	t_{PLH6}		02	9, 10, 11	4	18	ns
	t_{PHL6}		02	9, 10, 11	5	18	ns
Propagation delay time, U/$\overline{D}$ to $\overline{RCO}$	t_{PLH7}		01	9, 10, 11	4	21	ns
			02		9	31	
	t_{PHL7}		01	9, 10, 11	5	26	ns
			02		9	33	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay time, $\overline{ACLR}$ to Q	t_{PHL8}	V_{CC} = 4.5 V to 5.5 V C_L = 50 pF R_L = 500Ω 5/ See figures 3 and 5	02	9, 10, 11	9	25	ns
Enable time, $\overline{G}$ to Q	t_{PZH}		02	9, 10, 11	6	23	ns
	t_{PZL}				6	29	
Disable time, $\overline{G}$ to Q	t_{PHZ}		02	9, 10, 11	1	12	ns
	t_{PLZ}				3	29	

1/ Unused inputs that do not directly control the pin under test must be $\ge$ 2.5 V or $\le$ 0.4 V. No unused inputs shall exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.

2/ All outputs must be tested. In the case where only one input at V_{IL} maximum or V_{IH} minimum produces the proper output state, the test must be performed with each input being selected as the V_{IL} maximum or the V_{IH} minimum input.

3/ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}. Not more than one output will be tested at one time and the duration of the test condition shall not exceed 1 second.

4/ Functional tests shall be conducted at input test conditions of GND $\le V_{IL} \le V_{OL}$ and $V_{OH} \le V_{IH} \le V_{CC}$.

5/ Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or $\le$ 0.3 V.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

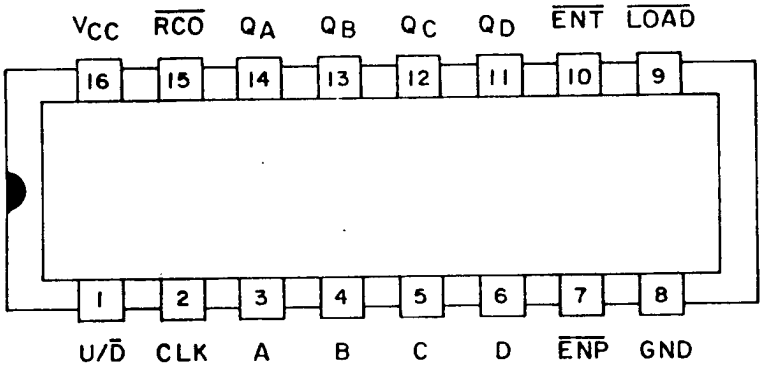
a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 and 8 tests shall verify the truth table as specified on figure 2 herein.

Device type 01

Cases E and F



Device type 01

Case 2

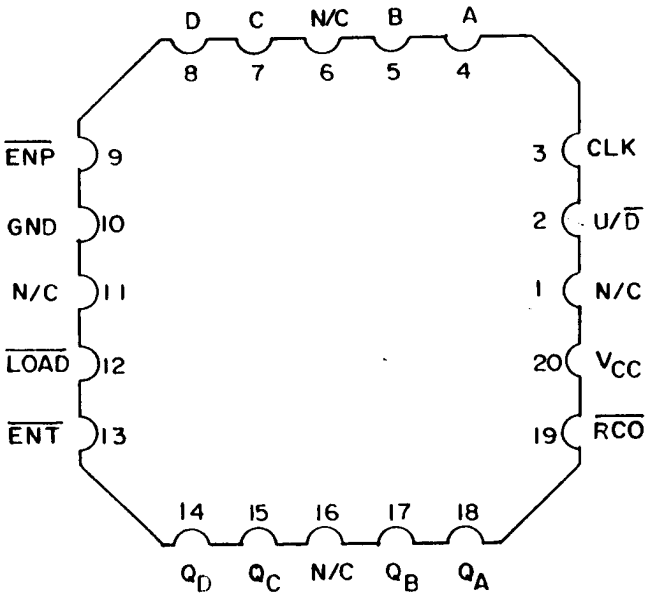
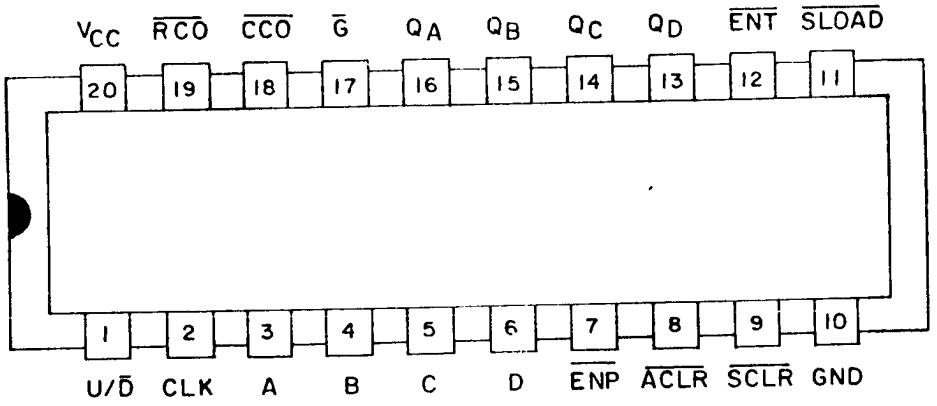


FIGURE 1. Terminal connections.

Device type 02

Cases R and S



Device type 02

Case 2

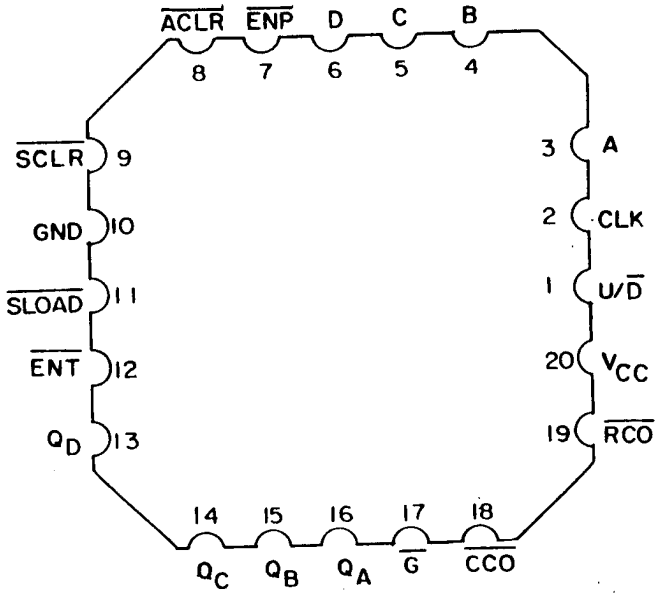


FIGURE 1. Terminal connections - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		83025
		REVISION LEVEL D	SHEET 9

Device type 01

Operation	Inputs at time t_n									Outputs at time t_{n+1}				
	CLK	$\overline{ENP}$	$\overline{ENT}$	$\overline{Load}$	A	B	C	D	U/$\overline{D}$	Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$
Load	↑	L	L	L	X	X	X	X	X	A	B	C	D	L if count = 15 H if count ≠ 15
count up	↑	L	L	H	X	X	X	X	H	Previous count plus 1				L if count = 15 H if count ≠ 15
count down	↑	L	L	H	X	X	X	X	L	Previous count minus 1				L if count = 0 H if count ≠ 0
Inhibit	↑	H	L	H	X	X	X	X	X	No change				No change
	↑	L	H	H	X	X	X	X	X					H
	↑	H	H	H	X	X	X	X	X					H

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level

FIGURE 2. Truth tables.

Count up sequence				
Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$
L	L	L	L	H
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	L	L	H
L	H	L	H	H
L	H	H	L	H
L	H	H	H	H
H	L	L	L	H
H	L	L	H	H
H	L	H	L	H
H	L	H	H	H
H	H	L	L	H
H	H	L	H	H
H	H	H	L	H
H	H	H	H	L

Count down sequence				
Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$
H	H	H	H	H
H	H	H	L	H
H	H	L	H	H
H	H	L	L	H
H	L	H	H	H
H	L	H	L	H
H	L	L	H	H
H	L	L	L	H
L	H	H	L	H
L	H	H	L	H
L	H	L	H	H
L	H	L	L	H
L	L	H	H	H
L	L	H	L	H
L	L	L	H	H
L	L	L	L	L

FIGURE 2. Truth tables - Continued.

Device type 02

Operation	Inputs at time t_n								Outputs at time t_{n+1}									
	$\overline{G}$	$\overline{ACLR}$	$\overline{SCLR}$	$\overline{LOAD}$	$\overline{ENT}$	$\overline{ENP}$	U/$\overline{D}$	CLK	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$	$\overline{CCO}$
Q outputs disabled	H	X	X	X	X	X	H	X	X	X	X	X	Z	Z	Z	Z	L if cnt = 15 H if cnt ≠ 15	1/
Asynchronous clear	L	L	X	X	X	X	X	X	X	X	X	X	L	L	L	L	H	H
Synchronous clear	L	H	L	X	X	X	X	↑	X	X	X	X	L	L	L	L	H	H
Load	L	H	H	L	X	X	H	↑	X	X	X	X	A	B	C	D	L if cnt = 15 H if cnt ≠ 15	1/
Count up	L	H	H	H	L	L	H	↑	X	X	X	x	Previous count plus 1				L if cnt = 15 H if cnt ≠ 15	1/
Count down	L	H	H	H	L	L	L	↑	X	X	X	X	Previous count minus 1				L if cnt = 0 H if cnt ≠ 0	1/
Inhibit count	L	H	H	H	X	H	X	X	X	X	X	X	No change (hold)				2/	1/
	L	H	H	H	H	X	X	X	X	X	X	X						
	L	H	H	H	H	H	X	X	X	X	X	X						

H = High level
L = Low level
Z = Disabled (High impedance state)
X = Irrelevant
↑ = Transition from low to high level

1/ $\overline{CCO}$ produces a low level pulse for the duration equal to that of the low level of the clock when $\overline{RCO}$ is low and the counter is enabled, otherwise, $\overline{CCO}$ is high.
2/ $\overline{RCO}$ produces a low level pulse while the count is 15 when counting up, or while the count is 0 when counting down.

FIGURE 2. Truth tables - Continued.

Count up sequence					
Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$	$\overline{CCO}$
L	L	L	L	H	H
L	L	L	H	H	H
L	L	H	L	H	H
L	L	H	H	H	H
L	H	L	L	H	H
L	H	L	H	H	H
L	H	H	L	H	H
L	H	H	H	H	H
H	L	L	L	H	H
H	L	L	H	H	H
H	L	H	L	H	H
H	L	H	H	H	H
H	H	L	L	H	H
H	H	L	H	H	H
H	H	H	L	H	H
H	H	H	H	L	1/

Count down sequence					
Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$	$\overline{CCO}$
H	H	H	H	H	H
H	H	H	L	H	H
H	H	L	H	H	H
H	H	L	L	H	H
H	L	H	H	H	H
H	L	H	L	H	H
H	L	L	H	H	H
H	L	L	L	H	H
L	H	H	H	H	H
L	H	H	L	H	H
L	H	L	H	H	H
L	H	L	L	H	H
L	L	H	H	H	H
L	L	H	L	H	H
L	L	L	H	H	H
L	L	L	L	L	1/

1/ $\overline{CCO}$ produces a low level pulse for the duration equal to that of the low level of the clock when $\overline{RCO}$ is low and the counter is enabled, otherwise, $\overline{CCO}$ is high.

FIGURE 2. Truth tables - Continued.

Device type 01

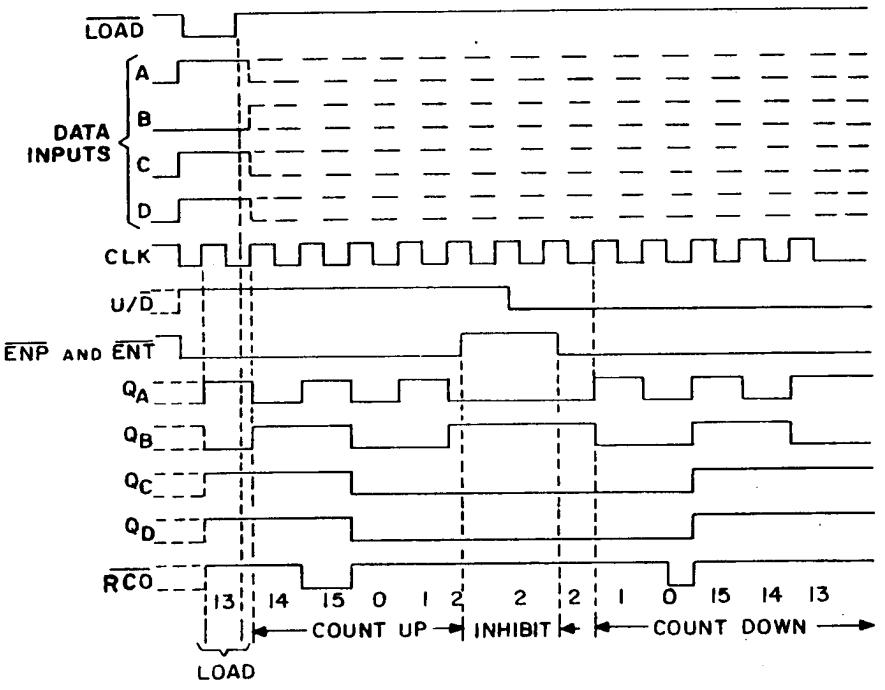


FIGURE 3. Counting sequence.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		83025
		REVISION LEVEL D	SHEET 14

Device type 02

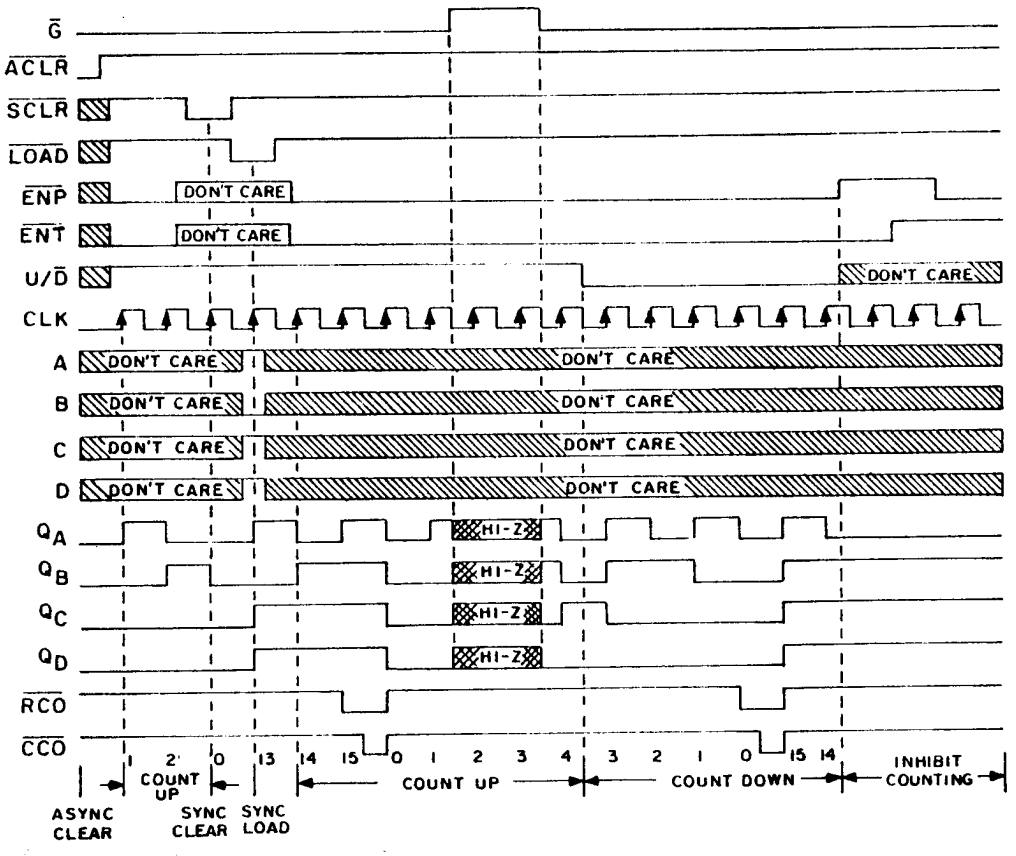


FIGURE 3. Counting sequence - Continued.

Device type 01

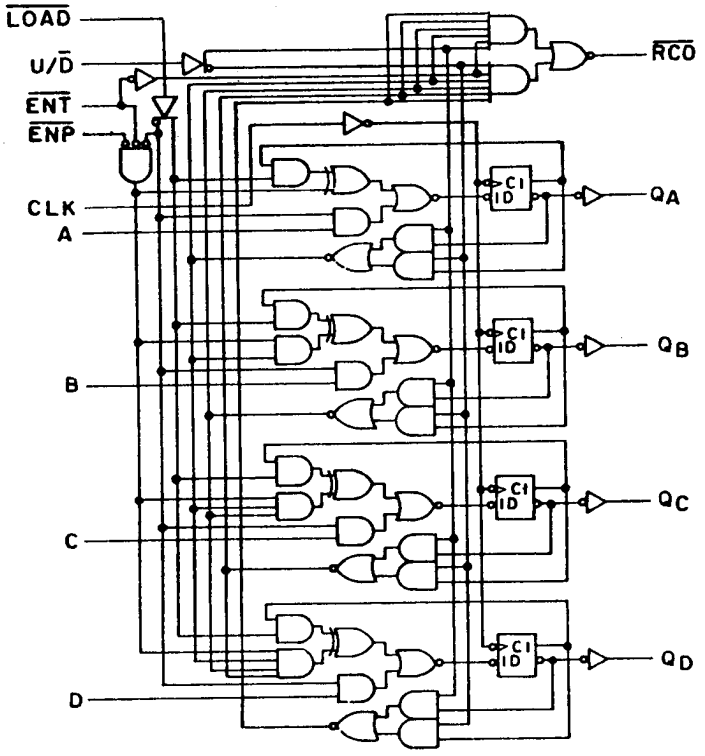


FIGURE 4. Logic diagrams.

Device type 02

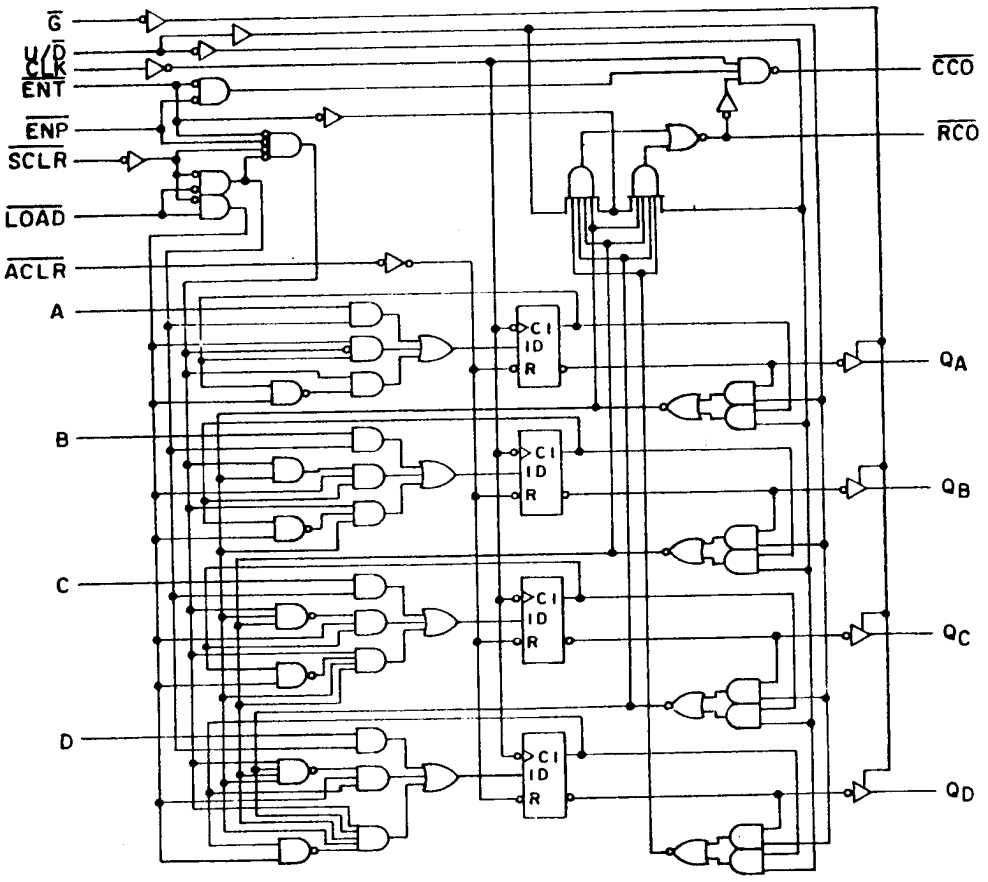
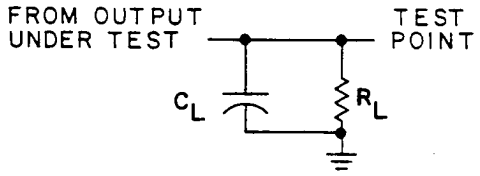
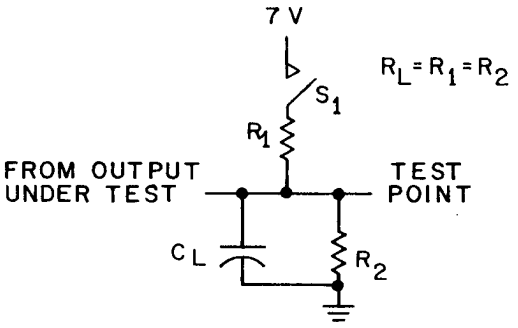


FIGURE 4. Logic diagrams - Continued.

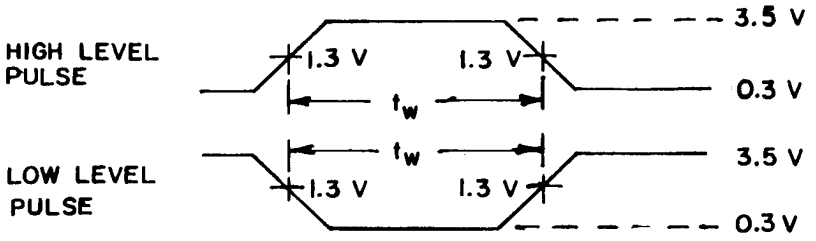
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		83025
		REVISION LEVEL E	SHEET 17



LOAD CIRCUIT FOR
BISTATE
TOTEM POLE OUTPUTS



LOAD CIRCUIT FOR
THREE-STATE OUTPUTS



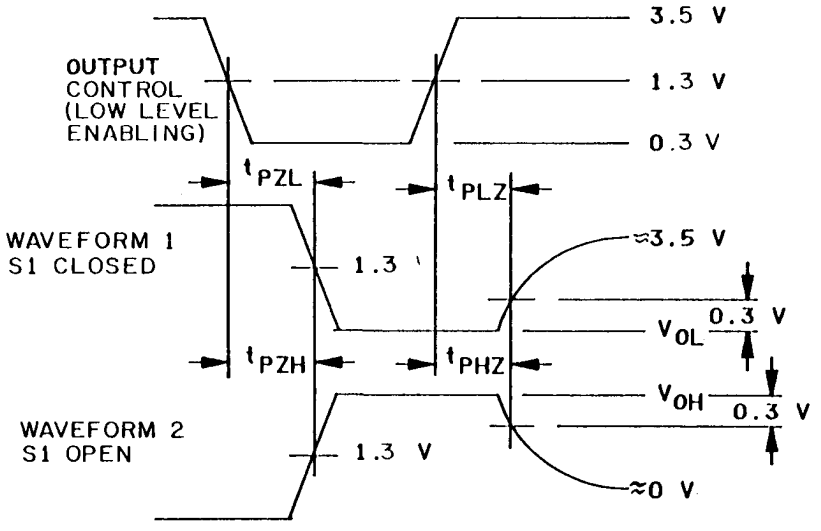
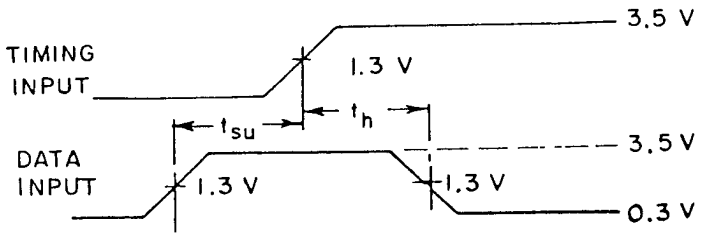
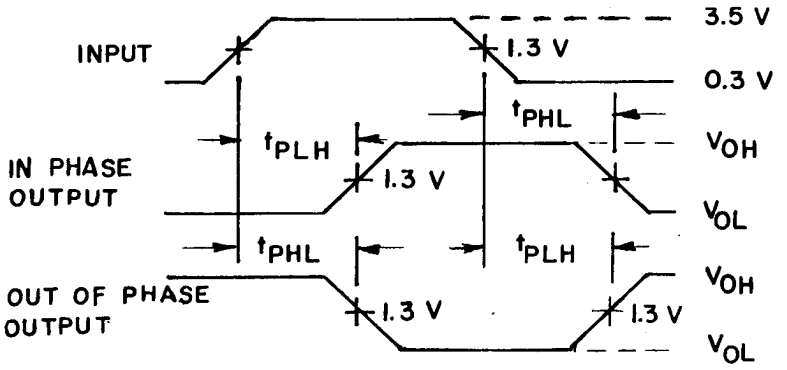


FIGURE 5. Switching circuits and waveforms.





PROPAGATION DELAY TIMES

NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses have the following characteristics: PRR $\leq$ 10 MHz, duty cycle = 50 percent, $t_r = t_f$ = 3 ns ±1 ns.
3. The outputs are measured one at a time with one input transition per measurement.
4. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
5. When measuring propagation delay items of three-state outputs, switch S1 is open.

FIGURE 5. Switching circuits and waveforms - Continued.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/3800XB--.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
8302501EX 2/	27014 01295	54ALS169BJ/883 SNJ54ALS169BJ	M38510/38003BEX
8302501FX	27014	54ALS169BJ/883	M38510/38003BFX
83025012X 2/	27014	54ALS169BW/883	M38510/38003B2X
8302502RX	01295	SNJ54ALS569AJ	M38510/38005BRX
8302502SX	01295	SNJ54ALS569AW	M38510/38005BSX
83025022X	01295	SNJ54ALS569AFK	M38510/38005B2X

010848

011943

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Inactive for new design. Use QPL-38510 product.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporation P.O. Box 6448 Midland, TX 79701
27014	National Semiconductor Corporated. 2900 Semiconductor Drive Santa Clara, CA 95051